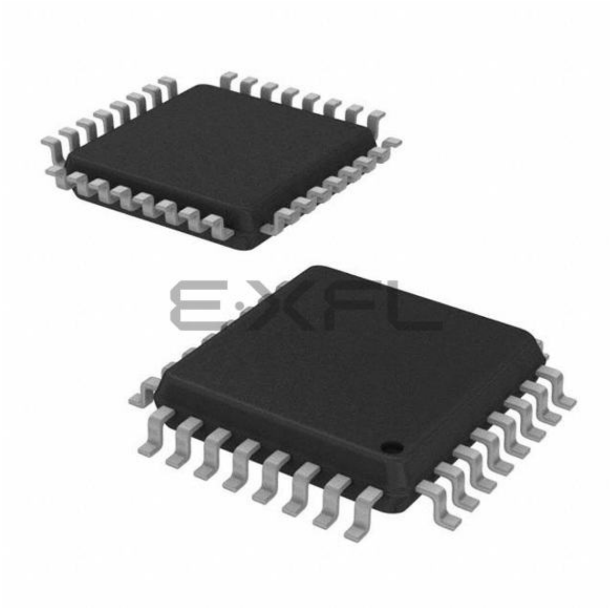

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9keazn16amlc

Field	Description	Values
FFF	Program flash memory size	• 16 = 16 KB • 32 = 32 KB • 64 = 64 KB
M	Maskset revision	• A = 1st Fab version • B = Revision after 1st version
T	Temperature range (°C)	• C = –40 to 85 • V= –40 to 105 • M = –40 to 125
PP	Package identifier	• LC = 32 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm)
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

S9KEAZN64AMLH

3 Ratings

3.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

3.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4 General

4.1 Nonswitching electrical specifications

4.1.1 DC characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 2. DC characteristics

Symbol	Descriptions			Min	Typical[1]	Max	Unit
—	Operating voltage		—	2.7	—	5.5	V
V_{OH}	Output high voltage	All I/O pins, except PTA2 and PTA3, standard-drive strength	5 V, I_{load} = –5 mA	V_{DD} – 0.8	—	—	V
			3 V, I_{load} = –2.5 mA	V_{DD} – 0.8	—	—	V
		High current drive pins, high-drive strength[2]	5 V, I_{load} = –20 mA	V_{DD} – 0.8	—	—	V
			3 V, I_{load} = –10 mA	V_{DD} – 0.8	—	—	V
I_{OHT}	Output high current	Max total I_{OH} for all ports	5 V	—	—	–100	mA
			3 V	—	—	–60	
V_{OL}	Output low voltage	All I/O pins, standard-drive strength	5 V, I_{load} = 5 mA	—	—	0.8	V
			3 V, I_{load} = 2.5 mA	—	—	0.8	V
		High current drive pins, high-drive strength[2]	5 V, I_{load} =20 mA	—	—	0.8	V
			3 V, I_{load} = 10 mA	—	—	0.8	V
I_{OLT}	Output low current	Max total I_{OL} for all ports	5 V	—	—	100	mA
			3 V	—	—	60	
V_{IH}	Input high voltage	All digital inputs	4.5≤V_{DD}<5.5 V	0.65 × V_{DD}	—	—	V
			2.7≤V_{DD}<4.5 V	0.70 × V_{DD}	—	—	
V_{IL}	Input low voltage	All digital inputs	4.5≤V_{DD}<5.5 V	—	—	0.35 × V_{DD}	V
			2.7≤V_{DD}<4.5 V	—	—	0.30 × V_{DD}	
V_{hys}	Input hysteresis	All digital inputs	—	0.06 × V_{DD}	—	—	mV
$\|I_{In}\|$	Input leakage current	Per pin (pins in high impedance input mode)	V_{IN} = V_{DD} or V_{SS}	—	0.1	1	µA

Table continues on the next page...

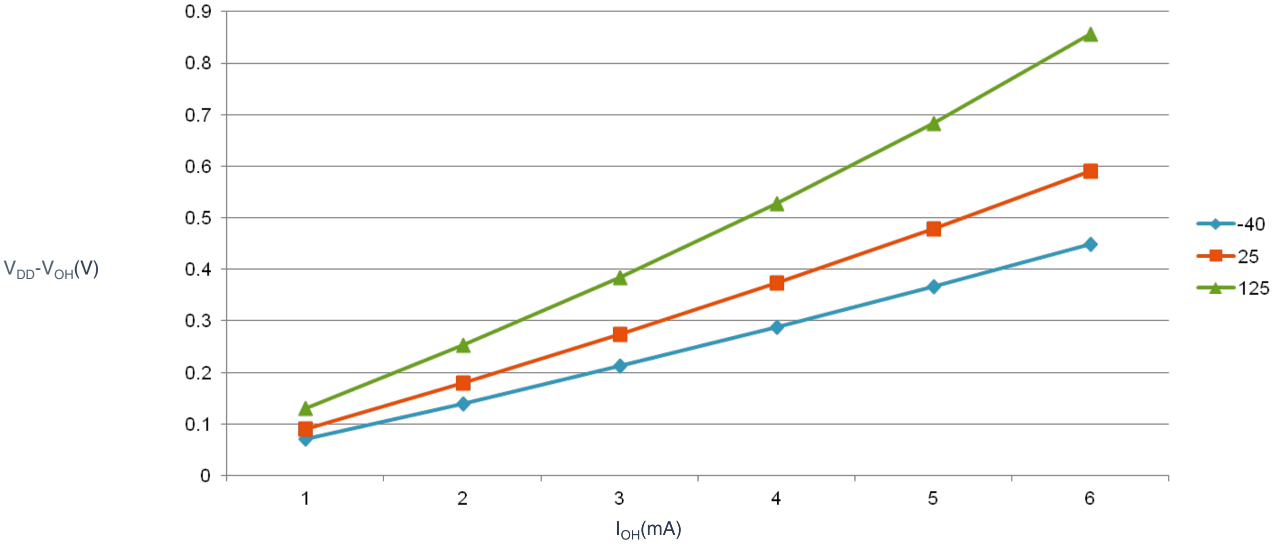

Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

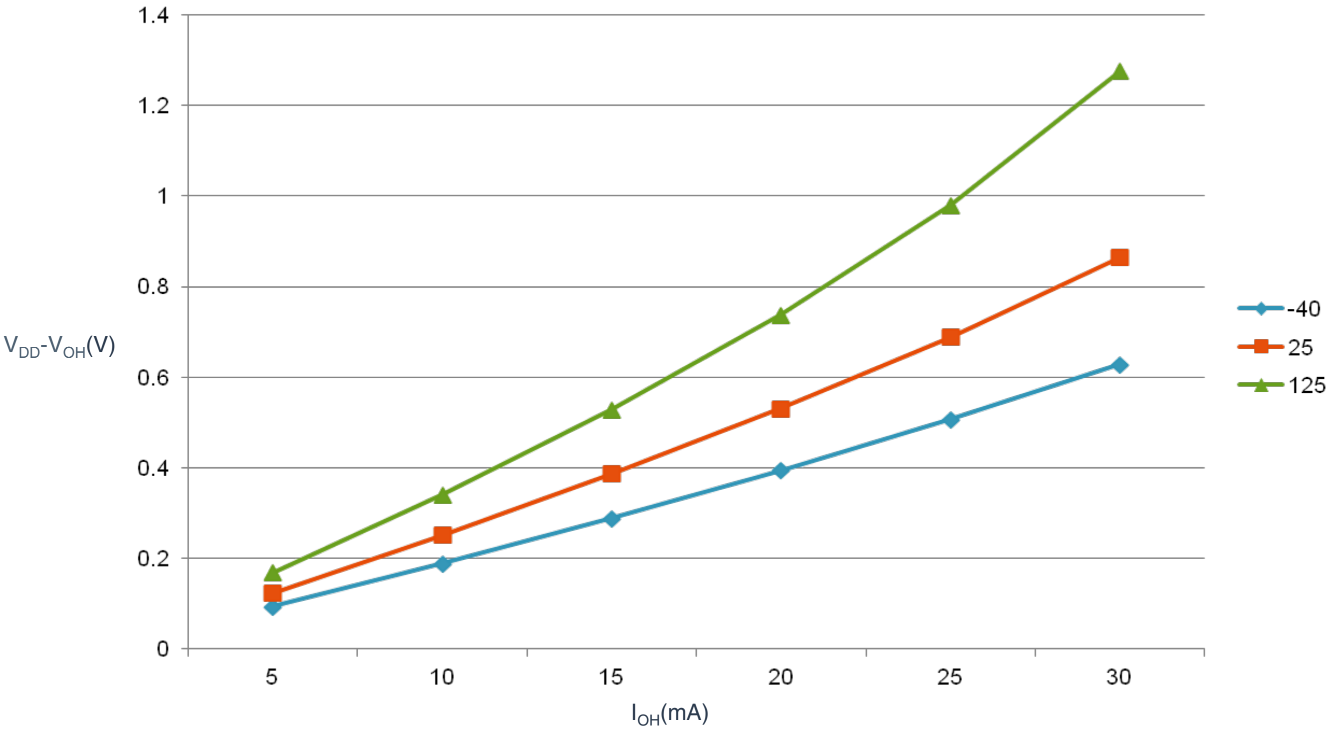

Figure 3. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 5 V)

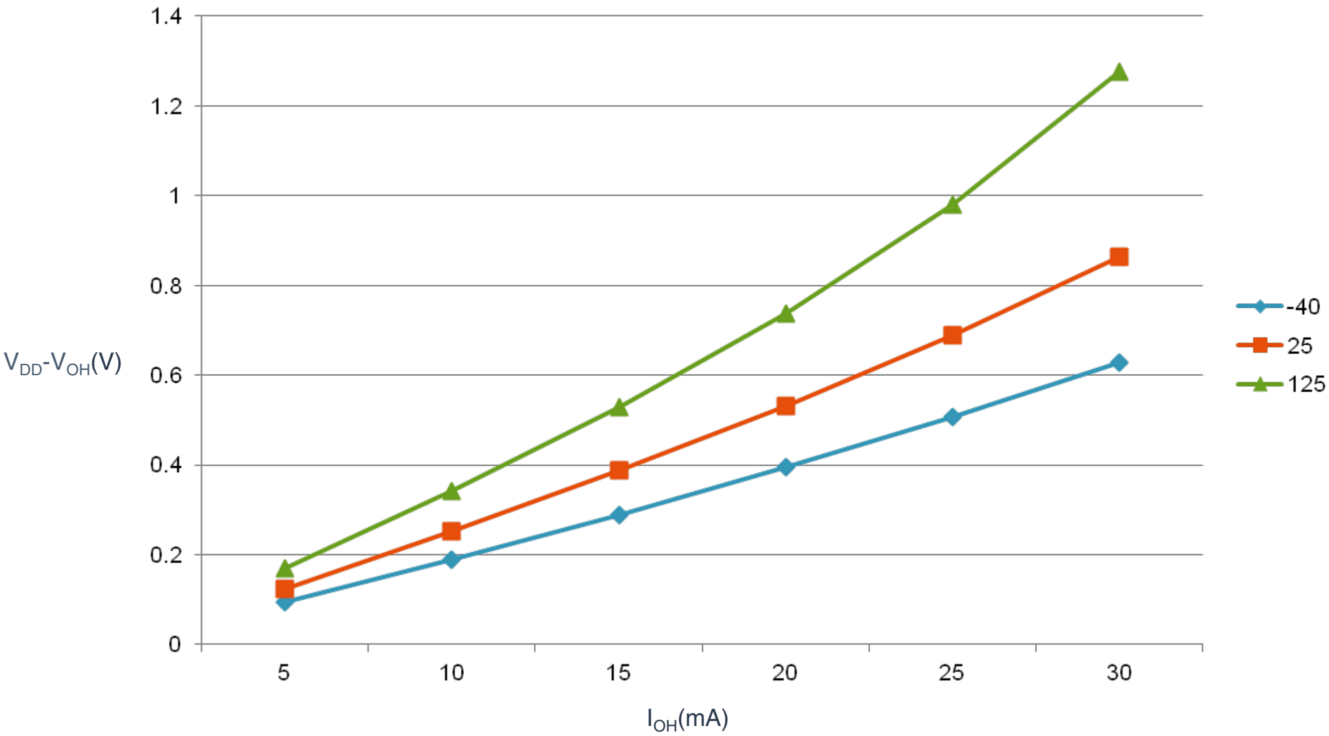

Figure 4. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 3 V)

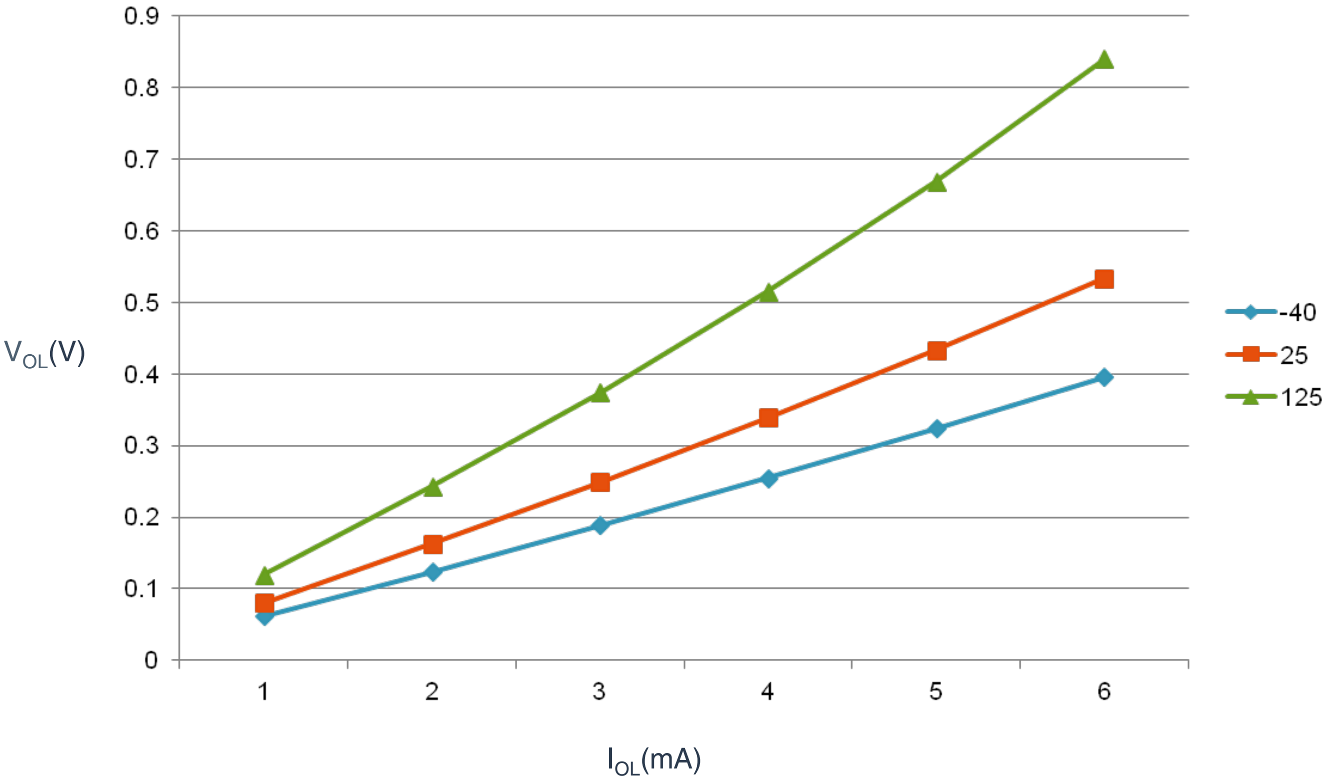

Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

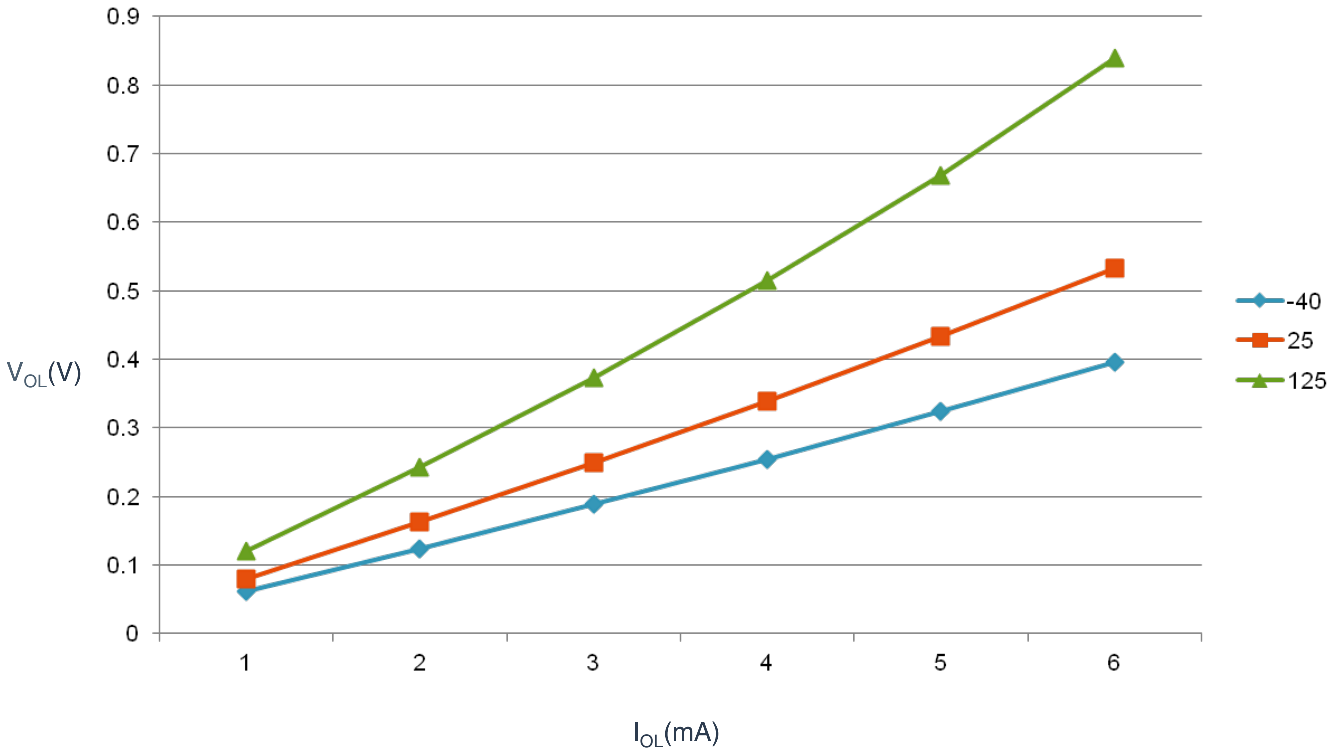

Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 3 V)

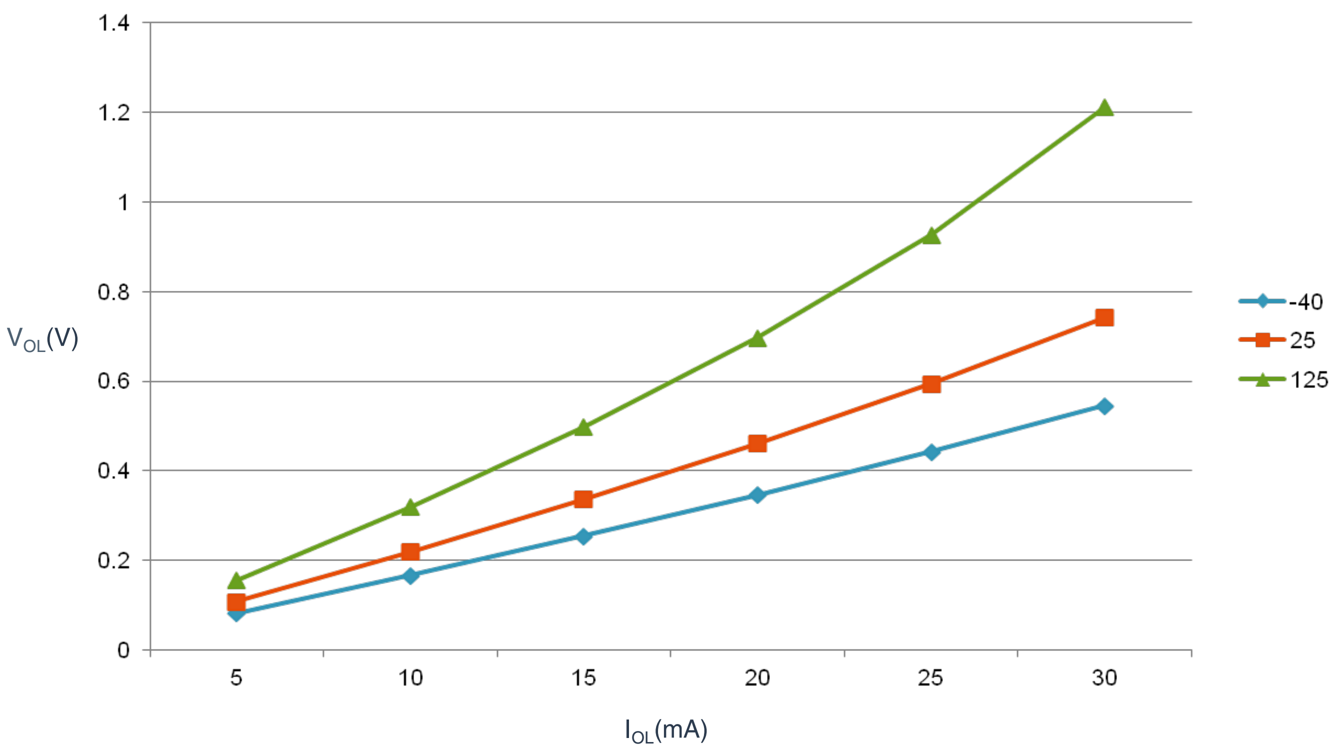

Figure 7. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 5 V)

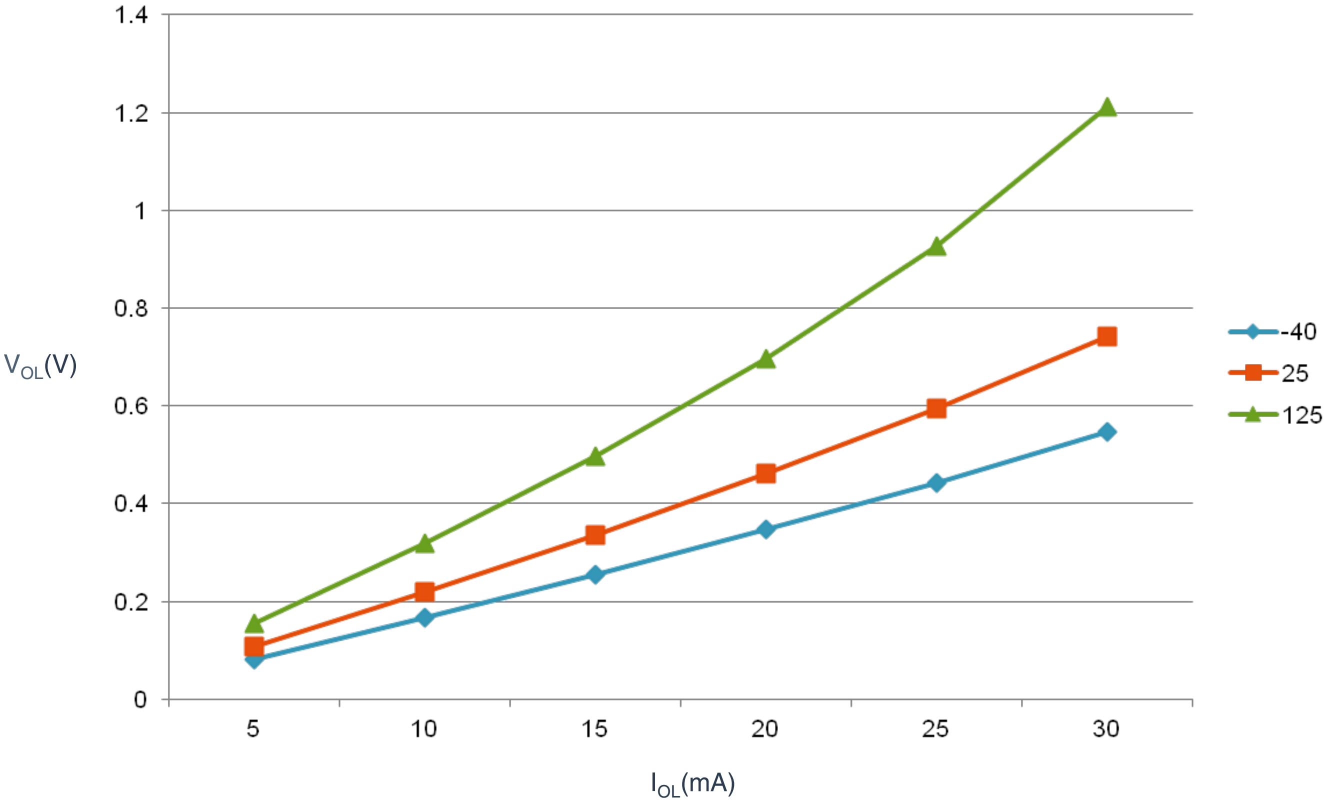

Figure 8. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 3 V)

4.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	20 MHz	5	6.7	—	mA	–40 to 125 °C
		10 MHz		4.5	—		
		1 MHz		1.5	—		
		20 MHz	3	6.6	—		
		10 MHz		4.4	—		
		1 MHz		1.45	—		
Run supply current FEI mode, all modules clocks disabled; run from flash	RI_{DD}	20 MHz	5	5.3	—	mA	–40 to 125 °C
		10 MHz		3.7	—		
		1 MHz		1.5	—		
		20 MHz	3	5.3	—		
		10 MHz		3.7	—		
		1 MHz		1.4	—		

Table continues on the next page...

Table 4. Supply current characteristics (continued)

Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
Run supply current FBE mode, all modules clocks enabled; run from RAM	RI_{DD}	20 MHz	5	9	14.8	mA	–40 to 125 °C
		10 MHz		5.2	—		
		1 MHz		1.45	—		
		20 MHz	3	8.8	11.8		
		10 MHz		5.1	—		
		1 MHz		1.4	—		
Run supply current FBE mode, all modules clocks disabled; run from RAM	RI_{DD}	20 MHz	5	8	12.3	mA	–40 to 125 °C
		10 MHz		4.4	—		
		1 MHz		1.35	—		
		20 MHz	3	7.8	9.2		
		10 MHz		4.2	—		
		1 MHz		1.3	—		
Wait mode current FEI mode, all modules clocks enabled	WI_{DD}	20 MHz	5	5.5	7	mA	–40 to 125 °C
		10 MHz		3.5	—		
		1 MHz		1.4	—		
		20 MHz	3	5.4	6.9		
		10 MHz		3.4	—		
		1 MHz		1.4	—		
Stop mode supply current no clocks active (except 1 kHz LPO clock)[2]	SI_{DD}	—	5	2	145	μA	–40 to 125 °C
		—	3	1.9	135		–40 to 125 °C
ADC adder to Stop ADLPC = 1 ADLSMP = 1 ADCO = 1 MODE = 10B ADICLK = 11B	—	—	5	86 (64-pin packages) 42 (32-pin package)	—	μA	–40 to 125 °C
			3	82 (64-pin packages) 41 (32-pin package)	—		
ACMP adder to Stop	—	—	5	12	—	μA	–40 to 125 °C
			3	12	—		
LVD adder to stop[3]	—	—	5	128	—	μA	–40 to 125 °C
			3	124	—		

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. RTC adder causes I_{DD} to increase typically by less than 1 μA; RTC clock source is 1 kHz LPO clock.
3. LVD is periodically woken up from Stop by 5% duty cycle. The period is equal to or less than 2 ms.

4.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following NXP applications notes, available on **nxp.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

4.2 Switching specifications

4.2.1 Control timing

Table 5. Control timing

Num	Rating		Symbol	Min	Typical[1]	Max	Unit
1	System and core clock		f_{Sys}	DC	—	40	MHz
2	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	20	MHz
3	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
4	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
5	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
6	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
		Synchronous path[3]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
7	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
		Synchronous path	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
8	Port rise and fall time - Normal drive strength (load = 50 pF)[4]	—	t_{Rise}	—	10.2	—	ns
			t_{Fall}	—	9.5	—	ns
	Port rise and fall time - high drive strength (load = 50 pF)[4]	—	t_{Rise}	—	5.4	—	ns
			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a $\overline{RESET}$ pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 125 °C.

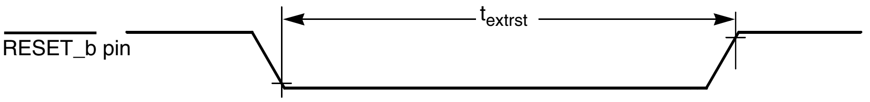

Figure 9. Reset timing

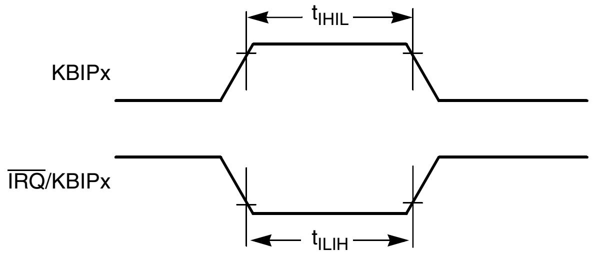

Figure 10. KBIPx timing

4.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 6. FTM input timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
External clock period	t_{TCLK}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

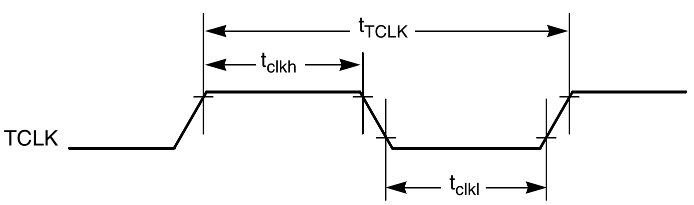

Figure 11. Timer external clock

4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T_J) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

5 Peripheral operating requirements and behaviors

5.1 Core modules

5.1.1 SWD electricals

Table 8. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation			

Table continues on the next page...

Table 8. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

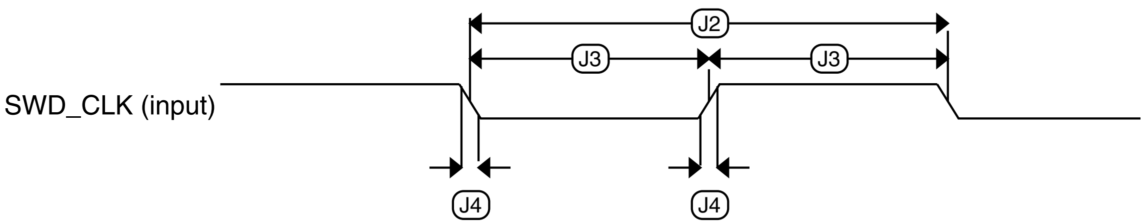

Figure 13. Serial wire clock input timing

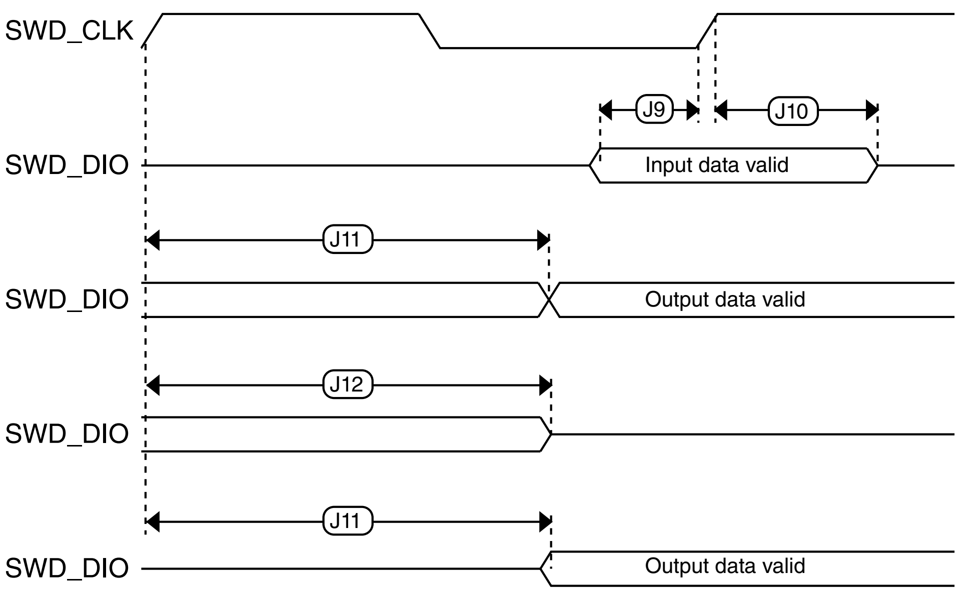

Figure 14. Serial wire data timing

5.2 External oscillator (OSC) and ICS characteristics

Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	Crystal or resonator frequency	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
		High range (RANGE = 1)	f_{hi}	4	—	20	MHz
2	Load capacitors		C1, C2	See Note[2]			
3	Feedback resistor	Low Frequency, Low-Power Mode[3]	R_F	—	—	—	MΩ
		Low Frequency, High-Gain Mode		—	10	—	MΩ
		High Frequency, Low-Power Mode		—	1	—	MΩ
		High Frequency, High-Gain Mode		—	1	—	MΩ
4	Series resistor - Low Frequency	Low-Power Mode [3]	R_S	—	0	—	kΩ
		High-Gain Mode		—	200	—	kΩ
5	Series resistor - High Frequency	Low-Power Mode[3]	R_S	—	0	—	kΩ
	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
		8 MHz		—	0	—	kΩ
		16 MHz		—	0	—	kΩ
6	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal[4,5]	Low range, low power	t_{CSTL}	—	1000	—	ms
		Low range, high gain		—	800	—	ms
		High range, low power	t_{CSTH}	—	3	—	ms
		High range, high gain		—	1.5	—	ms
7	Internal reference start-up time		t_{IRST}	—	20	50	μs
8	Internal reference clock (IRC) frequency trim range		f_{int_t}	31.25	—	39.0625	kHz
9	Internal reference clock frequency, factory trimmed	T = 125 °C, V_{DD} = 5 V	f_{int_ft}	—	31.25	—	kHz
10	DCO output frequency range	FLL reference = fint_t, flo, or fhi/RDIV	f_{dco}	—	—	—	MHz
11	Factory trimmed internal oscillator accuracy	T = 125 °C, V_{DD} = 5 V	Δf_{int_ft}	-0.8	—	0.8	%
12	Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 5 V	Over temperature range from -40 °C to 125°C	Δf_{int_t}	-1	—	0.8	%

Table continues on the next page...

Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient) (continued)

Num	Characteristic		Symbol	Min	Typical[1]	Max	Unit
13	Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 125°C	Δf_{dco_ft}	-2.3	—	0.8	%
14	FLL acquisition time[4,6]		$t_{Acquire}$	—	—	2	ms
15	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

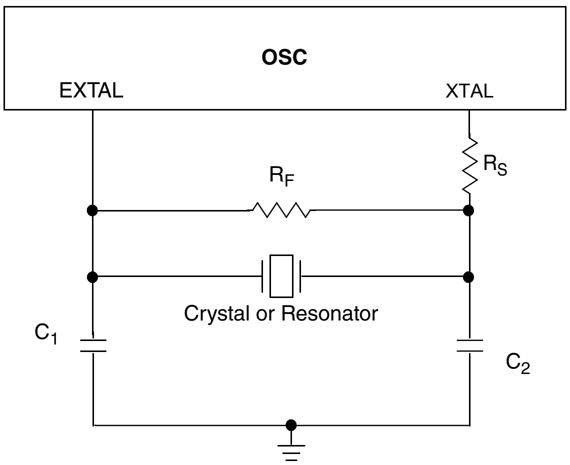

Figure 15. Typical crystal or resonator circuit

5.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 10. Flash and EEPROM characteristics

Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
Supply voltage for program/erase –40 °C to 125 °C	$V_{prog/erase}$	2.7	—	5.5	V
Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
NVM Bus frequency	f_{NVMBUS}	1	—	20	MHz
NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
Erase Verify All Blocks	t_{VFYALL}	—	—	2605	t_{cyc}
Erase Verify Flash Block	t_{RD1BLK}	—	—	2579	t_{cyc}
Erase Verify EEPROM Block	t_{RD1BLK}	—	—	810	t_{cyc}
Erase Verify Flash Section	t_{RD1SEC}	—	—	485	t_{cyc}
Erase Verify EEPROM Section	$t_{DRD1SEC}$	—	—	555	t_{cyc}
Read Once	t_{RDONCE}	—	—	464	t_{cyc}
Program Flash (2 word)	t_{PGM2}	0.12	0.13	0.31	ms
Program Flash (4 word)	t_{PGM4}	0.21	0.21	0.49	ms
Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
Program EEPROM (1 Byte)	t_{DPGM1}	0.10	0.10	0.27	ms
Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.43	ms
Program EEPROM (3 Byte)	t_{DPGM3}	0.25	0.26	0.60	ms
Program EEPROM (4 Byte)	t_{DPGM4}	0.32	0.33	0.77	ms
Erase All Blocks	t_{ERSALL}	95.42	100.18	100.30	ms
Erase Flash Block	t_{ERSBLK}	95.42	100.18	100.30	ms
Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.09	ms
Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	20.57	ms
Unsecure Flash	t_{UNSECU}	95.42	100.19	100.31	ms
Verify Backdoor Access Key	t_{VFYKEY}	—	—	482	t_{cyc}
Set User Margin Level	t_{MLOADU}	—	—	415	t_{cyc}
FLASH Program/erase endurance T_L to T_H = -40 °C to 125 °C	n_{FLPE}	10 k	100 k	—	Cycles
EEPROM Program/erase endurance TL to TH = -40 °C to 125 °C	n_{FLPE}	50 k	500 k	—	Cycles
Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

5.4 Analog

5.4.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDA})	ΔV_{DDA}	-100	0	+100	mV	—
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})	ΔV_{SSA}	-100	0	+100	mV	—
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	—
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 12. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit
	Low power (ADLPC = 1)		1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)		—	40	—	
Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)		—	23.5	—	
Total unadjusted Error[2]	12-bit mode	E_{TUE}	—	±5.0	—	LSB[3]
	10-bit mode		—	±1.5	±2.0	
	8-bit mode		—	±0.7	±1.0	
Differential Non-Liniarity	12-bit mode	DNL	—	±1.0	—	LSB[3]
	10-bit mode[4]		—	±0.25	±0.5	
	8-bit mode[4]		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	INL	—	±1.0	—	LSB[3]
	10-bit mode		—	±0.3	±0.5	
	8-bit mode		—	±0.15	±0.25	
Zero-scale error[5]	12-bit mode	E_{ZS}	—	±2.0	—	LSB[3]
	10-bit mode		—	±0.25	±1.0	
	8-bit mode		—	±0.65	±1.0	
Full-scale error[6]	12-bit mode	E_{FS}	—	±2.5	—	LSB[3]
	10-bit mode		—	±0.5	±1.0	
	8-bit mode		—	±0.5	±1.0	
Quantization error	≤12 bit modes	E_Q	—	—	±0.5	LSB[3]
Input leakage error[7]	all modes	E_{IL}	$I_{In} \times R_{AS}$			mV
Temp sensor slope	-40 °C–25 °C	m	—	3.266	—	mV/°C
	25 °C–125 °C		—	3.638	—	
Temp sensor voltage	25 °C	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{In} = leakage current (refer to DC characteristics)

5.4.2 Analog comparator (ACMP) electricals

Table 13. Comparator electrical specifications

Characteristic	Symbol	Min	Typical	Max	Unit
Supply voltage	V_{DDA}	2.7	—	5.5	V
Supply current (Operation mode)	I_{DDA}	—	10	20	µA
Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
Analog input offset voltage	V_{AIO}	—	—	40	mV
Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
Propagation Delay	t_D	—	0.4	1	µs

5.5 Communication interfaces

5.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for communicating with slower peripheral devices. All timing is shown with respect to 20% V_{DD} and 80% V_{DD}, unless noted, and 25 pF load on all SPI pins. All timing assumes slew rate control is disabled and high-drive strength is enabled for SPI output pins.

Table 14. SPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	f_{Bus}/2048	f_{Bus}/2	Hz	f_{Bus} is the bus clock
2	t_{SPSCK}	SPSCK period	2 x t_{Bus}	2048 x t_{Bus}	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} – 30	1024 x t_{Bus}	ns	—
6	t_{SU}	Data setup time (inputs)	8	—	ns	—
7	t_{HI}	Data hold time (inputs)	8	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	25	ns	—
9	t_{HO}	Data hold time (outputs)	20	—	ns	—

Table continues on the next page...

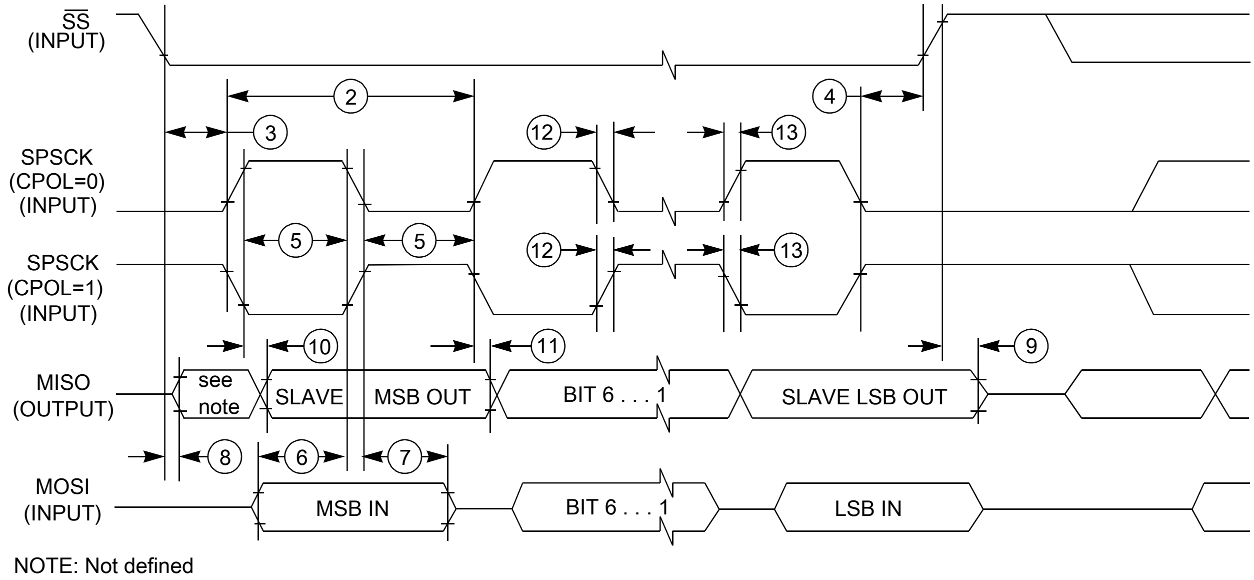

Figure 20. SPI slave mode timing (CPHA=1)

6 Dimensions

6.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **nxp.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
64-pin LQFP	98ASS23234W

7 Pinout

7.1 Signal multiplexing and pin assignments

For the pin muxing details see section Signal Multiplexing and Signal Descriptions of KEA64 Reference Manual.

8 Revision History

The following table provides a revision history for this document.

Table 16. Revision History

Rev. No.	Date	Substantial Changes
Rev. 1	11 March 2014	Initial Release
Rev. 2	18 June 2014	• Parameter Classification section is removed. • Classification column is removed from all the tables in the document. • Supply current characteristics section is updated.

Rev. 3	18 July 2014	• ESD handling ratings section is updated.
		• Figures in DC characteristics section are updated.
		• Specs updated in following tables:
		  • Table 9.
		  • Table 4.

Rev. 4	03 Sept 2014	• Data Sheet type changed to "Technical Data".
Rev. 5	12 May 2016	• In section: Key features, Changed the number of instances of IIC to 1.

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Document Number S9KEA64P64M20SF0
Revision 5, 05/2016