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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/s9keazn64amlh

Table of Contents

Field	Description	Values
FFF	Program flash memory size	• 16 = 16 KB • 32 = 32 KB • 64 = 64 KB
M	Maskset revision	• A = 1st Fab version • B = Revision after 1st version
T	Temperature range (°C)	• C = –40 to 85 • V= –40 to 105 • M = –40 to 125
PP	Package identifier	• LC = 32 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm)
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

S9KEAZN64AMLH

3 Ratings

3.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

3.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

3.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*. The test produced the following results:
   - Test was performed at 125 °C case temperature (Class II).
   - I/O pins pass +100/-100 mA I-test with I_{DD} current limit at 800 mA (V_{DD} collapsed during positive injection).
   - I/O pins pass +70/-100 mA I-test with I_{DD} current limit at 1000 mA for V_{DD}.
   - Supply groups pass 1.5 V_{ccmax}.
   - RESET_B pin was only tested with negative I-test due to product conditioning requirement.

3.4 Voltage and current operating ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this document.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pullup resistor associated with the pin is enabled.

Table 1. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	6.0	V
I_{DD}	Maximum current into V_{DD}	—	120	mA
V_{IN}	Input voltage except true open drain pins	–0.3	V_{DD} + 0.3[1]	V
	Input voltage of true open drain pins	–0.3	6	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum rating of V_{DD} also applies to V_{IN}.

Table 2. DC characteristics (continued)

Symbol	Descriptions			Min	Typical[1]	Max	Unit
$\lvert I_{INTOT} \rvert$	Total leakage combined for all port pins	Pins in high impedance input mode	$V_{IN} = V_{DD}$ or V_{SS}	—	—	2	µA
R_{PU}	Pullup resistors	All digital inputs, when enabled (all I/O pins other than PTA2 and PTA3)	—	30.0	—	50.0	kΩ
R_{PU}[3]	Pullup resistors	PTA2 and PTA3 pins	—	30.0	—	60.0	kΩ
I_{IC}	DC injection current[4, 5, 6]	Single pin limit	$V_{IN} < V_{SS}$, $V_{IN} > V_{DD}$	-2	—	2	mA
		Total MCU limit, includes sum of all stressed pins		-5	—	25	
C_{In}	Input capacitance, all pins		—	—	—	7	pF
V_{RAM}	RAM retention voltage		—	2.0	—	—	V

1. Typical values are measured at 25 °C. Characterized, not tested.
2. Only PTB4, PTB5, PTD0, PTD1, PTE0, PTE1, PTH0, and PTH1 support high current output.
3. The specified resistor value is the actual value internal to the device. The pullup value may appear higher when measured externally on the pin.
4. All functional non-supply pins, except for PTA2 and PTA3, are internally clamped to V_{SS} and V_{DD}. PTA2 and PTA3 are true open drain I/O pins that are internally clamped to V_{SS}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger value.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If the positive injection current ($V_{In} > V_{DD}$) is higher than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure that external V_{DD} load will shunt current higher than maximum injection current when the MCU is not consuming power, such as when no system clock is present, or clock rate is very low (which would reduce overall power consumption).

Table 3. LVD and POR specification

Symbol	Description		Min	Typ	Max	Unit
V_{POR}	POR re-arm voltage[1]		1.5	1.75	2.0	V
V_{LVDH}	Falling low-voltage detect threshold—high range (LVDV = 1)[2]		4.2	4.3	4.4	V
V_{LVW1H}	Falling low-voltage warning threshold— high range	Level 1 falling (LVWV = 00)	4.3	4.4	4.5	V
V_{LVW2H}		Level 2 falling (LVWV = 01)	4.5	4.5	4.6	V
V_{LVW3H}		Level 3 falling (LVWV = 10)	4.6	4.6	4.7	V
V_{LVW4H}		Level 4 falling (LVWV = 11)	4.7	4.7	4.8	V
V_{HYSH}	High range low-voltage detect/ warning hysteresis		—	100	—	mV

Table continues on the next page...

Table 3. LVD and POR specification (continued)

Symbol	Description		Min	Typ	Max	Unit
V_{LVDL}	Falling low-voltage detect threshold—low range (LVDV = 0)		2.56	2.61	2.66	V
V_{LVW1L}	Falling low-voltage warning threshold—low range	Level 1 falling (LVWV = 00)	2.62	2.7	2.78	V
V_{LVW2L}		Level 2 falling (LVWV = 01)	2.72	2.8	2.88	V
V_{LVW3L}		Level 3 falling (LVWV = 10)	2.82	2.9	2.98	V
V_{LVW4L}		Level 4 falling (LVWV = 11)	2.92	3.0	3.08	V
V_{HYSDL}	Low range low-voltage detect hysteresis		—	40	—	mV
V_{HYSWL}	Low range low-voltage warning hysteresis		—	80	—	mV
V_{BG}	Buffered bandgap output [3]		1.14	1.16	1.18	V

1. Maximum is highest voltage that POR is guaranteed.
2. Rising thresholds are falling threshold + hysteresis.
3. voltage Factory trimmed at V_{DD} = 5.0 V, Temp = 125 °C

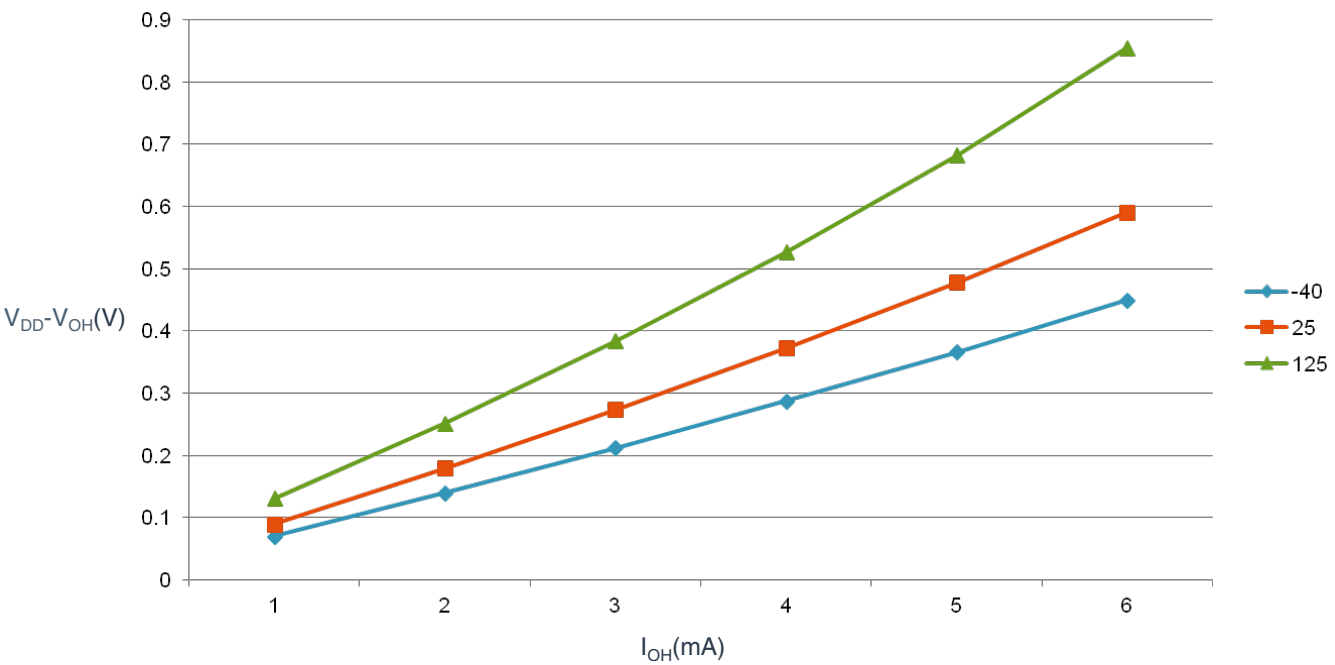


Figure 1. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 5 V)

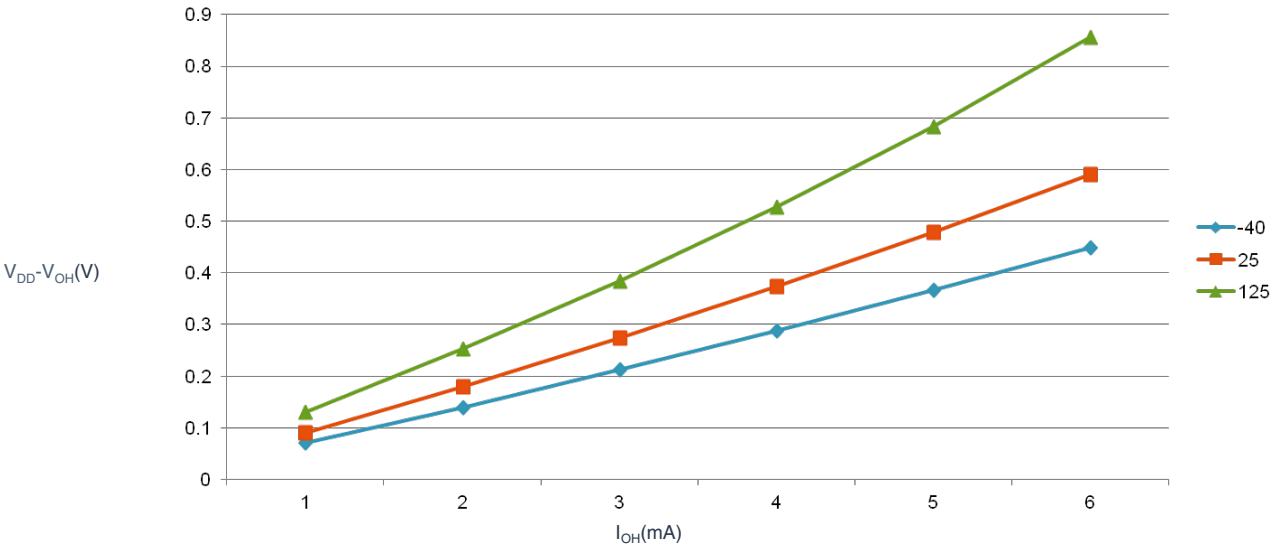


Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

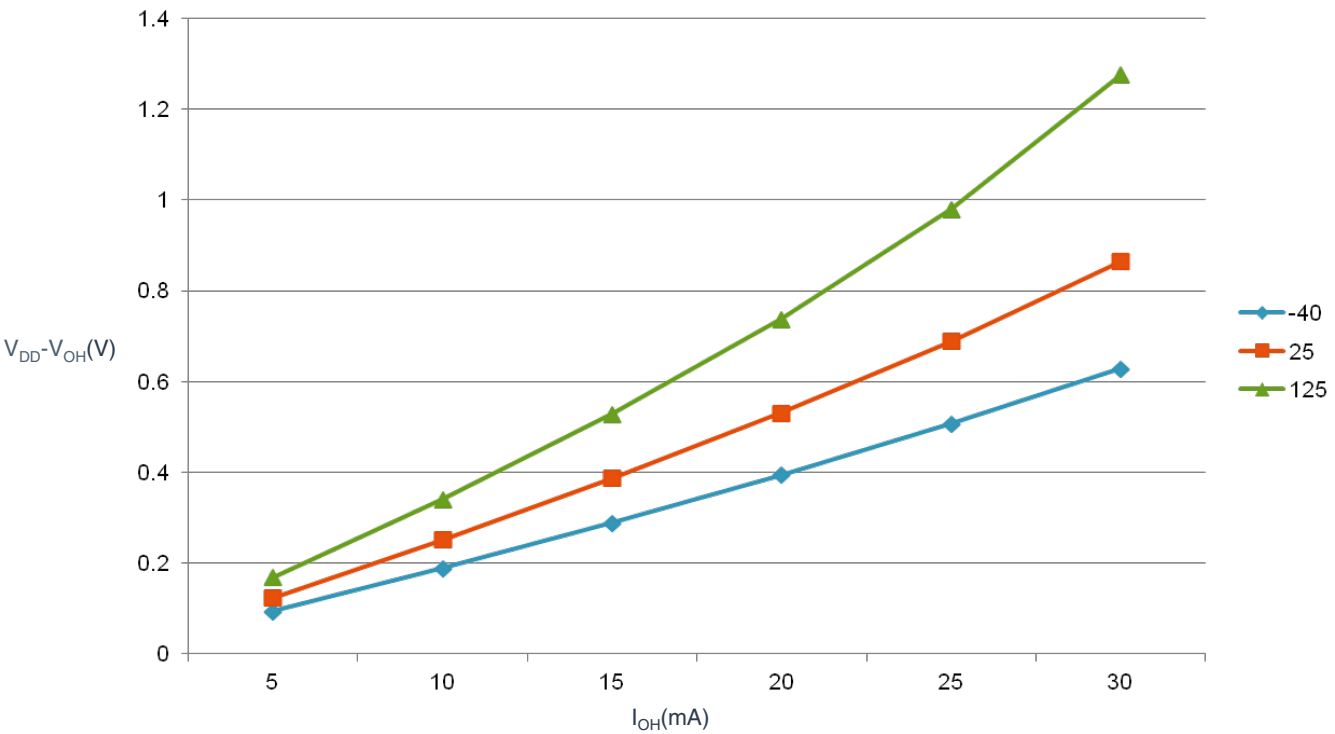


Figure 3. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 5 V)

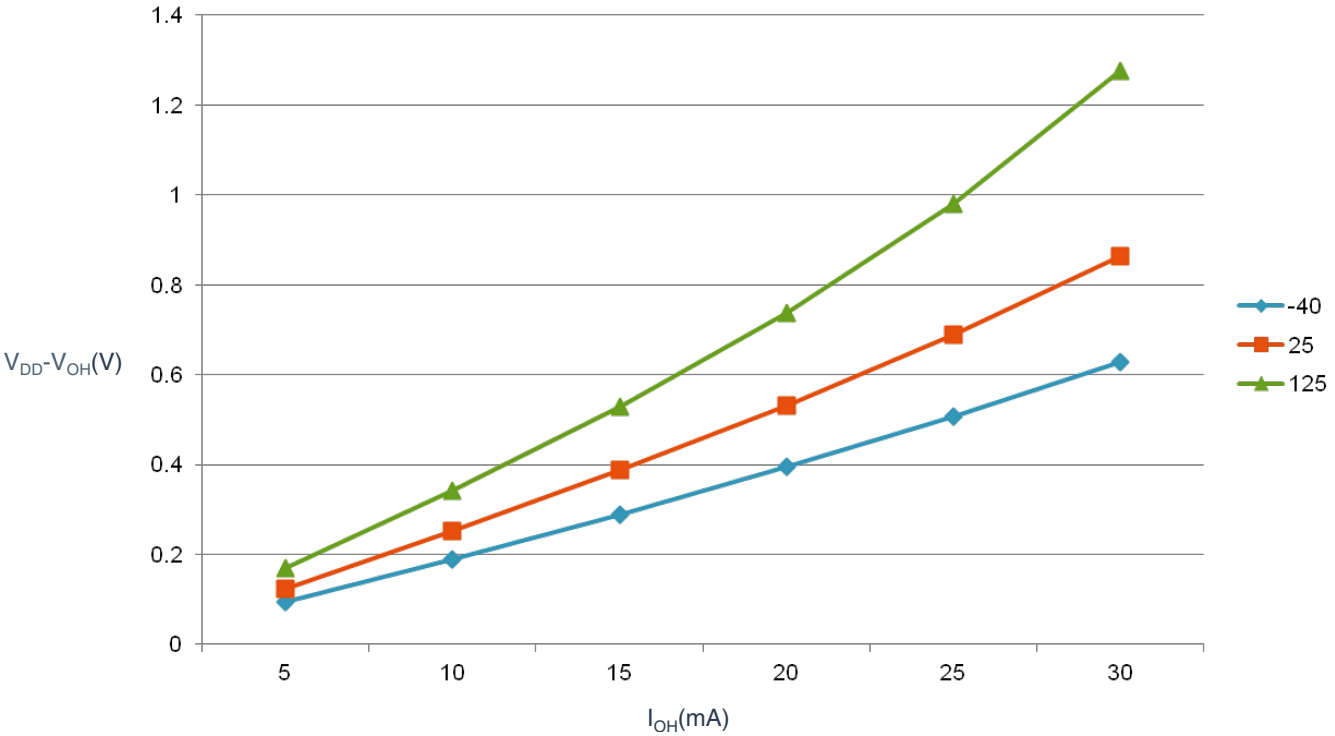


Figure 4. Typical V_{DD}-V_{OH} Vs. I_{OH} (high drive strength) (V_{DD} = 3 V)

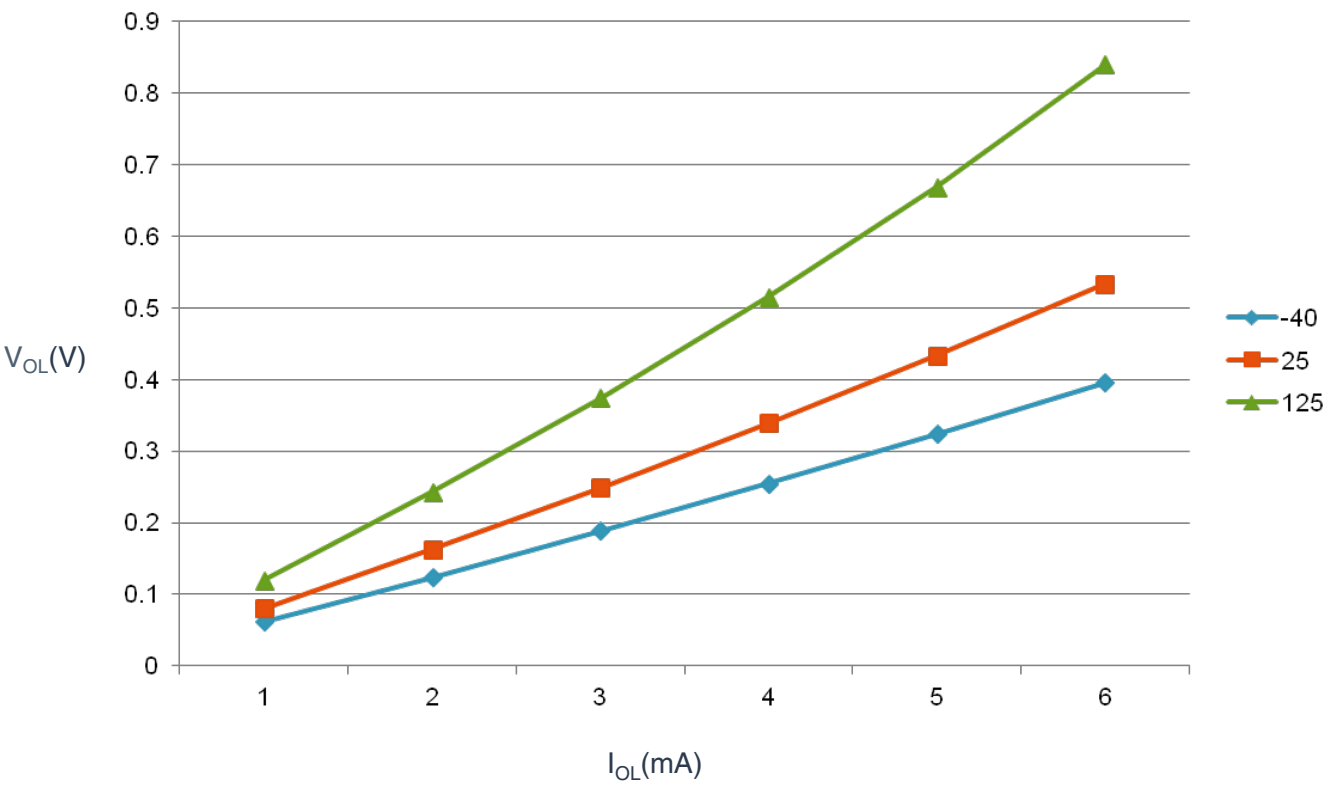


Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

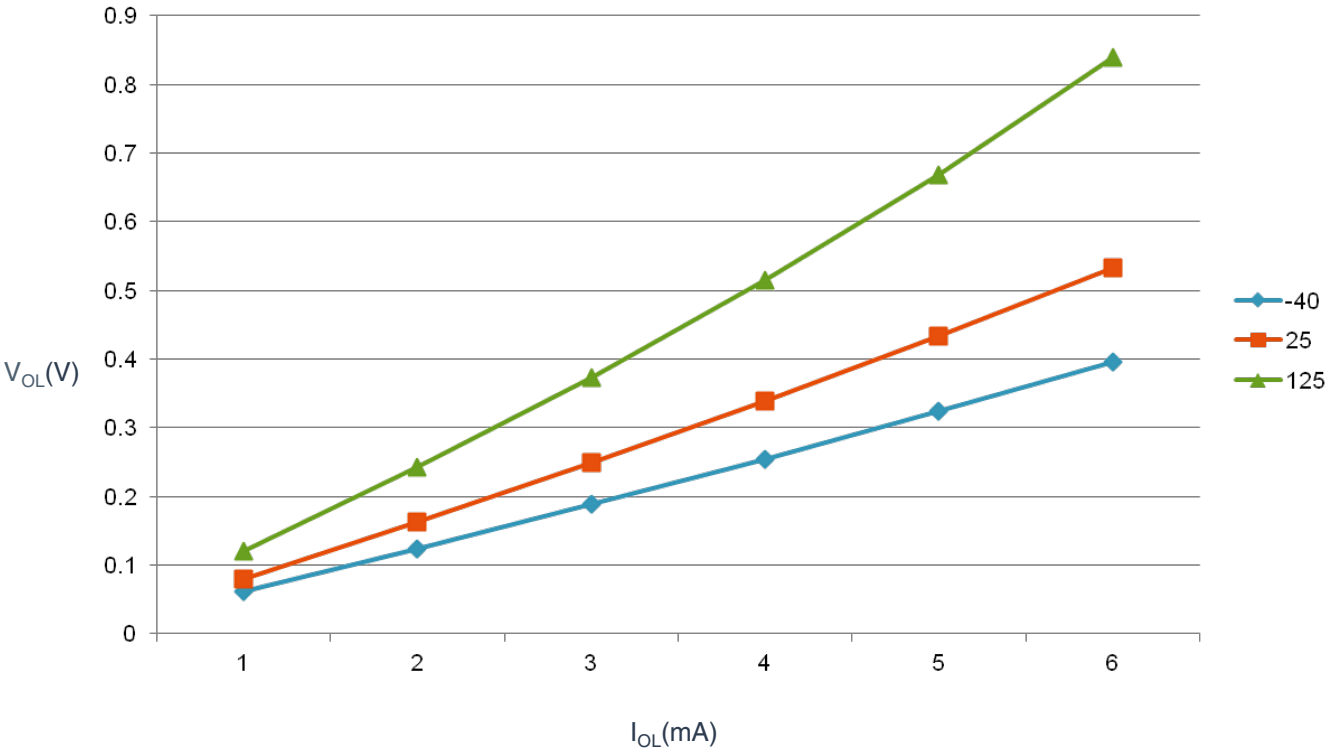


Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 3 V)

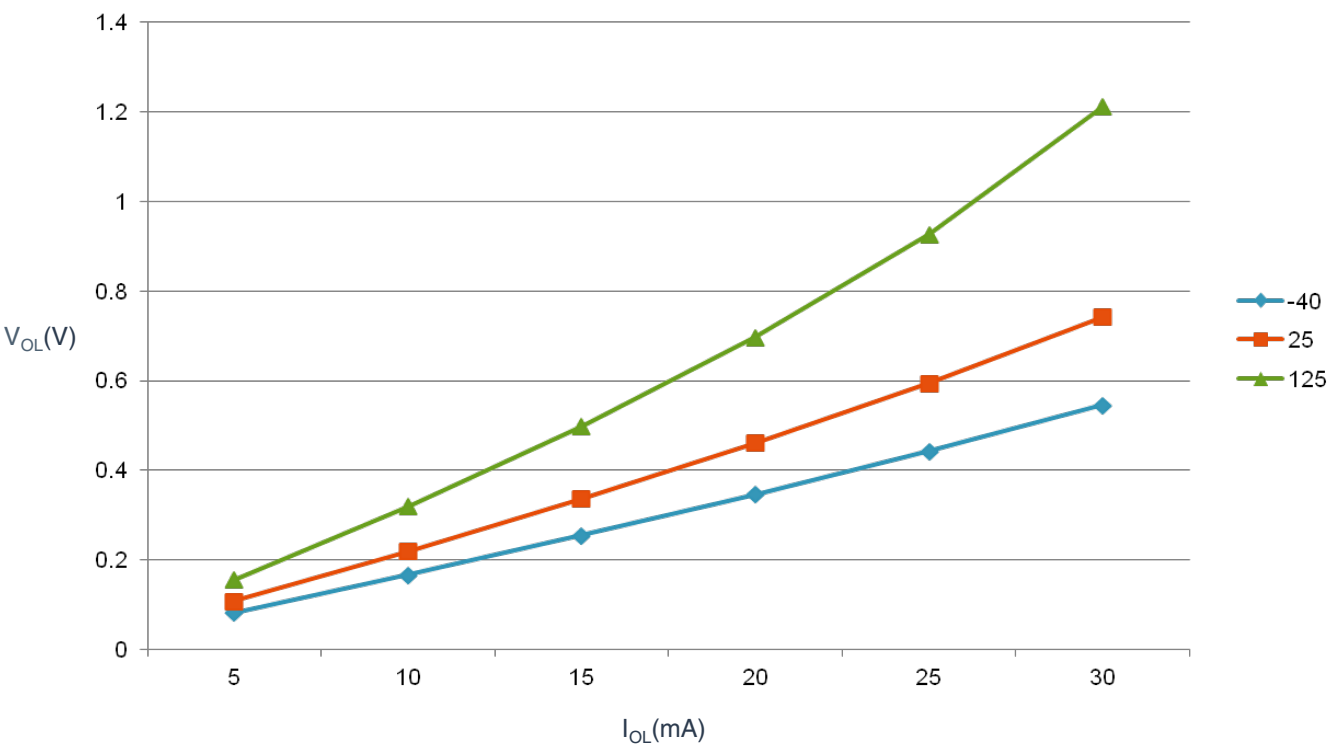


Figure 7. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 5 V)

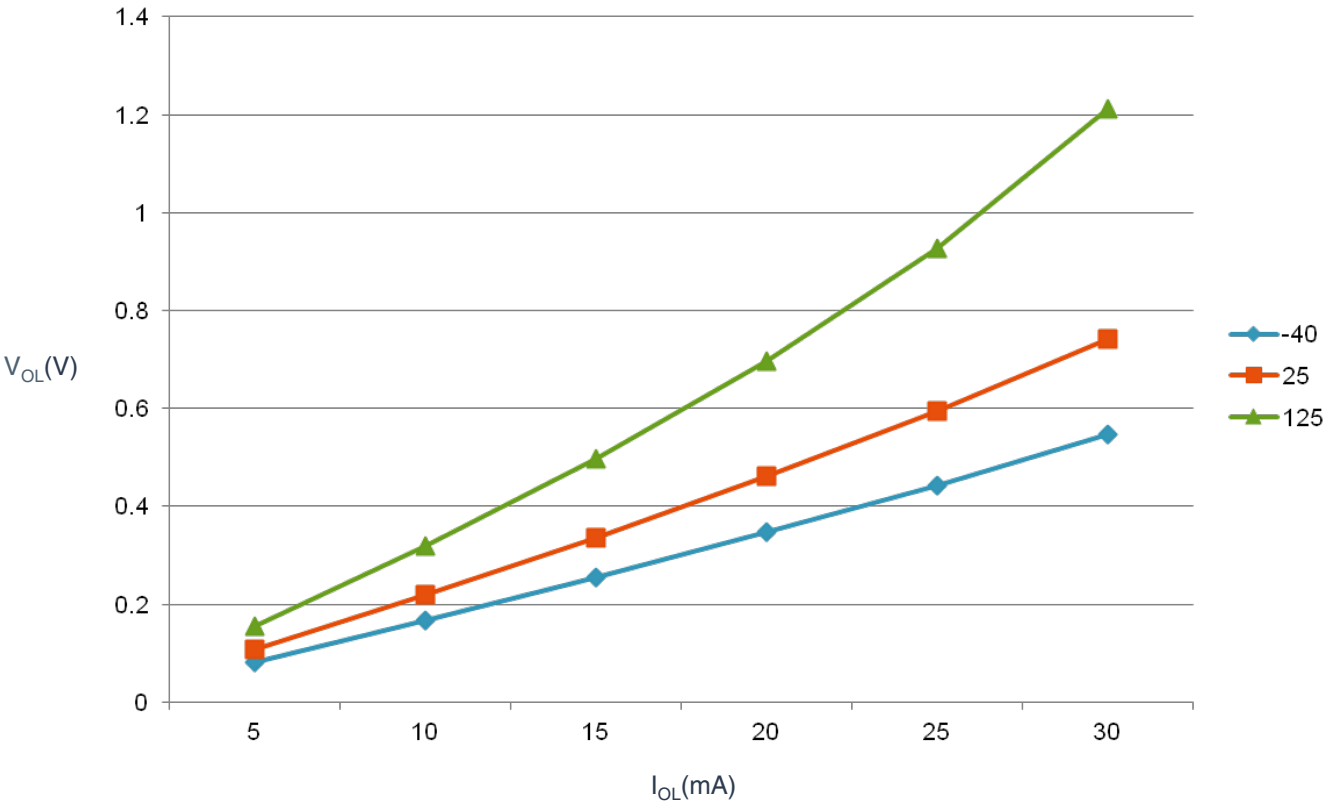


Figure 8. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 3 V)

4.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 4. Supply current characteristics

Parameter	Symbol	Bus Freq	V_{DD} (V)	Typical[1]	Max	Unit	Temp
Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	20 MHz	5	6.7	—	mA	–40 to 125 °C
		10 MHz		4.5	—		
		1 MHz		1.5	—		
		20 MHz	3	6.6	—		
		10 MHz		4.4	—		
		1 MHz		1.45	—		
Run supply current FEI mode, all modules clocks disabled; run from flash	RI_{DD}	20 MHz	5	5.3	—	mA	–40 to 125 °C
		10 MHz		3.7	—		
		1 MHz		1.5	—		
		20 MHz	3	5.3	—		
		10 MHz		3.7	—		
		1 MHz		1.4	—		

Table continues on the next page...

4.1.3 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation play a significant role in EMC performance. The system designer must consult the following NXP applications notes, available on **nxp.com** for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers
- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

4.2 Switching specifications

4.2.1 Control timing

Table 5. Control timing

Num	Rating		Symbol	Min	Typical[1]	Max	Unit
1	System and core clock		f_{Sys}	DC	—	40	MHz
2	Bus frequency (t_{cyc} = 1/f_{Bus})		f_{Bus}	DC	—	20	MHz
3	Internal low power oscillator frequency		f_{LPO}	0.67	1.0	1.25	KHz
4	External reset pulse width[2]		t_{extrst}	1.5 × t_{cyc}	—	—	ns
5	Reset low drive		t_{rstdrv}	34 × t_{cyc}	—	—	ns
6	IRQ pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
		Synchronous path[3]	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
7	Keyboard interrupt pulse width	Asynchronous path[2]	t_{ILIH}	100	—	—	ns
		Synchronous path	t_{IHIL}	1.5 × t_{cyc}	—	—	ns
8	Port rise and fall time - Normal drive strength (load = 50 pF)[4]	—	t_{Rise}	—	10.2	—	ns
			t_{Fall}	—	9.5	—	ns
	Port rise and fall time - high drive strength (load = 50 pF)[4]	—	t_{Rise}	—	5.4	—	ns
			t_{Fall}	—	4.6	—	ns

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 125 °C.

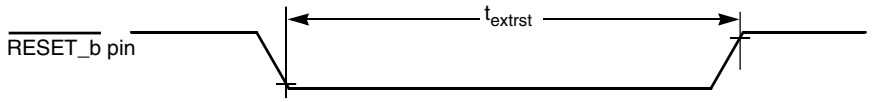


Figure 9. Reset timing

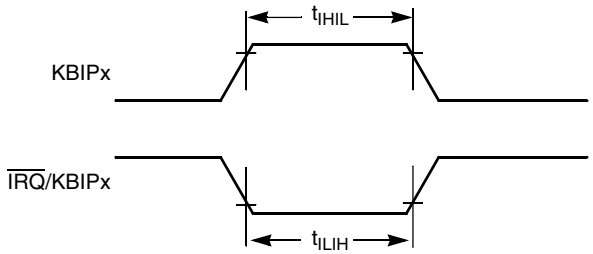


Figure 10. KBIPx timing

4.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 6. FTM input timing

Function	Symbol	Min	Max	Unit
External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
External clock period	t_{TCLK}	4	—	t_{cyc}
External clock high time	t_{clkh}	1.5	—	t_{cyc}
External clock low time	t_{clkl}	1.5	—	t_{cyc}
Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

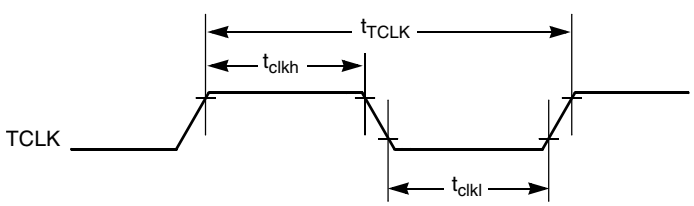


Figure 11. Timer external clock

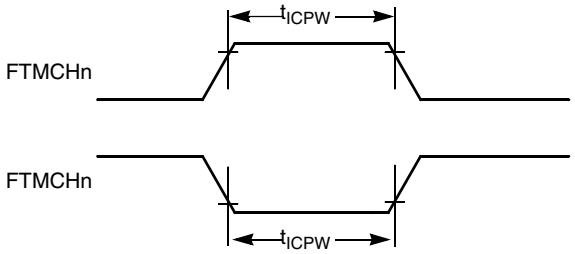


Figure 12. Timer input capture pulse

4.3 Thermal specifications

4.3.1 Thermal characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 7. Thermal attributes

Board type	Symbol	Description	64 LQFP	32 LQFP	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	86	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	57	°C/W	1, 3
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	72	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	51	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	33	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	20	24	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	5	6	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.

4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the solder pad on the bottom of the package. Interface resistance is ignored.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization.

The average chip-junction temperature (T_J) in °C can be obtained from:

$T_J = T_A + (P_D \times \theta_{JA})$

Where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts - chip internal power

$P_{I/O}$ = Power dissipation on input and output pins - user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$P_D = K \div (T_J + 273\ °C)$

Solving the equations above for K gives:

$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2$

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

5 Peripheral operating requirements and behaviors

5.1 Core modules

5.1.1 SWD electricals

Table 8. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation			

Table continues on the next page...

Table 8. SWD full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
	• Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

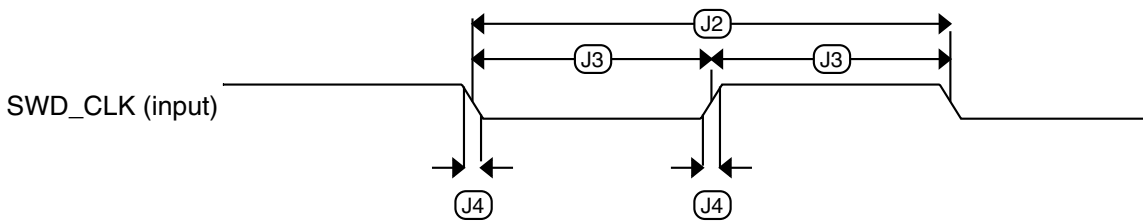


Figure 13. Serial wire clock input timing

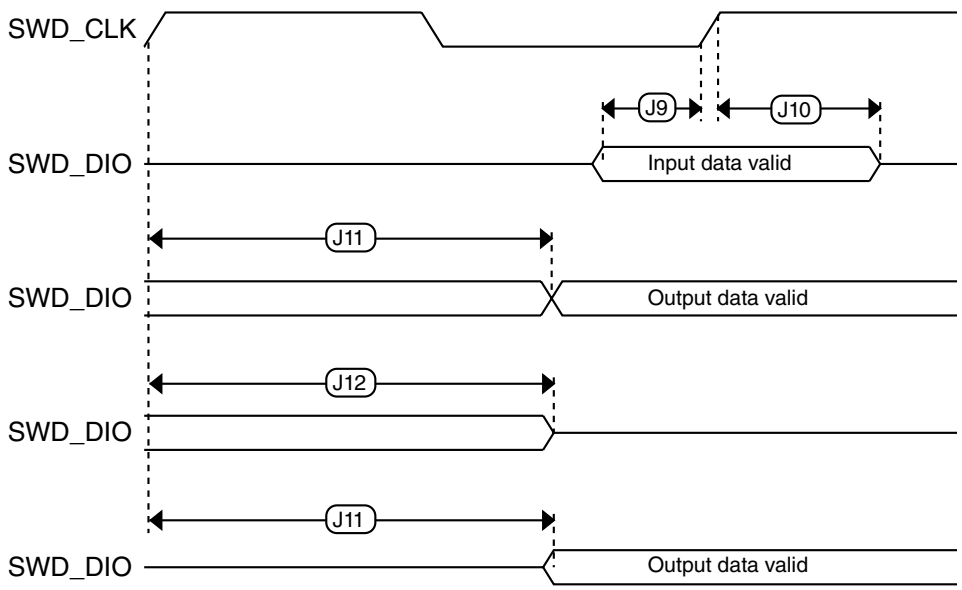


Figure 14. Serial wire data timing

5.2 External oscillator (OSC) and ICS characteristics

Table 9. OSC and ICS specifications (temperature range = -40 to 125 °C ambient)

Num	Characteristic		Symbol	Min	Typical[1]	Max	Unit
1	Crystal or resonator frequency	Low range (RANGE = 0)	f_{lo}	31.25	32.768	39.0625	kHz
		High range (RANGE = 1)	f_{hi}	4	—	20	MHz
2	Load capacitors		C1, C2	See Note[2]			
3	Feedback resistor	Low Frequency, Low-Power Mode[3]	R_F	—	—	—	MΩ
		Low Frequency, High-Gain Mode		—	10	—	MΩ
		High Frequency, Low-Power Mode		—	1	—	MΩ
		High Frequency, High-Gain Mode		—	1	—	MΩ
4	Series resistor - Low Frequency	Low-Power Mode [3]	R_S	—	0	—	kΩ
		High-Gain Mode		—	200	—	kΩ
5	Series resistor - High Frequency	Low-Power Mode[3]	R_S	—	0	—	kΩ
	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
		8 MHz		—	0	—	kΩ
		16 MHz		—	0	—	kΩ
6	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal[4,5]	Low range, low power	t_{CSTL}	—	1000	—	ms
		Low range, high gain		—	800	—	ms
		High range, low power	t_{CSTH}	—	3	—	ms
		High range, high gain		—	1.5	—	ms
7	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	Internal reference clock (IRC) frequency trim range		f_{int_t}	31.25	—	39.0625	kHz
9	Internal reference clock frequency, factory trimmed,	T = 125 °C, V_{DD} = 5 V	f_{int_ft}	—	31.25	—	kHz
10	DCO output frequency range	FLL reference = fint_t, flo, or fhi/RDIV	f_{dco}	—	—	—	MHz
11	Factory trimmed internal oscillator accuracy	T = 125 °C, V_{DD} = 5 V	Δf_{int_ft}	-0.8	—	0.8	%
12	Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 5 V	Over temperature range from -40 °C to 125°C	Δf_{int_t}	-1	—	0.8	%

Table continues on the next page...

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

5.4 Analog

5.4.1 ADC characteristics

Table 11. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDA})	ΔV_{DDA}	-100	0	+100	mV	—
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})	ΔV_{SSA}	-100	0	+100	mV	—
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	—
Input resistance		R_{ADIN}	—	3	5	kΩ	—
Analog source resistance	12-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz	R_{AS}	— —	— —	2 5	kΩ	External to MCU
	10-bit mode • f_{ADCK} > 4 MHz • f_{ADCK} < 4 MHz		— —	— —	5 10		
	8-bit mode (all valid f_{ADCK})		—	—	10		
ADC conversion clock frequency	High speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	—
	Low power (ADLPC=1)		0.4	—	4.0		

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

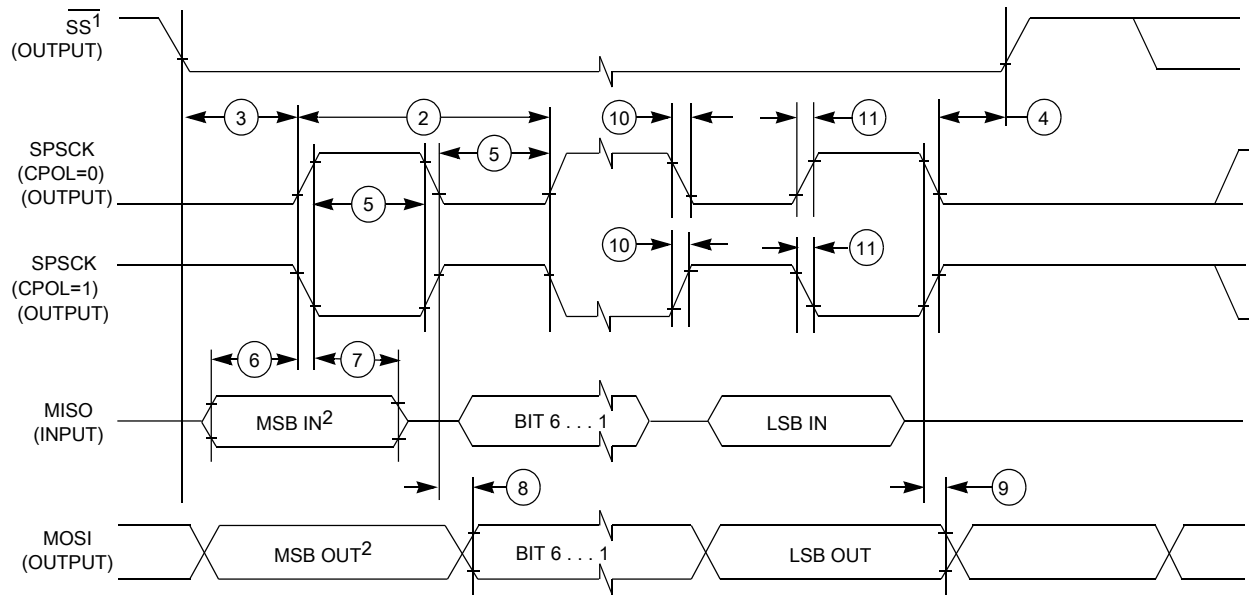
Table 12. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit
	Low power (ADLPC = 1)		1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)		—	40	—	
Sample time	Short sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)		—	23.5	—	
Total unadjusted Error[2]	12-bit mode	E_{TUE}	—	±5.0	—	LSB[3]
	10-bit mode		—	±1.5	±2.0	
	8-bit mode		—	±0.7	±1.0	
Differential Non-Liniarity	12-bit mode	DNL	—	±1.0	—	LSB[3]
	10-bit mode[4]		—	±0.25	±0.5	
	8-bit mode[4]		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode	INL	—	±1.0	—	LSB[3]
	10-bit mode		—	±0.3	±0.5	
	8-bit mode		—	±0.15	±0.25	
Zero-scale error[5]	12-bit mode	E_{ZS}	—	±2.0	—	LSB[3]
	10-bit mode		—	±0.25	±1.0	
	8-bit mode		—	±0.65	±1.0	
Full-scale error[6]	12-bit mode	E_{FS}	—	±2.5	—	LSB[3]
	10-bit mode		—	±0.5	±1.0	
	8-bit mode		—	±0.5	±1.0	
Quantization error	≤12 bit modes	E_Q	—	—	±0.5	LSB[3]
Input leakage error[7]	all modes	E_{IL}	I_{In} x R_{AS}			mV
Temp sensor slope	-40 °C–25 °C	m	—	3.266	—	mV/°C
	25 °C–125 °C		—	3.638	—	
Temp sensor voltage	25 °C	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
4. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
5. $V_{ADIN} = V_{SSA}$
6. $V_{ADIN} = V_{DDA}$
7. I_{In} = leakage current (refer to DC characteristics)

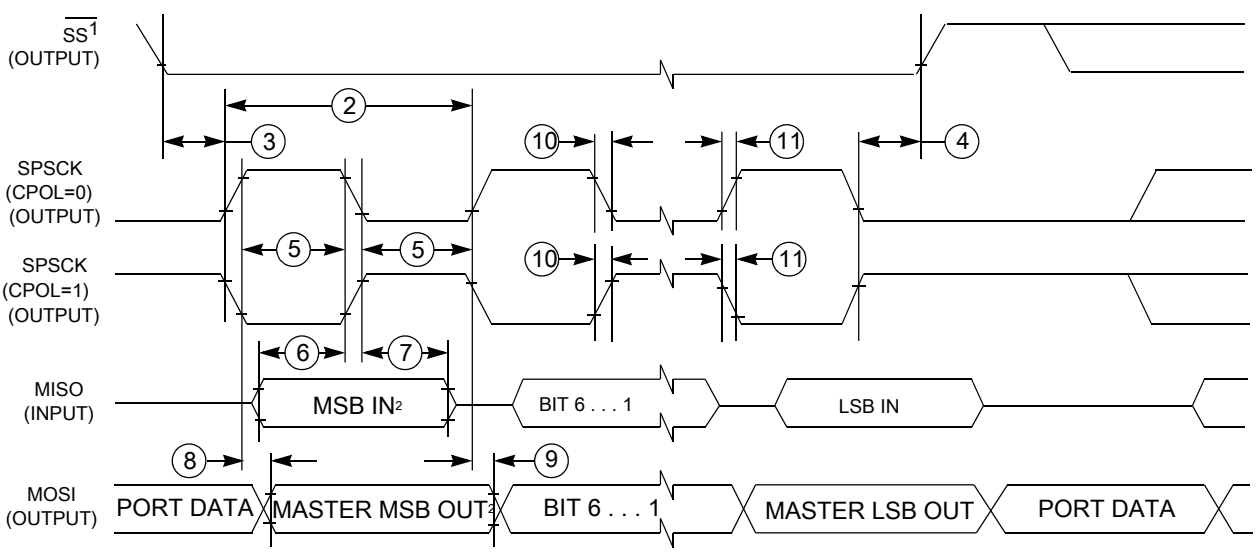
Table 14. SPI master mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Comment
10	t_{RI}	Rise time input	—	t_{Bus} – 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. SPI master mode timing (CPHA=0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. SPI master mode timing (CPHA=1)

Table 15. SPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Comment
1	f_{op}	Frequency of operation	0	$f_{Bus}/4$	Hz	f_{Bus} is the bus clock as defined in Control timing.
2	t_{SPSCK}	SPSCK period	4 x t_{Bus}	—	ns	$t_{Bus} = 1/f_{Bus}$
3	t_{Lead}	Enable lead time	1	—	t_{Bus}	—
4	t_{Lag}	Enable lag time	1	—	t_{Bus}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{Bus} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	15	—	ns	—
7	t_{HI}	Data hold time (inputs)	25	—	ns	—
8	t_a	Slave access time	—	t_{Bus}	ns	Time to data active from high-impedance state
9	t_{dis}	Slave MISO disable time	—	t_{Bus}	ns	Hold time to high-impedance state
10	t_v	Data valid (after SPSCK edge)	—	25	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{Bus} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

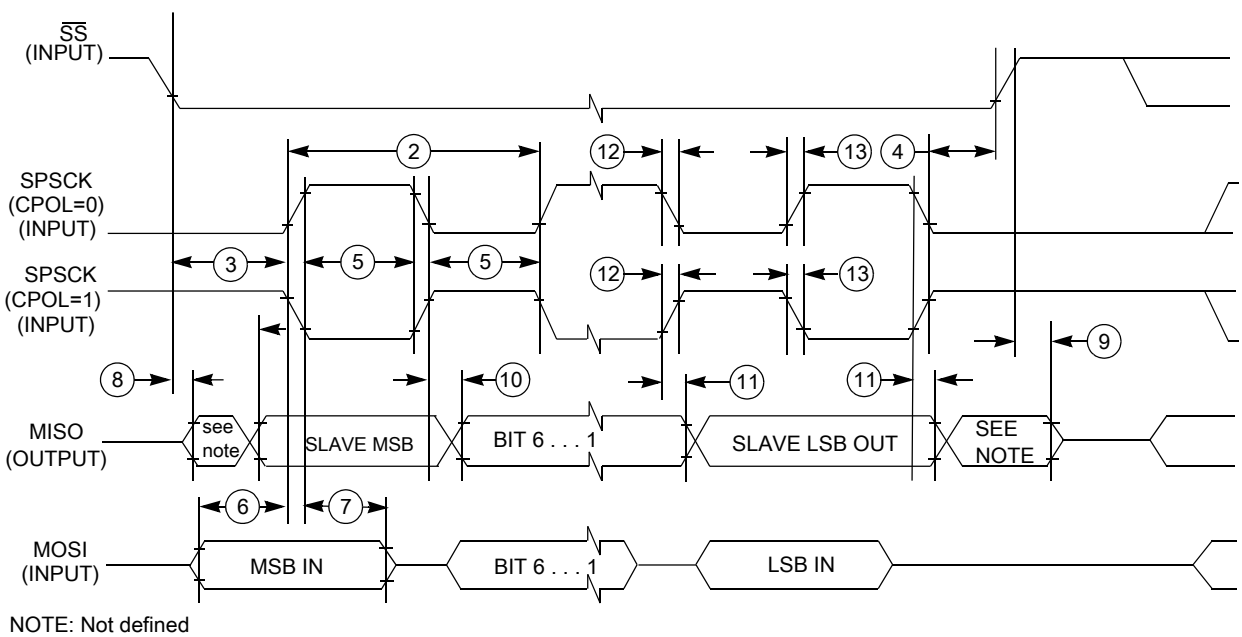


Figure 19. SPI slave mode timing (CPHA = 0)

8 Revision History

The following table provides a revision history for this document.

Table 16. Revision History

Rev. No.	Date	Substantial Changes
Rev. 1	11 March 2014	Initial Release
Rev. 2	18 June 2014	• Parameter Classification section is removed. • Classification column is removed from all the tables in the document. • Supply current characteristics section is updated.

Rev. 3	18 July 2014	• ESD handling ratings section is updated.
		• Figures in DC characteristics section are updated.
		• Specs updated in following tables:
		  • Table 9.
		  • Table 4.

Rev. 4	03 Sept 2014	• Data Sheet type changed to "Technical Data".
Rev. 5	12 May 2016	• In section: Key features, Changed the number of instances of IIC to 1.