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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Audio
Interface	I²C, I²S, SPDIF
Clock Rate	24.576MHz
Non-Volatile Memory	-
On-Chip RAM	1.375KB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	-25°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	SQFP-T52M (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/bu9408ks2

●Absolute Maximum Ratings

Items	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	4.5	V
Power dissipation	P_d	850(*1)	mW
Operating temp. range	T_{opr}	-25～+85	°C
Storage temp. range	T_{stg}	-55～+125	°C

*1Use of this processor at Ta = 25°C and over is subject to reduction of 8.5mW per 1°C.
Operation is not guaranteed.

●Recommended Operating Rating(s)

Items	Symbol	Ratings	Unit
Power supply voltage	V_{DD}	3.0～3.6	V

*1 This product is not designed for protection against radioactive rays.

●Electrical Characteristics(Digital system)

V_{DD}=3.3V (Unless otherwise specified Ta = 25°C)

Items		Symbol	Limit			Unit	Conditions	Adaptive terminal
			MIN	TYP	MAX			
Input voltage	H-level voltage	V_{IH}	2.3	-	-	V		*1
	L-level voltage	V_{IL}	-	-	1.0	V		*1
Hysteresis input voltage	H-level voltage	V_{IH}	2.5	-	-	V		*2,3,4
	L-level voltage	V_{IL}	-	-	0.8	V		*2,3,4
Input current		I_I	-1	-	+1	μA	V_{IN}=0~3.3V	*1,2
Input L current to Pull-up resistor		I_{IL}	-150	-100	-50	μA	V_{IN}=0V	*3
Input H current to Pull-down resistor		I_{IH}	35	70	105	μA	V_{IN}=3.3V	*4
Output voltage	H-level voltage	V_{OH}	2.75	-	-	V	I_O=-0.6mA	*5
	L-level voltage	V_{OL}	-	-	0.55	V	I_O=0.6mA	*5
SDA Output voltage	L-level voltage	V_{OL}	-	-	0.4	V	I_O=3mA	*6

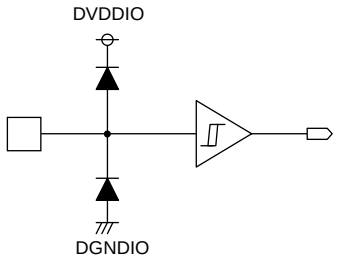
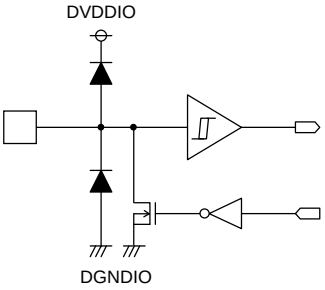
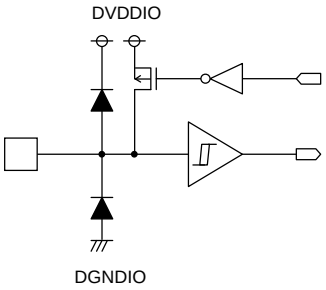
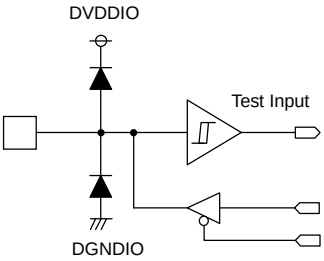
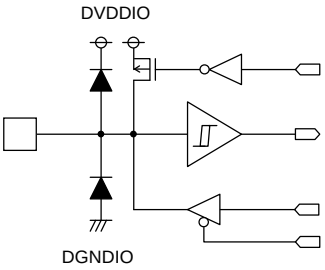
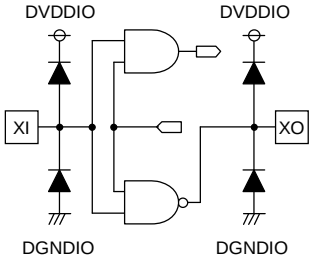
Adaptive terminal
*1 CMOS input terminal
XI(33pin)
*2 CMOS hysteresis input terminal
SCANTEST(5pin), SCL(7pin), SDA(8pin)
*3 CMOS hysteresis input terminal with a built-in pull-up resistor
LRCKI1(41pin), BCKI1(42pin), DATAI1(43pin), LRCKI2(44pin), BCKI2(45pin), DATAI2(46pin), LRCKI3(47pin), BCKI3(48pin), DATAI3(49pin), LRCKI4(50pin), BCKI4(51pin), DATAI4(52pin)
*4 CMOS input terminal with a built-in pull down resistor
I2CADR(6pin), RESETB(10pin), MUTE1B(12pin), MUTE2B(13pin), MUTE3B(14pin)
*5 CMOS output terminal
ERR1_LRC(24pin), ERR2_BCK(25pin), DATASO(26pin), DATAMO(27pin), BCKO(28pin), LRCKO(29pin), AMCLKO(30pin), SPDIFO(31pin), XO(34pin),
*6 Open drain output terminal
SDA(8pin)

●Electrical Characteristics (Analog system)

V_{DD}=3.3V (Unless otherwise specified Ta = 25°C, R_L=10kΩ, standard V_C)

Item	Symbol	Limit			Unit	Applicable pins, conditions
		MIN	TYP	MAX		
Total						
Circuit current	I_Q	-	40	70	mA	DVDDIO,DVDDPLL,AVDDDA1, AVDDDA2
Regulator						
Output voltage	V_{REG}	1.3	1.5	1.7	V	I_O=100mA
PLLA						
Lock frequency	f_{PA8}	-	24.576	-	MHz	BCK=3.072MHz (fs=48kHz)
Audio DAC						
Max-output amplitude	V_{OMAX}	0.63	0.75	0.86	Vrms	
THD+N	THD_{DA}	-	0.005	0.03	%	0dB,1kHz
S/N	S/N_{DA}	-	96	-	dB	0dB,1kHz,A-weighted
16bitDAC						
Max-output amplitude	V_{OMAX}	0.65	0.77	0.88	Vrms	
THD+N	THD_{DA}	-	0.03	-	%	0dB,1kHz
S/N	S/N_{DA}	-	90	-	dB	0dB,1kHz,A-weighted

●Terminal equal circuit figure

A	B	C
		
D	**E**	**F**
		
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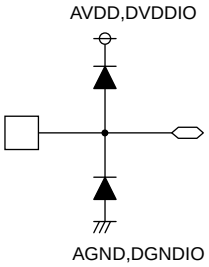
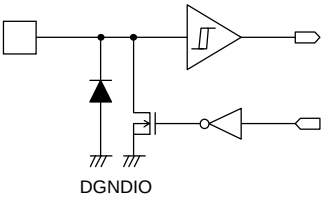
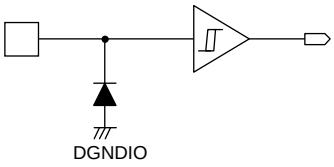
		

2-12. System Clock Selecting of DF1＋ΔΣDAC (Dotted line ③)

Default = 0

Select Address	Value	Operation Description
&h0A [1:0]	0	The 24.576MHz (512fs) system clock from the XI terminal
	1	The clock of 512fs made from PLL1 of the S-P conversion 1
	2	The clock of 512fs made from PLL2 of the S-P conversion 2

2-13. System Clock Selecting DF2＋16bit DAC (Dotted line ④)

Default = 0

Select Address	Value	Operation Description
&h0A [5:4]	0	The 24.576MHz (512fs) system clock from the XI terminal
	1	The clock of 512fs made from PLL1 of the S-P conversion 1
	2	The clock of 512fs made from PLL2 of the S-P conversion 2

When using DATASO as an asynchronous output to DATAMO, it sets up system clock selecting of the P-S conversion 2 by this command. (Dotted line ⑤)

3-1. Bit Clock Frequency Configuration for 3-line Serial Input

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h0B [4]	0	64fs format
S-P Conversion 2 &h0C [4]	1	48fs format

3-2. Format Configuration for 3-line Serial Input

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h0B [3:2]	0	IIS format
S-P Conversion 2 &h0C [3:2]	1	Left-justified format
	2	Right-justified format

3-3. Data Bit Width Configuration for 3-line Serial Input

Default = 0

Select Address	Value	Operation Description
S-P Conversion 1 &h0B [1:0]	0	16 bit
S-P Conversion 2 &h0C [1:0]	1	20 bit
	2	24 bit

Setting of K

P2V_K sets the slop of D range. It sets the P2V_MAX = “1Eh” (-30dB) and represents the output level V_{Omax} at the time of input level V_I = 0dB.

Default = 00h

Select Address	Operational explanation
&h36 [3:0]	

command	gain	comman	gain
0	−30dB	8	−14dB
1	−28dB	9	−12dB
2	−26dB	A	−10dB
3	−24dB	B	−8dB
4	−22dB	C	−6dB
5	−20dB	D	−4dB
6	−18dB	E	−2dB
7	−16dB	F	0dB

Setting of α

P2V_OFS makes small voice easy to be heard because the whole output level is lifted.

Default = 00h

Select Address	Operational explanation
&h37 [4:0]	

command	gain	command	gain	command	gain	command	gain
00	0dB	08	+8dB	10	+16dB	18	+24dB
01	+1dB	09	+9dB	11	+17dB	19	−
02	+2dB	0A	+10dB	12	+18dB	1A	−
03	+3dB	0B	+11dB	13	+19dB	1B	−
04	+4dB	0C	+12dB	14	+20dB	1C	−
05	+5dB	0D	+13dB	15	+21dB	1D	−
06	+6dB	0E	+14dB	16	+22dB	1E	−
07	+7dB	0F	+15dB	17	+23dB	1F	−

Setting 1 of transition time at the time of attack

A_RATE is the setting of transition time when the state of P^2Volume function is transited to (2)→(3).

Default = 0

Select Address	Operational explanation
&h38 [6:4]	

command	A_RATE time	command	A_RATE time
0	1ms	4	5ms
1	2ms	5	10ms
2	3ms	6	20ms
3	4ms	7	40ms

Setting 1 of transition time at the time of recovery

R_RATE is the setting of transition time when the state of P^2Volume function is transited to (3)→(2).

Default = 0h

Select Address	Operational explanation
&h38 [3:0]	

command	R_RATE time	command	R_RATE time
0	0.25s	8	3s
1	0.5s	9	4s
2	0.75s	A	5s
3	1s	B	6s
4	1.25s	C	7s
5	1.5s	D	8s
6	2s	E	9s
7	2.5s	F	10s

Selection of frequency (F_0)

Default = 0Eh

Select Address	Operational explanation

&h45 [5:0]

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	–
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	–
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	–

Selection of quality factor (Q)

Default = 4h

Select Address	Operational explanation

&h46 [3:0]

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address	Operational explanation

&h47 [6:0]

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

Setting of the Start of transmitting to coefficient RAM

In the case of using the smooth transition, it is transmitted to the coefficient RAM for smooth transition. In the case of not using of the smooth transition, it is transmitted to the direct coefficient RAM.

Default = 0

Select Address	Value	Operational explanation
&h48 [0]	0	TREBLE coefficient transmission stop
	1	TREBLE coefficient transmission start

Selection of frequency (F_0)

Default = 0Eh

Select Address	Operational explanation
&h49 [5:0]	

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	−
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	−
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	−

Selection of quality factor (Q)

Default = 4h

Select Address	Operational explanation
&h4A [3:0]	

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address	Operational explanation
&h4B [6:0]	

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

Setting of P^{2}Bass deep bass gain

Default = 00h

Select Address	Operational explanation
&h74 [7:4]	

Command	Gain	Command	Gain
0	0dB	8	+8dB
1	+1dB	9	+9dB
2	+2dB	A	+10dB
3	+3dB	B	+11dB
4	+4dB	C	+12dB
5	+5dB	D	+13dB
6	+6dB	E	+14dB
7	+7dB	F	+15dB

Setting of P^{2}Bass HPF cutoff frequency

Default = 0

Select Address	Value	Operational explanation
&h74 [3:2]	0	60Hz
	1	80Hz
	2	100Hz
	3	120Hz

Setting of P^{2}Bass LPF cutoff frequency

Default = 0

Select Address	Value	Operational explanation
&h74 [1:0]	0	120Hz
	1	160Hz
	2	200Hz
	3	240Hz

ON/OFF of pseudo bass function

It can contribute to bass emphasis effect caused by pseudo bass. And it can also be used independently.

Default = 0

Select Address	Value	Operational explanation
&h72 [7]	0	Not using of pseudo bass function
	1	Using of pseudo bass function

Setting of pseudo bass gain

Default = 00h

Select Address	Operational explanation
&h72 [6:4]	

Command	Gain	Command	Gain
0	−4dB	4	+4dB
1	−2dB	5	+6dB
2	0dB	6	+8dB
3	+2dB	7	+10dB

Selection of frequency (F_0)

Default = 0Eh

Select Address	Operational explanation
bit [5:0] It sets to all band	

Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency	Command	Frequency
00	20Hz	08	50Hz	10	125Hz	18	315Hz	20	800Hz	28	2kHz	30	5kHz	38	12.5kHz
01	22Hz	09	56Hz	11	140Hz	19	350Hz	21	900Hz	29	2.2kHz	31	5.6kHz	39	14kHz
02	25Hz	0A	63Hz	12	160Hz	1A	400Hz	22	1kHz	2A	2.5kHz	32	6.3kHz	3A	16kHz
03	28Hz	0B	70Hz	13	180Hz	1B	450Hz	23	1.1kHz	2B	2.8kHz	33	7kHz	3B	18kHz
04	32Hz	0C	80Hz	14	200Hz	1C	500Hz	24	1.25kHz	2C	3.15kHz	34	8kHz	3C	20kHz
05	35Hz	0D	90Hz	15	220Hz	1D	560Hz	25	1.4kHz	2D	3.5kHz	35	9kHz	3D	–
06	40Hz	0E	100Hz	16	250Hz	1E	630Hz	26	1.6kHz	2E	4kHz	36	10kHz	3E	–
07	45Hz	0F	110Hz	17	280Hz	1F	700Hz	27	1.8kHz	2F	4.5kHz	37	11kHz	3F	–

Selection of quality factor (Q)

Default = 4h

Select Address	Operational explanation
bit [3:0] It sets to every band	

Command	Quality factor	Command	Quality factor
0	0.33	8	2.2
1	0.43	9	2.7
2	0.56	A	3.3
3	0.75	B	3.9
4	1.0	C	4.7
5	1.2	D	5.6
6	1.5	E	6.8
7	1.8	F	8.2

Selection of Gain

Default = 40h

Select Address	Operational explanation
bit [6:0] It sets to every band	

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

The Select Address of each band is shown in the table below:

	Band1	Band2	Band3	Band4	Band5	Band6	Band7
Selection of filter type bit [7:6] Setting of the Start of transmitting to coefficient RAM bit [0]	&h50h	&h54h	&h58h	&h5Ch	&h60h	&h64h	&h68h
F(frequency) selection bit [5:0]	&h51h	&h55h	&h59h	&h5Dh	&h61h	&h65h	&h69h
Q(Quality Factor) selection bit [3:0]	&h52h	&h56h	&h5Ah	&h5Eh	&h62h	&h66h	&h6Ah
Gain selection bit [6:0]	&h53h	&h57h	&h5Bh	&h5Fh	&h63h	&h67h	&h6Bh

4-20. Sub output channel mixer

Mixing setting of sound of the left channel and the right channel of the digital signal for sub output which is input into sound DSP is done. The monaural conversion of the stereo signal is done here.

The data which is input into Lch of Sub output signal processing is mixed.

Default = 0

Select Address	Value	Operating explanation
&h22 [3:2]	0	Inputting the Lch data
	1	Inputting the data of (Lch + Rch) / 2
	2	Inputting the data of (Lch + Rch) / 2
	3	Inputting the Rch data

The data which is input into Rch of Sub output signal processing is mixed.

Default = 0

Select Address	Value	Operating explanation
&h22 [1:0]	0	Inputting the Rch data
	1	Inputting the data of （Lch + Rch） / 2
	2	Inputting the data of （Lch + Rch） / 2
	3	Inputting the Lch data

4-21. LPF for sub woofer output

It is the crossover filter (LPF) for sub woofer output.
LPF function ON/OFF.

Default = 0

Select Address	Value	Operating explanation
&h7A [7]	0	LPF function is not used
	1	LPF function is used

Setting of the cut off frequency (Fc) of LPF

Default = 0h

Select Address	Operating explanation
&h7A [6:4]	

Command	Fc	Command	Fc
0	60Hz	4	160Hz
1	80Hz	5	200Hz
2	100Hz	6	240Hz
3	120Hz	7	280Hz

Selection of Gain

Default = 40h

Select Address	Operating explanation
bit [6:0] It sets to all band	

Command	Gain
1C	−18dB
⋮	⋮
3E	−1dB
3F	−0.5dB
40	0dB
41	+0.5dB
42	+1dB
⋮	⋮
64	+18dB

If the coefficient of b0, b1, b2, a1, and a2 exceeds ±4, it may not operate normally.

Select Address of every band is as in chart below

	Band1	Band2	Band3
Selection of filter type bit [7:6]	&h80h	&h84h	&h88h
Transfer start setting to coefficient RAM bit [0]			
F (frequency) selection bit [5:0]	&h81h	&h85h	&h89h
Q (quality factor) selection bit [3:0]	&h82h	&h86h	&h8Ah
Gain selection bit [6:0]	&h83h	&h87h	&h8Bh

4-23. Sub output EVR (electronic volume)

The volume for sub output can select with 0.5dB step from +24dB to -103dB.
When changing volume, smooth transition is done.
The expression in the transition time from x[dB] to y[dB] is |(10^(x/20)-10^(y/20)|*21.4ms (Sub output balance Lch=Rch=0dB).
The transition time is 21.4ms when it is from 0dB to -∞. Recommend that this setting value is 0dB and under.

Volume setting

Default = FFh

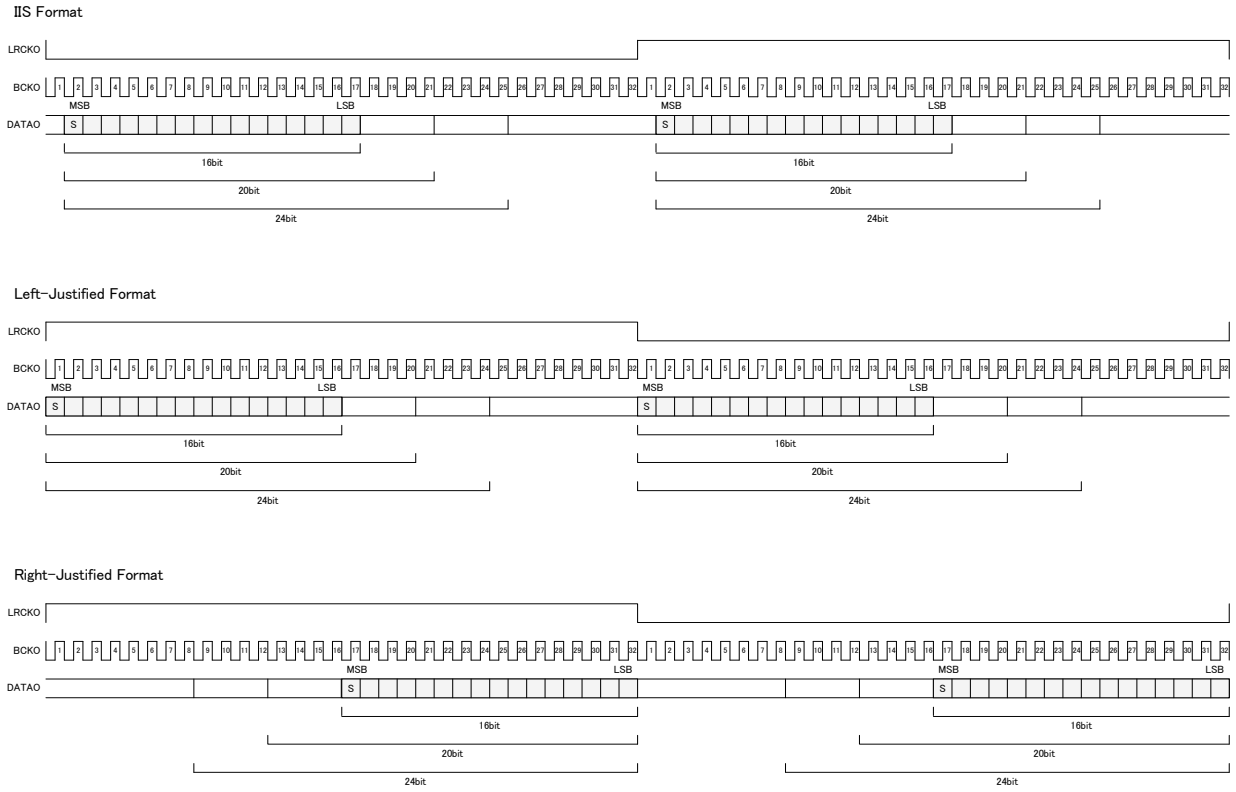
Select Address	Operating explanation
&h2C [7:0]	

Command	Gain
00	+24dB
01	+23.5dB
⋮	⋮
30	0dB
31	−0.5dB
32	−1dB
⋮	⋮
FE	−103dB
FF	−∞

5. P-S Conversion 1 and P-S Conversion 2

BU9408KS2 has two built-in parallel-serial conversion circuits (P-S Conversion 1 and P-S Conversion 2). P-S conversion 1 converts the output from the ASRC or DSP (Main/Sub) output to 3-line serial data before sending it from DATAMO, BCKO and LRCKO (pins 27, 28 and 29). (Refer to &h04 [1:0])
P-S conversion 2 converts the ASRC or DSP (Main/Sub) output or DF1 output into 3-line serial data before transmitting it from DATASO, BCKO and LRCKO (pins 26, 28 and 29). Moreover, it is also possible to output the synchronous clock for serial transfer from ERR1_LRC and an ERR2_BCK terminal by an output option (Refer to &h04 [5:4]).

The three output formats are IIS, left-justified and right-justified. 16bit, 20bit and 24bit output can be selected for each format.
The timing charts for each transfer format are as follows:



5-1. 3-line Serial Output Format Configuration

Default = 0

Select Address	Value	Operation Description
P-S Conversion 1 &h0D [3:2]	0	IIS format
P-S Conversion 2 &h0E [3:2]	1	Left-justified format
	2	Right-justified format

5-2. 3-line Serial Output Data Bit Width Configuration

Default = 0

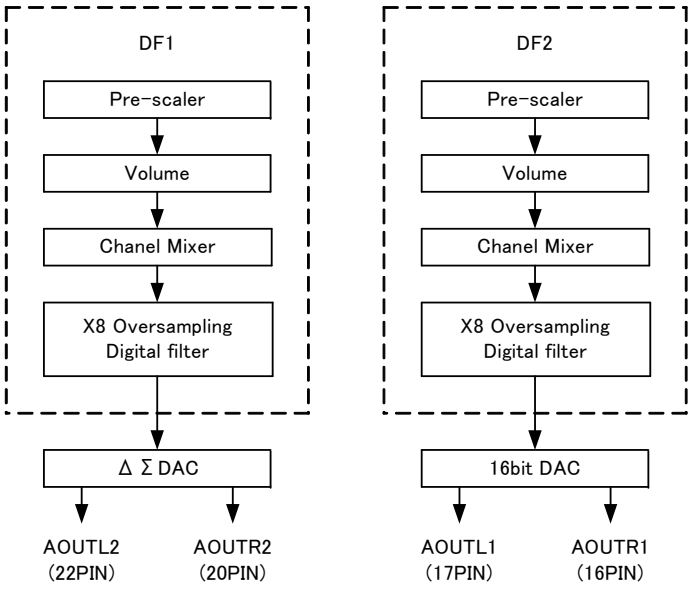
Select Address	Value	Operation Description
P-S Conversion 1 &h0D [1:0]	0	16 bit
P-S Conversion 2 &h0E [1:0]	1	20 bit
	2	24 bit

6. 8x Over-Sampling Digital Filter (DF)

In each BU9408KS2 audio analog signal output DAC, an 8x over-sampling digital filter is inserted into the previous step of the DAC input.

In addition to filter calculations, this block also performs pre-scaler, volume and Lch/Rch mix functions.

BU9408KS2's DF+DAC configurations are as follows:



6-1. Pre-Scaler Function (Attenuation)

The signal levels are adjusted in order to bring out the audio DAC performance.

For DF1, refer to &h90[7:0] and &h91[7:0]. The default value is h4000.

For DF1, refer to &h93[7:0] and &h94[7:0]. The default value is h4000.

6-2. Volume Function

The volume value can be configured in 0.5dB increments from +6dB to -121dB.
To change the volume value, coefficient soft transition takes place.
The expression in the transition time from x[dB] to y[dB] is |(10^(x/20)-10^(y/20)|*21.4ms. The transition time is 21.4ms when it is from 0dB to -∞. Recommend that this setting value is 0dB and under.

Default = FFh

Select Address	Operation Description
DF1 &h92 [7:0] DF2 &h95 [7:0]	

Command Value	Gain
00	+6dB
01	+5.5dB
⋮	⋮
0C	0dB
0D	−0.5dB
0E	−1dB
⋮	⋮
FE	−121dB
FF	−∞

Calculation format: (12-command value) x 0.5dB

7. Mute Function by MUTE1B, MUTE2B and MUTE3B Terminal

BU9408KS2 has a mute function by an external terminal.
It's possible to mute DSP's main and sub digital output by MUTE1B (12pin) terminal to “L”.
It's possible to mute DF1+ΔΣDAC output by MUTE2B (13pin) terminal to “L”.
It's possible to mute DF2＋16bit DAC output by MUTE3B (14pin) terminal to “L”.

Soft mute transition time setup of a MUTE1B terminal (12PIN)

Mute the Main and Sub output of DSP.
Select the transition time of entering from 0dB to mute state.

Default = 0

Select Address	Value	Operating Description
&h10 [1:0]	0	21.4ms (Release mute time is 21.4ms.)
	1	10.7ms (Release mute time is 10.7ms.)
	2	5.4ms (Release mute time is 10.7ms.)
	3	2.7ms (Release mute time is 10.7ms.)

Soft mute transition time setup of a MUTE2B terminal (13PIN)

Mute the AOUTL2(22PIN) and AOUTR2(20PIN) output of DF1+ΔΣDAC.
Select the transition time of entering from 0dB to mute state.

Default = 0

Select Address	Value	Operating Description
&h10 [3:2]	0	21.4ms (Release mute time is 21.4ms.)
	1	10.7ms (Release mute time is 10.7ms.)
	2	5.4ms (Release mute time is 10.7ms.)
	3	2.7ms (Release mute time is 10.7ms.)

Soft mute transition time setup of a MUTE3B terminal (14PIN)

Mute the AOUTL1(17PIN) and AOUTR1(16PIN) output of DF2+16bit DAC.
Select the transition time of entering from 0dB to mute state.

Default = 0

Select Address	Value	Operating Description
&h10 [5:4]	0	21.4ms (Release mute time is 21.4ms.)
	1	10.7ms (Release mute time is 10.7ms.)
	2	5.4ms (Release mute time is 10.7ms.)
	3	2.7ms (Release mute time is 10.7ms.)

8. Commands Transmitted after Reset Release

The following commands must be transmitted after reset release, including after power supply stand-up.

0. Turn power on.
↓
○Wait approximately 1ms until oscillation is stable. (The time to stabilization should be adjusted according to the pendulum product.)
↓
1. Reset release (RESETB = “H”), Mute release (MUTE1B,MUTE2B,MUTE3B = “H”)
↓
○Wait approximately 500us until RAM initialization is complete.
↓
2. &hF1[2] = 0 : Signals from the analog block are connected to the digital block.
↓
3. &hF3[1] = 0 : CLK100M for a down sample block of ASRC is set as a normal mode. (&hF3 = 00h）
↓
4. &hB0[5:4] = 0 : Configure PLL clock to regular use state. (&hB0 = 02）
↓
5. &hB1[7:0] = AAh : The phase of the clock outputted from PLL is adjusted.
↓
6. &h03[5:4][1:0] = 0 : Select input at SP1 and SP2.
↓
7. &h18[7] = 0 : Set 1 when use SPDIF. (Needless set when not use SPDIF.)
↓
8. &hA0 = A6h : Configure PLLA1.
&hA1 = A0h
&hA2 = A4h
&hA3 = A4h
&hA4 = 00h
&hA7 = 40h
↓
9. &hA8 = A6h : Configure PLLA2.
&hA9 = A0h
&hAA = A4h
&hAB = A4h
&hAC = 00h
&hAF = 40h
↓
○Wait approximately 20ms until PLL is stable.
↓
10. &h01[7:6] = 0 : The data clear of built-in RAM is completed and it changes into the condition that RAM can be used.
↓
11. &h08[4][0] = 0 : Configure system clock..
↓
12. &h14 = C0h : The data clear of ASRC is completed and it changes into normal condition.
&h14 = 40h
&h14 = 01h
↓
13. Configuration of other registers.
&h26[7:0] = **h : Mute release of Main data output volume （30h = 0dB）
&h2C[7:0] = **h : Mute release of Sub data output volume (30h = 0dB)
&h92[7:0] = **h : Mute release of DF1+ΔΣDAC output volume （0Ch = 0dB）
&h95[7:0] = **h : Mute release of DF2+16bitDACoutput volume （0Ch = 0dB）

10. Notes at the Time of Reset

Since the state of IC is not decided, please make it into RESETB=L at the time of a power supply injection, and surely apply reset.

Reset of BU9408KS2 is performing noise removal by MCLK.

Therefore, in order to apply reset, a MCLK clock pulse is required of the state of RESETB=L more than 10 times.

The power-on reset after a power supply injection, and when you usually apply reset at the time of operation, please be sure to carry out in the state where the clock is inputted, from MCLK.

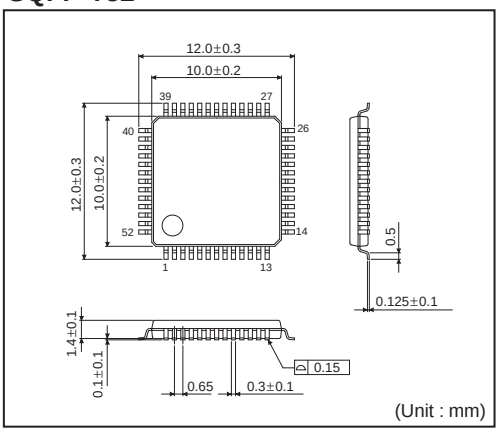
●Ordering Information

B U 9 4 0 8 K S 2	E2

- Part Number
- Package
  KS2: SQFP-T52
- Packaging and forming specification
  None: Tray, Tube

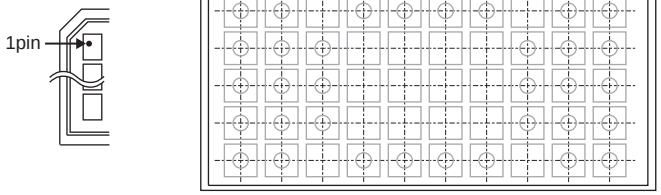
●Physical Dimension Tape and Reel Information

SQFP-T52



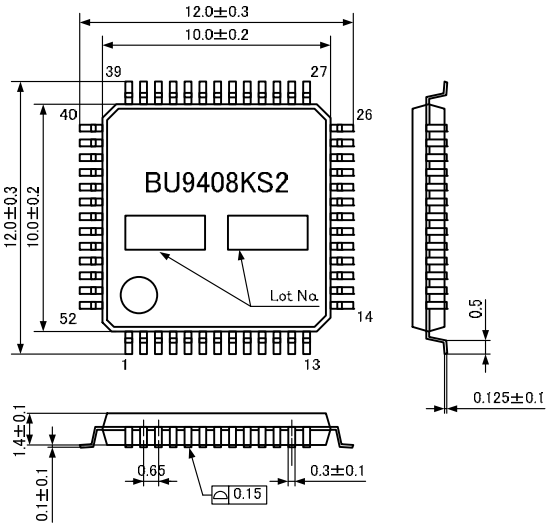
<Tape and Reel information>

Container	Tray (with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram(s)(TOP VIEW)



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1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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