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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	33MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21061ks-133

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REVISION HISTORY

5/13—Rev C to Rev D

Updated Development Tools 7

Added Related Signal Chains 8

Removed the ADSP-21061LAS-176, ADSP-21061LKS-160, and ADSP-21061LKS-176 models from Ordering Guide 52

GENERAL NOTE

This data sheet represents production released specifications for the ADSP-21061 (5 V) and ADSP-21061L (3.3 V) processors for 33 MHz, 40 MHz, 44 MHz, and 50 MHz speed grades. The product name“ADSP-21061” is used throughout this data sheet to represent all devices, except where expressly noted.

Six channels of DMA are available on the ADSP-21061—four via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21061s, memory or I/O transfers). Programs can be downloaded to the ADSP-21061 using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA request/grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Serial Ports

The ADSP-21061 features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of up to 50 Mbps. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports offers TDM multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and key mask features to enhance interprocessor communication.

Multiprocessing

The ADSP-21061 offers powerful features tailored to multiprocessor DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-21061's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21061s and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 500 Mbps over the external port. Broadcast writes allow simultaneous transmission of data to all ADSP-21061s and can be used to implement reflective semaphores.

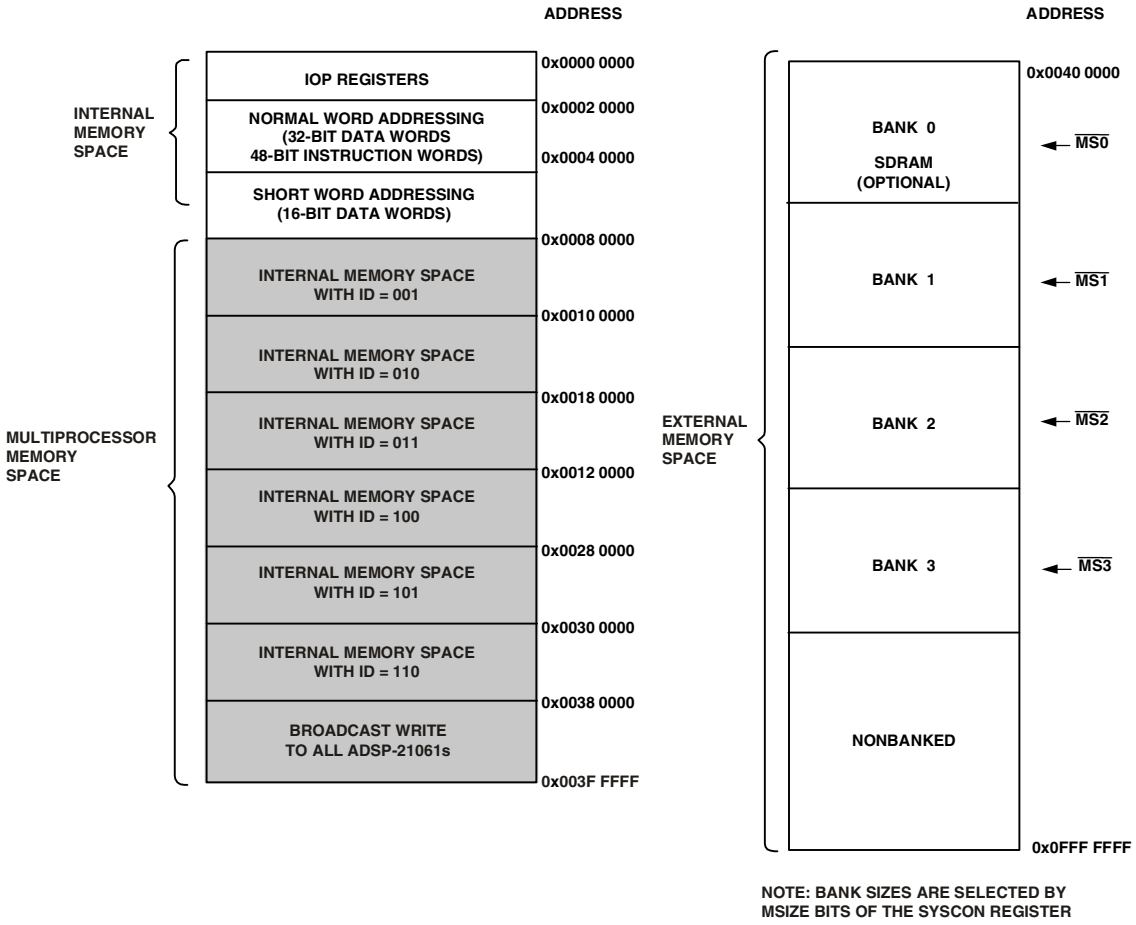

Figure 4. Memory Map

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21061 architecture and functionality. For detailed information on the ADSP-21000 Family core architecture and instruction set, refer to the *ADSP- 2106x SHARC User's Manual.*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
ACK	I/O/S	**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21061 deasserts ACK as an output to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave ADSP-21061 deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-21061 attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor halts and the memory access is not complete until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21061 deadlock, or used with a DRAM controller.
$\overline{\text{IRQ}}_{2-0}$	I/A	**Interrupt Request Lines.** May be either edge-triggered or level-sensitive.
FLAG_{3-0}	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or output. As an input, they can be tested as a condition. As an output, they can be used to signal external peripherals.
TIMEXP	O	**Timer Expired.** Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{\text{HBR}}$	I/A	**Host Bus Request.** This pin must be asserted by a host processor to request control of the ADSP-21061's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-21061 that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-21061 places the address, data, select, and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all ADSP-21061 bus requests $\overline{\text{BR}}_{6-1}$ in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	**Host Bus Grant.** Acknowledges a bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the ADSP-21061 until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-21061 bus master and is monitored by all others.
$\overline{\text{CS}}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21061.
REDY	O (O/D)	**Host Bus Acknowledge.** The ADSP-21061 deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. This pin is an open-drain output (O/D) by default; it can be programmed in the ADREDY bit of the SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{DMAR}}_{2-1}$	I/A	**DMA Request 1** (DMA Channel 7) and **DMA Request 2** (DMA Channel 6).
$\overline{\text{DMAG}}_{2-1}$	O/T	**DMA Grant 1** (DMA Channel 7) and **DMA Grant 2** (DMA Channel 6).
$\overline{\text{BR}}_{6-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21061 processors to arbitrate for bus mastership. An ADSP-21061 only drives its own $\overline{\text{BR}}$x line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21061s, the unused $\overline{\text{BR}}$x pins should be pulled high; the processor's own $\overline{\text{BR}}$x line must not be pulled high or low because it is an output.
$\overline{\text{ID2–0}}$	O (O/D)	**Multiprocessing ID.** Determines which multiprocessing bus request ($\overline{\text{BR1}}$– $\overline{\text{BR6}}$) is used by ADSP-21061. ID = 001 corresponds to $\overline{\text{BR1}}$, ID = 010 corresponds to $\overline{\text{BR2}}$, etc., ID = 000 in single-processor systems. These lines are a system configuration selection which should be hardwired or changed at reset only.
RPBA	I/S	**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-21061. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-21061.
$\overline{\text{CPA}}$	I/O (O/D)	**Core Priority Access.** Asserting its $\overline{\text{CPA}}$ pin allows the core processor of an ADSP-21061 bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{CPA}}$ is an open-drain output that is connected to all ADSP-21061s in the system. The $\overline{\text{CPA}}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, the $\overline{\text{CPA}}$ pin should be left unconnected.
DTx	O	**Data Transmit (Serial Ports 0, 1).** Each DT pin has a 50 kΩ internal pull-up resistor.
DRx	I	**Data Receive (Serial Ports 0, 1).** Each DR pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock (Serial Ports 0, 1).** Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock (Serial Ports 0, 1).** Each RCLK pin has a 50 kΩ internal pull-up resistor.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
TFSx	I/O	**Transmit Frame Sync (Serial Ports 0, 1).**
RFSx	I/O	**Receive Frame Sync (Serial Ports 0, 1).**
EBOOT	I	**EPROM Boot Select.** When EBOOT is high, the ADSP-21061 is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{\text{BMS}}$ inputs determine booting mode. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot.** Must be tied to GND.
$\overline{\text{BMS}}$	I/O/T*	**Boot Memory Select.** *Output*: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that ADSP-21061 will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). *EBOOT* *LBOOT* *$\overline{\text{BMS}}$* *Booting Mode* 1 0 Output EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.) 0 0 1(Input) Host Processor. 0 0 0 (Input) No Booting. Processor executes from external memory.
CLKIN	I	**Clock In.** External clock input to the ADSP-21061. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the minimum specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-21061 to a known state and begins program execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21061. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O	**Emulation Status.** Must be connected to the ADSP-21061 EZ-ICE target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
ICSA	O	**Reserved.** Leave unconnected.
VDD	P	**Power Supply**. (30 pins). See Operating Conditions (5 V) and Operating Conditions (3.3 V).
GND	G	**Power Supply Return.** (30 pins)
NC		**Do Not Connect.** Reserved pins which must be left open and unconnected.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

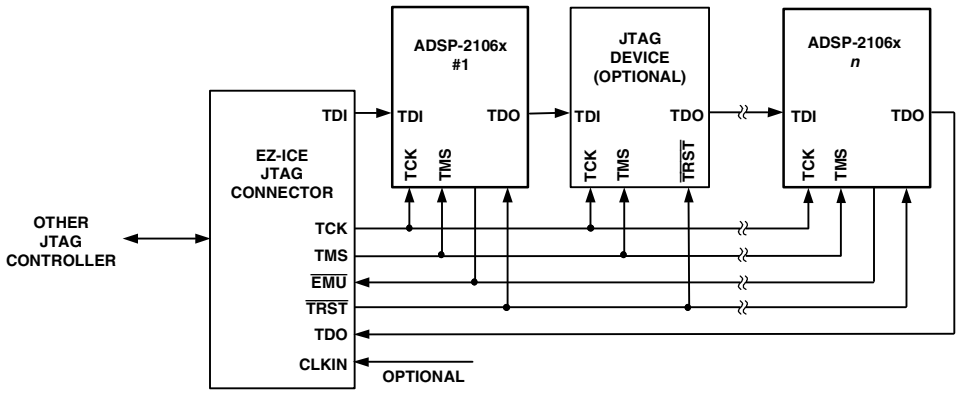

Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

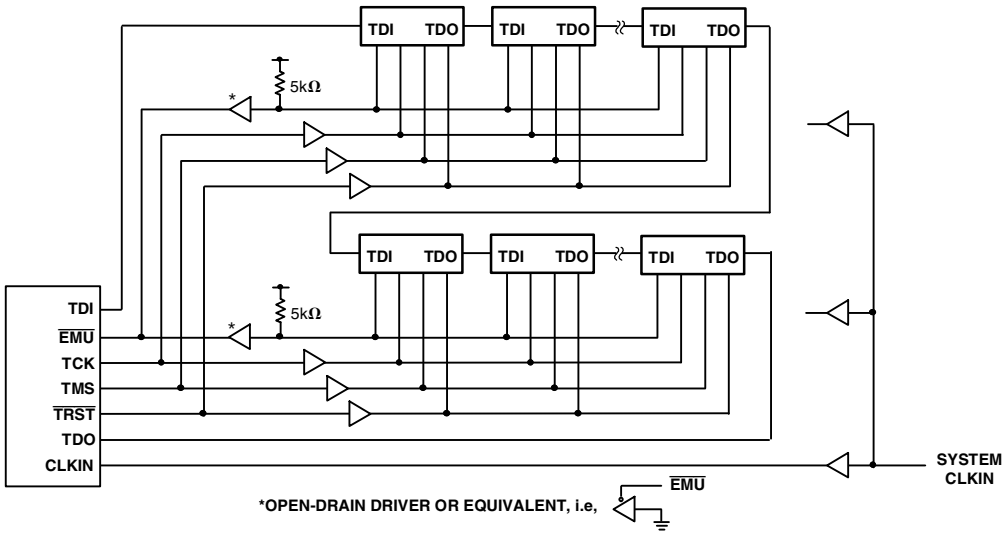

Figure 7. JTAG Clock Tree for Multiple ADSP-2106x Systems

ADSP-21061L SPECIFICATIONS

OPERATING CONDITIONS (3.3 V)

Parameter	Description	A Grade			K Grade			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	3.15	3.3	3.45	3.15	3.3	3.45	V
T_{CASE}	Case Operating Temperature	–40		+85	0		+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0		V_{DD} + 0.5	2.0		V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2		V_{DD} + 0.5	2.2		V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5		+0.8	–0.5		+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1,2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" on Page 45 for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 12. Memory Read—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address, Selects[3]	0.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 4]		15 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DRHA}	Address, Selects Hold After $\overline{RD}$ High	0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[2]	2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup Before ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data delay/setup: user must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] Data hold: user must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}. See Example System Hold Time Calculation on Page 43 for the calculation of hold times given capacitive and dc loads.
[4] ACK delay/setup: user must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} (Table 13 on Page 25) for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).

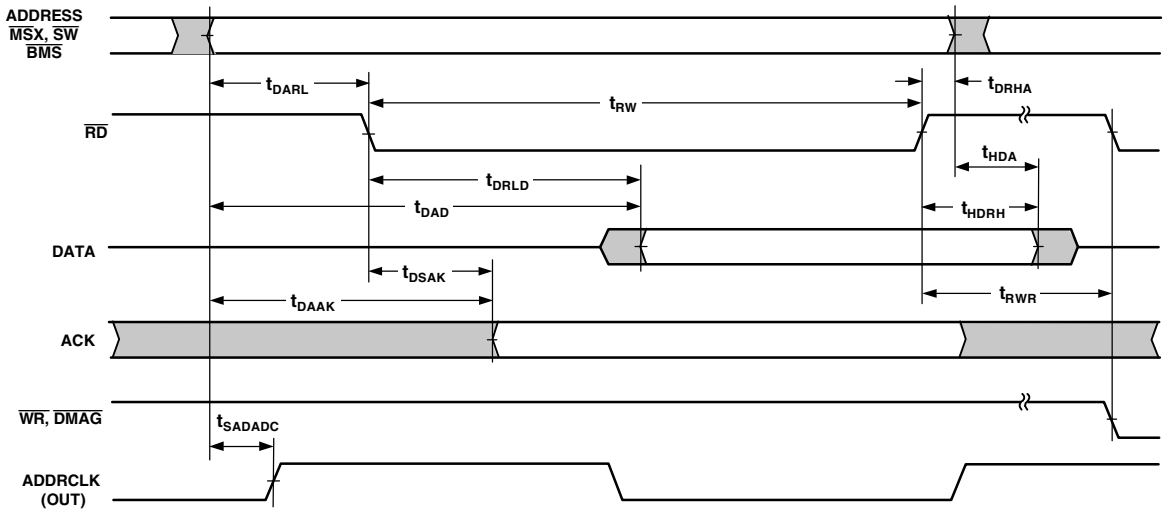

Figure 14. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 13. Memory Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		15 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	17 + 15DT/16 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulse Width	13 + 9DT/16 + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	7 + DT/2 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	1 + DT/16 + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1 + DT/16 + H	6 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 7DT/16 + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	5 + 3DT/8 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–1 + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] ACK delay/setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] For more information, see Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.

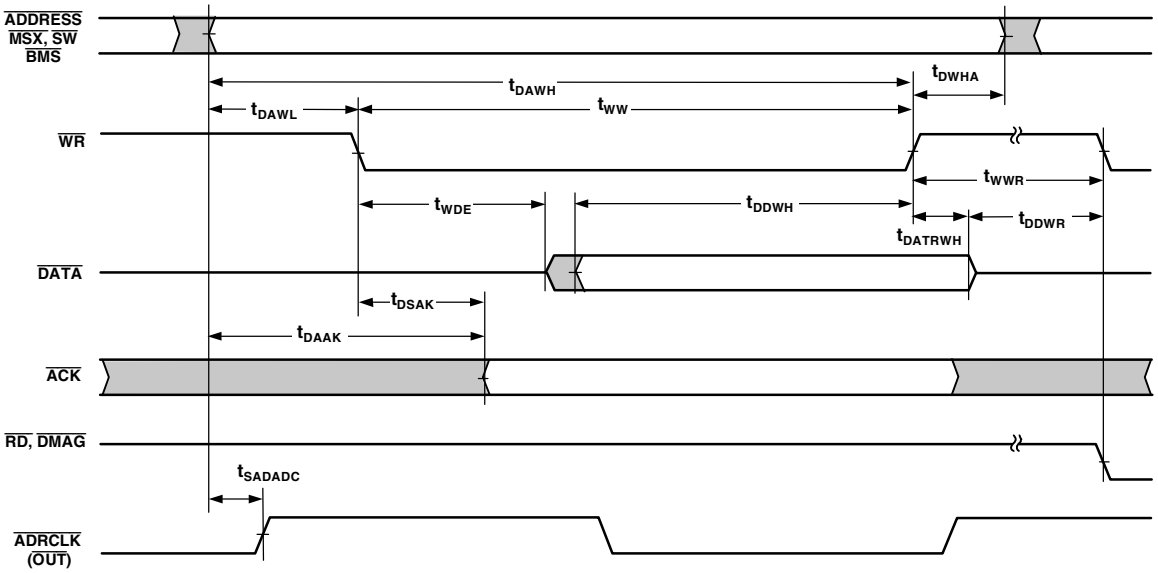

Figure 15. Memory Write—Bus Master

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21061s ($\overline{BRx}$) or a host processor, both synchronous and asynchronous ($\overline{HBR}$, $\overline{HBG}$).

Table 16. Multiprocessor Bus Request and Host Bus Request

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		20 + 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[2]		14 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN High		6 + DT/2	ns
t_{SBRI}	$\overline{BRx}$, $\overline{CPA}$ Setup Before CLKIN[3]	13 + DT/2		ns
t_{HBRI}	$\overline{BRx}$, $\overline{CPA}$ Hold After CLKIN High		6 + DT/2	ns
t_{SRPBAI}	RPBA Setup Before CLKIN	20 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold After CLKIN		12 + 3DT/4	ns
Switching Characteristics				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	–2 – DT/8		ns
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN		5.5 – DT/8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN	–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay After CLKIN[4]		6.5 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable After CLKIN	–2 – DT/8	4.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[5, 6]		8	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[5, 7]	44 + 27DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[5]		10	ns

[1] For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-21061" section in the *ADSP-2106x SHARC User's Manual*.

[2] Only required for recognition in the current cycle.

[3] $\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

[4] For the ADSP-21061L (3.3 V), this specification is 8.5 – DT/8 ns max.

[5] (O/D) = open drain, (A/D) = active drive.

[6] For the ADSP-21061L (3.3 V), this specification is 12 ns max.

[7] For the ADSP-21061L (3.3 V), this specification is 40 + 23DT/16 ns min.

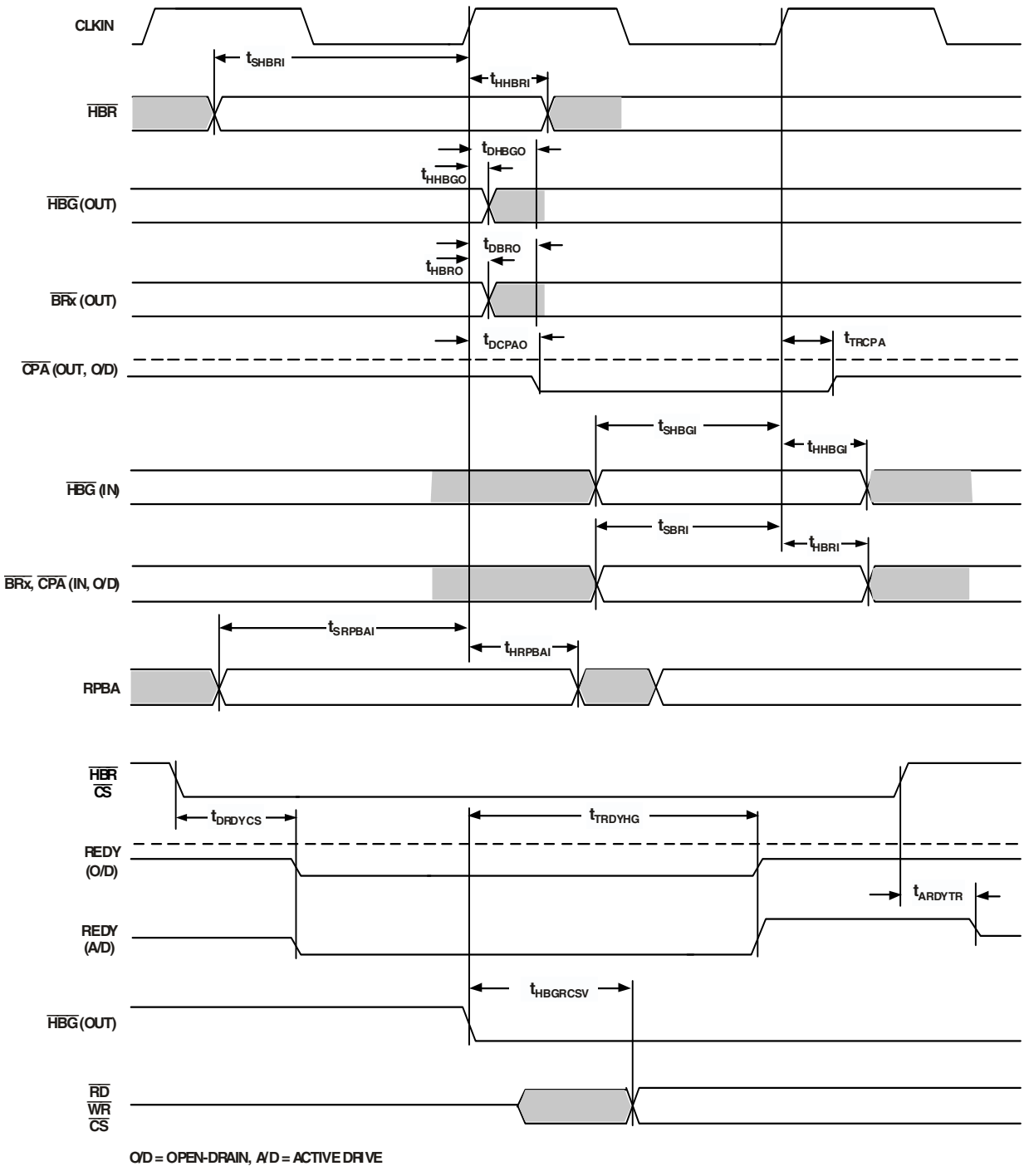

Figure 18. Multiprocessor Bus Request and Host Bus Request

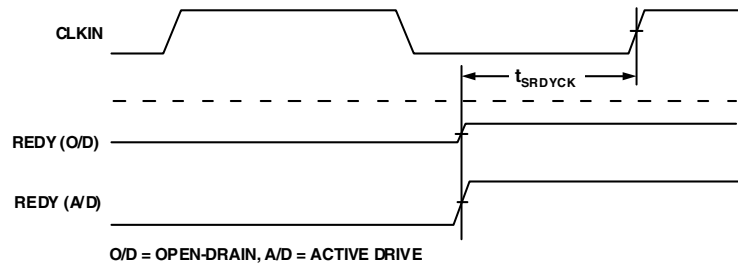

Figure 19. Synchronous REDY Timing

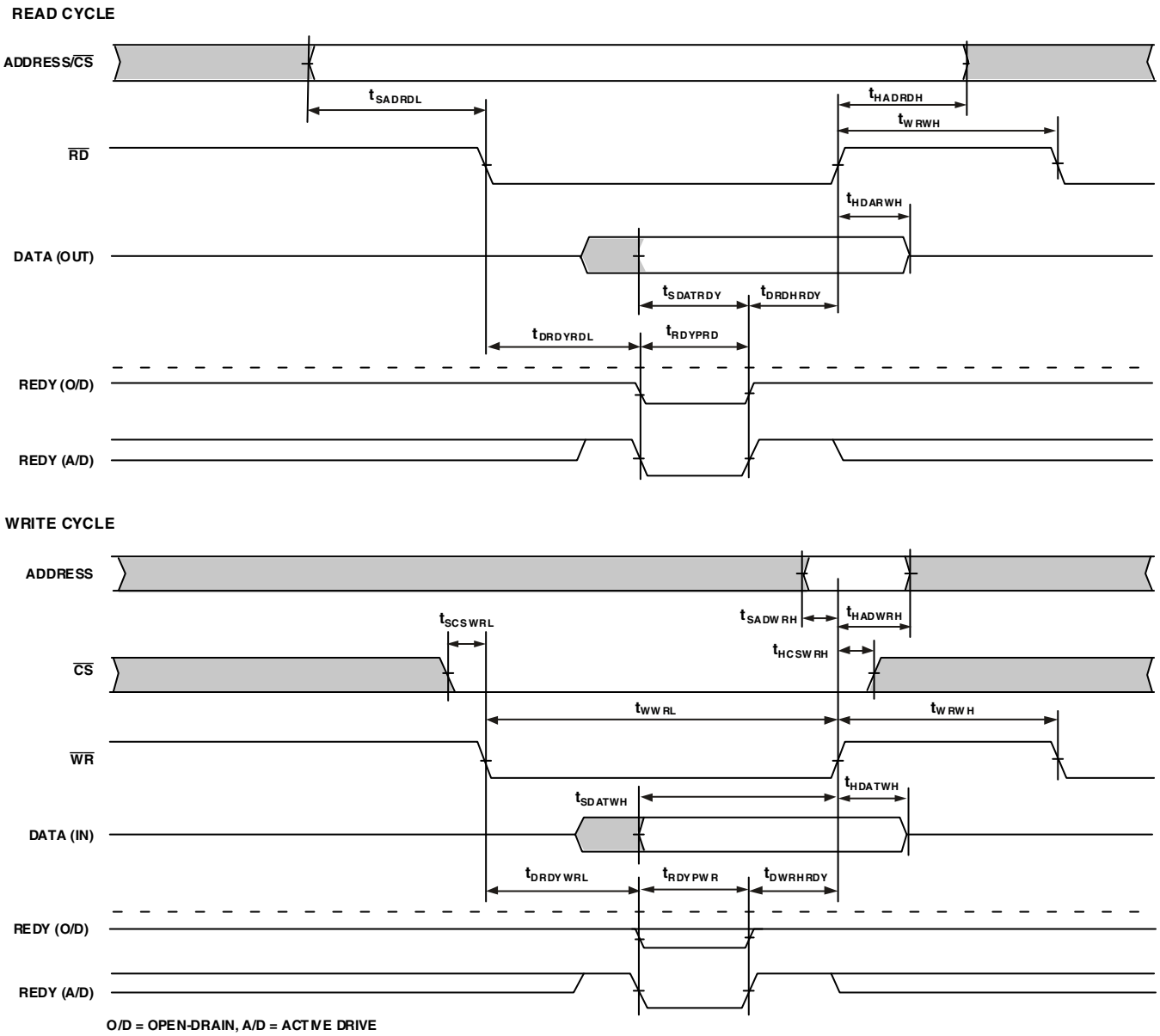

Figure 20. Asynchronous Read/Write—Host to ADSP-21061

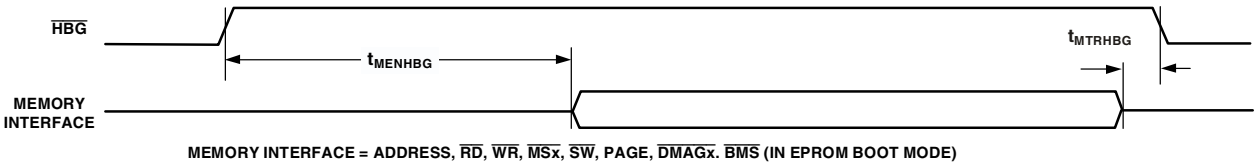

Figure 22. Three-State Timing (Bus Transition Cycle, SBTS Assertion)

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For Handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For External Handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAGx}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, $\overline{\text{SW}}$, PAGE, DATA47–0, and ACK also apply.

Table 20. DMA Handshake

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SDRLC}	$\overline{\text{DMARx}}$ Low Setup Before CLKIN[1]	5		ns
t_{SDRHC}	$\overline{\text{DMARx}}$ High Setup Before CLKIN[1]	5		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)	6		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[2]		10 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMARx}}$ High[2]		16 + 7DT/8	ns
t_{DMARLL}	$\overline{\text{DMARx}}$ Low Edge to Low Edge[3]	23 + 7DT/8		ns
t_{DMARH}	$\overline{\text{DMARx}}$ Width High	6		ns
Switching Characteristics				
t_{DDGL}	$\overline{\text{DMAGx}}$ Low Delay After CLKIN	9 + DT/4	15 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAGx}}$ High Width	6 + 3DT/8		ns
t_{WDGL}	$\overline{\text{DMAGx}}$ Low Width	12 + 5DT/8		ns
t_{HDGC}	$\overline{\text{DMAGx}}$ High Delay After CLKIN	–2 – DT/8	6 – DT/8	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAGx}}$ High[4]	8 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAGx}}$ High[5]	0	7	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DGWRH}	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WR}}$ High	10 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High Before $\overline{\text{DMAGx}}$ High	1 + DT/16	3 + DT/16	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ High	11 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High Before $\overline{\text{DMAGx}}$ High	0	3	ns
t_{DGWR}	$\overline{\text{DMAGx}}$ High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAGx}}$ Low	5 + 3DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAGx}}$ High	17 + DT		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAGx}}$ High[6]	–0.5		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.
[3] For the ADSP-21061L (3.3 V), this specification is 23.5 + 7DT/8 ns min.
[4] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - .25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
[5] See Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.
[6] For the ADSP-21061L (3.3 V), this specification is –1.0 ns min.

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 21. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	3.5		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4		ns
t_{SCLKW}	TCLK/RCLK Width	9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 22. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	8		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	1		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 23. Serial Ports—External or Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[1]		13	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[1]	3		ns

[1] Referenced to drive edge.

Table 24. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[1]		13	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[1]	3		ns
t_{DDTE}	Transmit Data Delay After TCLK[1]		16	ns
t_{HODTE}	Transmit Data Hold After TCLK[1]	5		ns

[1] Referenced to drive edge.

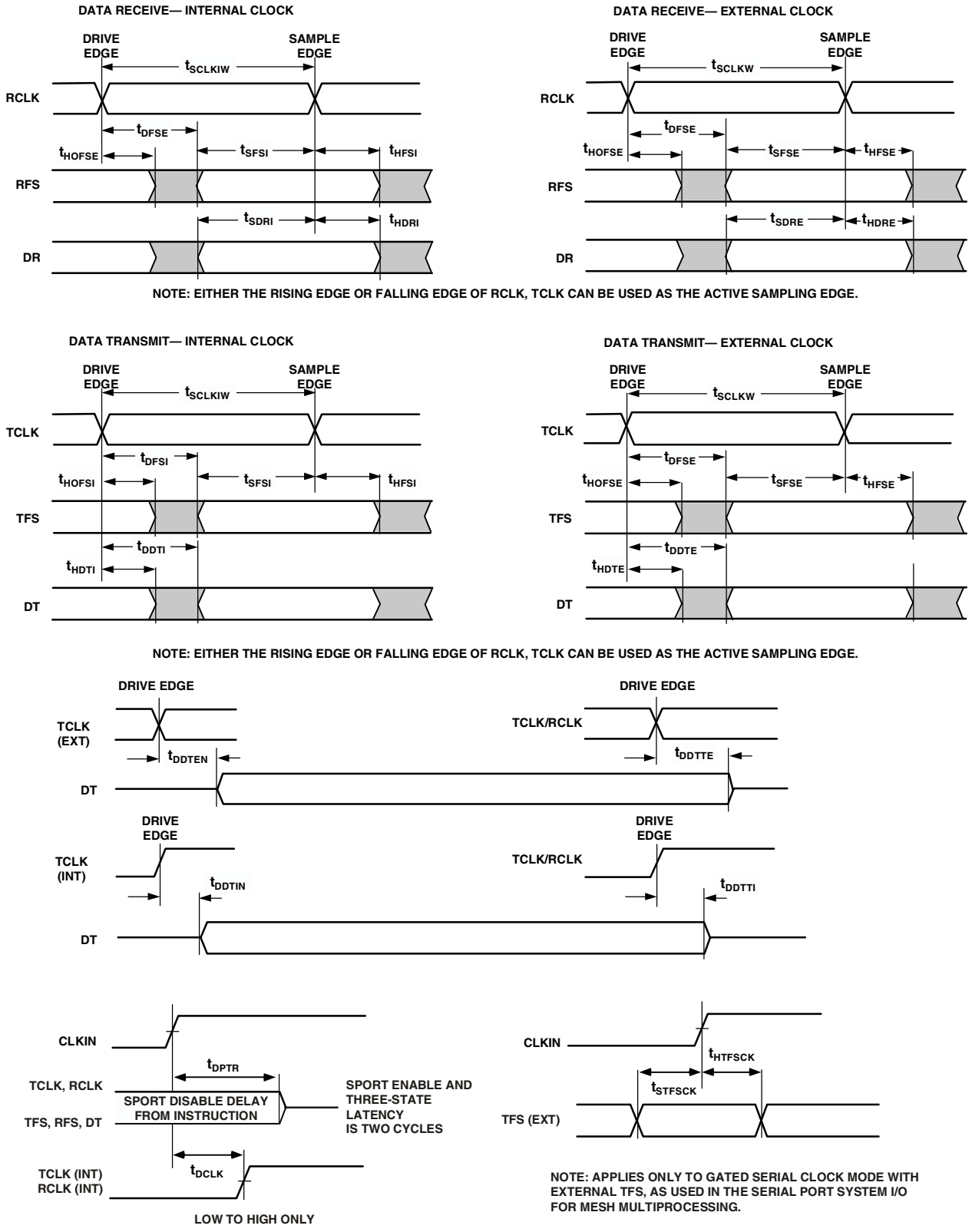

Figure 24. Serial Ports

JTAG Test Access Port and Emulation

For JTAG Test Access Port and Emulation, see Table 28 and Figure 26.

Table 28. JTAG Test Access Port and Emulation

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	t_{CK}		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		18.5	ns

[1] System Inputs = DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{IRQ2–0}$, FLAG3–0, $\overline{CPA}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.

[2] System Outputs = DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, ADRCLK, CLKOUT, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{CPA}$, FLAG3–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$.

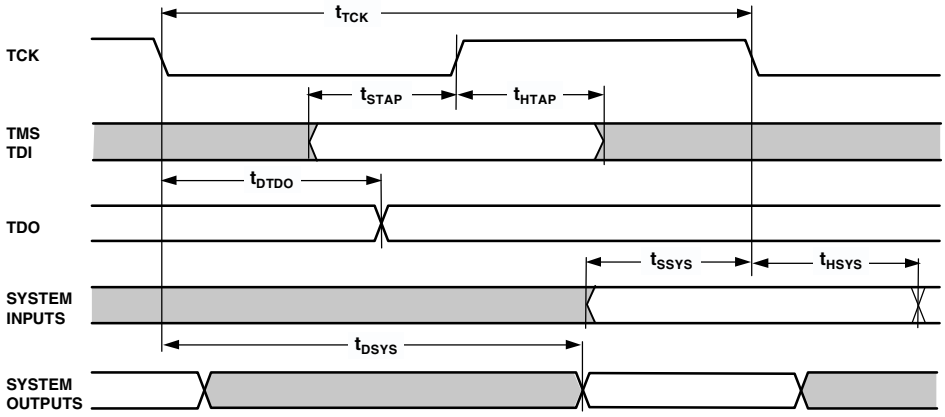

Figure 26. JTAG Test Access Port and Emulation

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21061 is available in 240-lead thermally enhanced MQFP package. The top surface of the thermally enhanced MQFP contains a metal slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the metal slug is internally connected to GND through the device substrate.

The ADSP-21061L is available in 240-lead MQFP and 225-ball plastic BGA packages.

All packages are specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} is not exceeded, a heatsink and/or an airflow source may be used. A heat sink should be attached with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD\ \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

T_{AMB} = Ambient temperature °C

PD =Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} =Value from tables below.

Table 29. ADSP-21061 (5 V Thermally Enhanced ED/MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	10	°C/W
	Airflow = 100	9	
	Airflow = 200	8	
	Airflow = 400	7	
	Airflow = 600	6	

Table 30. ADSP-21061L (3.3 V MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.6	°C/W
	Airflow = 100	17.6	
	Airflow = 200	15.6	
	Airflow = 400	13.9	
	Airflow = 600	12.2	

Table 31. ADSP-21061L (3.3 V PBGA Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.0	°C/W
	Airflow = 200	13.6	
	Airflow = 400	11.2	

225-BALL PBGA PIN CONFIGURATIONS

Table 32. ADSP-21061L 225-Lead Metric PBGA (B-225-2) Pin Assignments

Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number
$\overline{BMS}$	A01	ADDR25	D01	ADDR14	G01	ADDR6	K01	$\overline{EMU}$	N01
ADDR30	A02	ADDR26	D02	ADDR15	G02	ADDR5	K02	TDO	N02
$\overline{DMAR2}$	A03	$\overline{MS2}$	D03	ADDR16	G03	ADDR3	K03	$\overline{IRQ0}$	N03
DT1	A04	ADDR29	D04	ADDR19	G04	ADDR0	K04	$\overline{IRQ1}$	N04
RCLK1	A05	$\overline{DMAR1}$	D05	GND	G05	ICSA	K05	ID2	N05
TCLK0	A06	TFS1	D06	V_{DD}	G06	GND	K06	NC	N06
RCLK0	A07	$\overline{CPA}$	D07	V_{DD}	G07	V_{DD}	K07	NC	N07
ADRCLK	A08	$\overline{HBG}$	D08	V_{DD}	G08	V_{DD}	K08	NC	N08
$\overline{CS}$	A09	$\overline{DMAG2}$	D09	V_{DD}	G09	V_{DD}	K09	NC	N09
CLKIN	A10	$\overline{BR5}$	D10	V_{DD}	G10	GND	K10	NC	N10
PAGE	A11	$\overline{BR1}$	D11	GND	G11	GND	K11	NC	N11
$\overline{BR3}$	A12	DATA40	D12	DATA22	G12	DATA8	K12	NC	N12
DATA47	A13	DATA37	D13	DATA25	G13	DATA11	K13	NC	N13
DATA44	A14	DATA35	D14	DATA24	G14	DATA13	K14	DATA1	N14
DATA42	A15	DATA34	D15	DATA23	G15	DATA14	K15	DATA3	N15
$\overline{MS0}$	B01	ADDR21	E01	ADDR12	H01	ADDR2	L01	$\overline{TRST}$	P01
$\overline{SW}$	B02	ADDR22	E02	ADDR11	H02	ADDR1	L02	TMS	P02
ADDR31	B03	ADDR24	E03	ADDR13	H03	FLAG0	L03	EBOOT	P03
$\overline{HBR}$	B04	ADDR27	E04	ADDR10	H04	FLAG3	L04	ID0	P04
DR1	B05	GND	E05	GND	H05	RPBA	L05	NC	P05
DT0	B06	GND	E06	V_{DD}	H06	GND	L06	NC	P06
DR0	B07	GND	E07	V_{DD}	H07	GND	L07	NC	P07
REDY	B08	GND	E08	V_{DD}	H08	GND	L08	NC	P08
$\overline{RD}$	B09	GND	E09	V_{DD}	H09	GND	L09	NC	P09
ACK	B10	GND	E10	V_{DD}	H10	GND	L10	NC	P10
$\overline{BR6}$	B11	NC	E11	GND	H11	NC	L11	NC	P11
$\overline{BR2}$	B12	DATA33	E12	DATA18	H12	DATA4	L12	NC	P12
DATA45	B13	DATA30	E13	DATA19	H13	DATA7	L13	NC	P13
DATA43	B14	DATA32	E14	DATA21	H14	DATA9	L14	NC	P14
DATA39	B15	DATA31	E15	DATA20	H15	DATA10	L15	DATA0	P15
$\overline{MS3}$	C01	ADDR17	F01	ADDR9	J01	FLAG1	M01	TCK	R01
$\overline{MS1}$	C02	ADDR18	F02	ADDR8	J02	FLAG2	M02	$\overline{IRQ2}$	R02
ADDR28	C03	ADDR20	F03	ADDR7	J03	TIMEXP	M03	$\overline{RESET}$	R03
$\overline{SBTS}$	C04	ADDR23	F04	ADDR4	J04	TDI	M04	ID1	R04
TCLK1	C05	GND	F05	GND	J05	LBOOT (GND)	M05	NC	R05
RFS1	C06	GND	F06	V_{DD}	J06	NC	M06	NC	R06
TFS0	C07	V_{DD}	F07	V_{DD}	J07	NC	M07	NC	R07
RFS0	C08	V_{DD}	F08	V_{DD}	J08	NC	M08	NC	R08
$\overline{WR}$	C09	V_{DD}	F09	V_{DD}	J09	NC	M09	NC	R09
$\overline{DMAG1}$	C10	GND	F10	V_{DD}	J10	NC	M10	NC	R10
$\overline{BR4}$	C11	GND	F11	GND	J11	NC	M11	NC	R11
DATA46	C12	DATA29	F12	DATA12	J12	NC	M12	NC	R12

OUTLINE DIMENSIONS

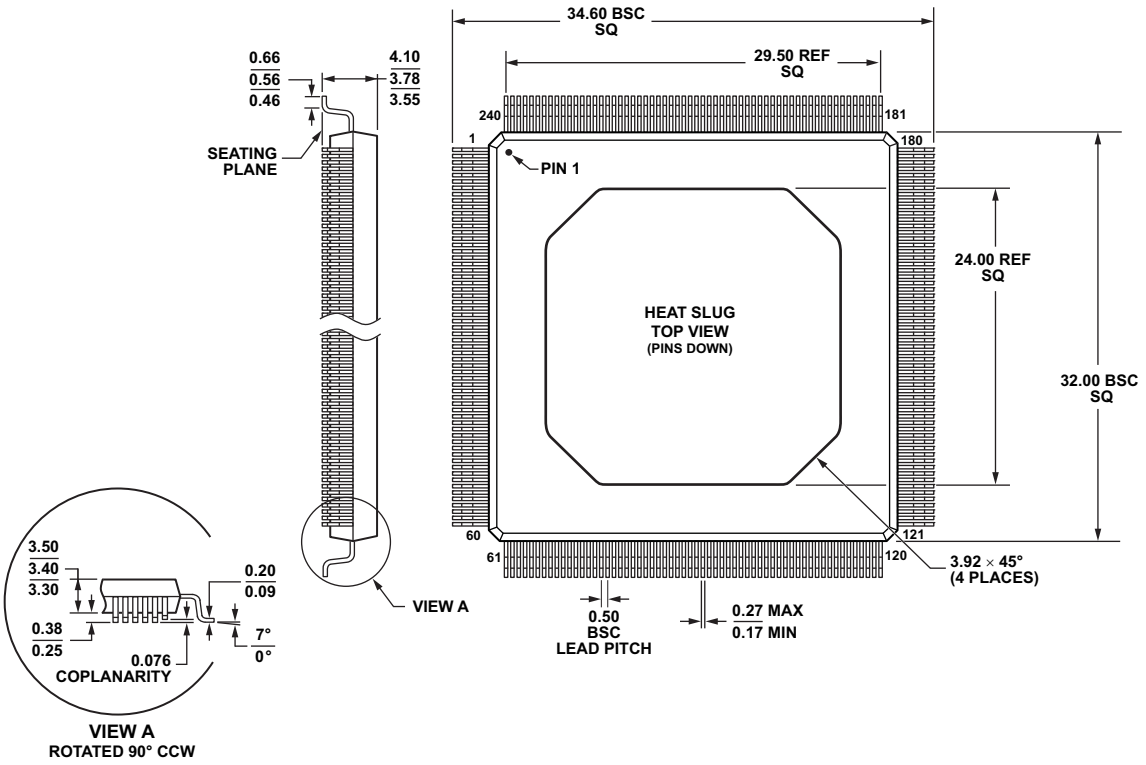

Figure 39. 240-Lead Metric Quad Flat Package, Thermally Enhanced [MQFP/ED] (SP-240-2)