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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	50MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21061ks-200

Program Booting

The internal memory of the ADSP-21061 can be booted at system power-up from either an 8-bit EPROM, or a host processor. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (boot memory select), EBOOT (EPROM boot), and LBOOT (host boot) pins. 32-bit and 16-bit host processors can be used for booting.

PORTING CODE FROM THE ADSP-21060 OR ADSP-21062

The ADSP-21061 is pin compatible with the ADSP-21060/ADSP-21061/ADSP-21062 processors. The ADSP-21061 pins that correspond to the link port pins of the ADSP-21060/ADSP-21062 are no-connects.

The ADSP-21061 is object code compatible with the ADSP-21060/ADSP-21062 processors except for the following functional elements:

- The ADSP-21061 memory is organized into two blocks with eight columns that are 4k deep per block. The ADSP-21060/ADSP-21062 memory has 16 columns per block.
- Link port functions are not available.
- Handshake external port DMA pins DMAR2 and DMAG2 are assigned to external port DMA Channel 6 instead of Channel 8.
- 2-D DMA capability of the SPORT is not available.
- The modify registers in SPORT DMA are not programmable.

On the ADSP-21061, Block 0 starts at the beginning of internal memory, normal word address 0x0002 0000. Block 1 starts at the end of Block 0, with contiguous addresses. The remaining addresses in internal memory are divided into blocks that alias into Block 1. This allows any code or data stored in Block 1 on the ADSP-21062 to retain the same addresses on the ADSP- 21061—these addresses will alias into the actual Block 1 of each processor.

If you develop your application using the ADSP-21062, but will migrate to the ADSP-21061, use only the first eight columns of each memory bank. Limit your application to 8k of instructions or up to 16k of data in each bank of the ADSP-21062, or any combination of instructions or data that does not exceed the memory bank.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

PIN FUNCTION DESCRIPTIONS

ADSP-21061 pin definitions are listed below. All pins are identical on the ADSP-21061 and ADSP-21061L. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31-0, DATA47-0, FLAG3-0, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTx, DRx, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 2. Pin Descriptions

Pin	Type	Function
$ADDR_{31-0}$	I/O/T	**External Bus Address.** The ADSP-21061 outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/write of the internal memory or IOP registers of other ADSP-21061s. The ADSP-21061 inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
$DATA_{47-0}$	I/O/T	**External Bus Data.** The ADSP-21061 inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over Bits 47 to 16 of the bus. 40-bit extended-precision floating-point data is transferred over Bits 47 to 8 of the bus. 16-bit short word data is transferred over Bits 31 to 16 of the bus. In PROM boot mode, 8-bit data is transferred over Bits 23 to 16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{MS}_{3-0}$	O/T	**Memory Select Lines.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-21061's system control register (SYSCON). The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{3-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{MS}_0$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{MS}_{3-0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** This pin is asserted (low) when the ADSP-21061 reads from external memory devices or from the internal memory of other ADSP-21061s. External devices (including other ADSP-21061s) must assert $\overline{\text{RD}}$ to read from the ADSP-21061's internal memory. In a multiprocessing system $\overline{\text{RD}}$ is output by the bus master and is input by all other ADSP-21061s.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted (low) when the ADSP-21061 writes to external memory devices or to the internal memory of other ADSP-21061s. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21061's internal memory. In a multiprocessing system $\overline{\text{WR}}$ is output by the bus master and is input by all other ADSP-21061s.
PAGE	O/T	**DRAM Page Boundary.** The ADSP-21061 asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-21061's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system PAGE is output by the bus master.
ADRCLK	O/T	**Clock Output Reference.** In a multiprocessing system ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal is used to interface the ADSP-21061 to synchronous memory devices (including other ADSP-21061s). The ADSP-21061 asserts $\overline{\text{SW}}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by all other ADSP-21061s to determine if the multiprocessor memory access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-21061(s).

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, TDI, TDO, and GND signals be made accessible on the target system via a 14-pin connector (a 2-row, 7-pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the farthest device sharing the EZ-ICE JTAG pin should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

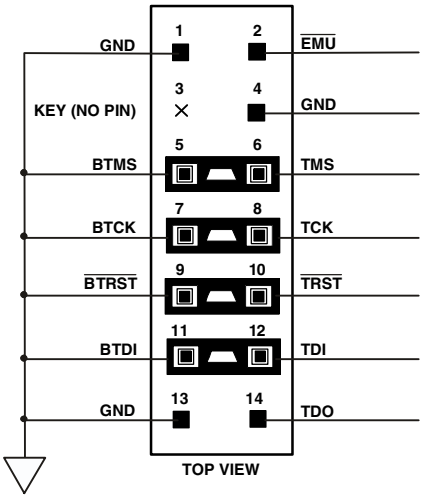

Figure 5. Target Board Connector For ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inches in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec. The BTMS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing.

When the connector is not being used for emulation, place jumpers between the Bxxx pins and the xxx pins as shown in Figure 5. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted (pulsed low) after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, and 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as shown in Table 3.

Table 3. Core Instruction Rate/CLKIN Ratio Selection

Signal	Termination
TMS	Driven Through 22 Ω Resistor (16 mA Driver)
TCK	Driven at 10 MHz Through 22 Ω Resistor (16 mA Driver)
$\overline{\text{TRST}}$[1]	Active Low Driven Through 22 Ω Resistor (16 mA Driver) (Pulled Up by On-Chip 20 kΩ Resistor)
TDI	Driven by 22 Ω Resistor (16 mA Driver)
TDO	One TTL Load, Split Termination (160/220)
CLKIN	One TTL Load, Split Termination (160/220)
$\overline{\text{EMU}}$	Active Low, 4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP)

[1] $\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software startup. After software startup, is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-21061 processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN, and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-21061s (more than eight) in your system, then treat them as a "clock tree" using multiple drivers to minimize skew. (See Figure 7 below and "JTAG Clock Tree" and "Clock Distribution" in the "High Frequency Design Considerations" section of the *ADSP-2106x SHARC User's Manual*.)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$, and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

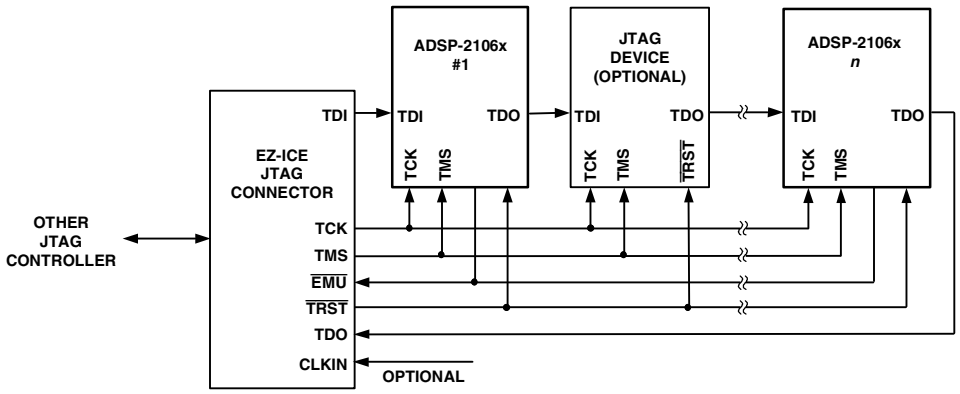

Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

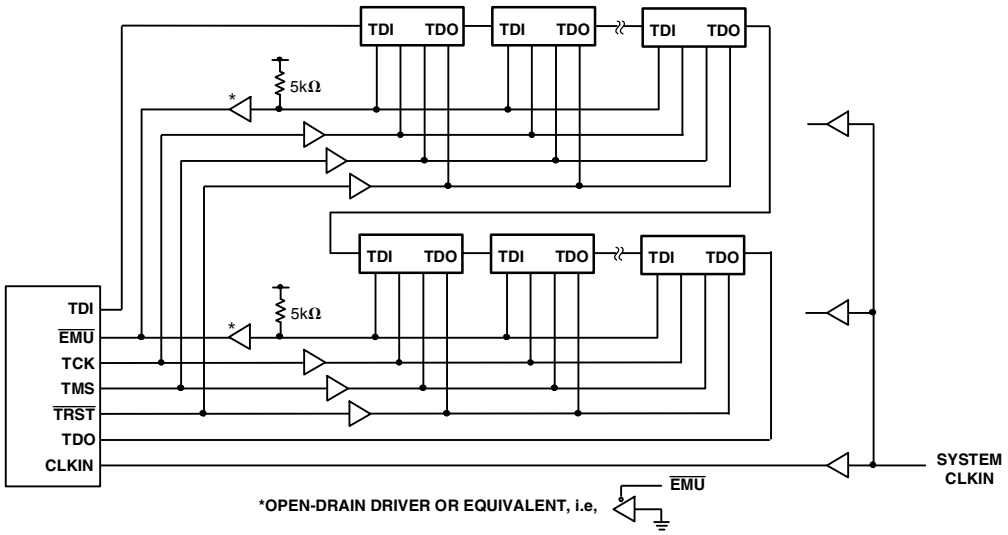

Figure 7. JTAG Clock Tree for Multiple ADSP-2106x Systems

ADSP-21061 SPECIFICATIONS

OPERATING CONDITIONS (5 V)

Parameter	Description	K Grade			Unit
		Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
T_{CASE}	Case Operating Temperature	0		85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0		V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2		V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5		+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (5 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	4.1		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" on Page 44 for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups:DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios:

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

%PEAK $I_{DDINPEAK}$ + *%HIGH* $I_{DDINHIGH}$ + *%LOW* $I_{DDINLOW}$ + *%IDLE* I_{DDIDLE} = *power consumption*

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	595	mA
	t_{CK} = 25 ns, V_{DD} = Max	680	mA
	t_{CK} = 20 ns, V_{DD} = Max	850	
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	460	mA
	t_{CK} = 25 ns, V_{DD} = Max	540	mA
	t_{CK} = 20 ns, V_{DD} = Max	670	
$I_{DDINLOW}$ Supply Current (Internal)[3]	t_{CK} = 30 ns, V_{DD} = Max	270	mA
	t_{CK} = 25 ns, V_{DD} = Max	320	mA
	t_{CK} = 20 ns, V_{DD} = Max	390	
I_{DDIDLE} Supply Current (Idle)[4]	V_{DD} = Max	200	mA
I_{DDIDLE} Supply Current (Idle16)[5]	V_{DD} = Max	55	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[4] Idle denotes ADSP-21061L state during execution of IDLE instruction.

[5] Idle16 denotes ADSP-2106x state during execution of IDLE16 instruction.

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:
$P_{INT} = I_{DDIN} \times V_{DD}$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- —the number of output pins that switch during each cycle (O)
- —the maximum frequency at which they can switch (f)
- —their load capacitance (C)
- —their voltage swing (V_{DD})

and is calculated by:

$$PEXT = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128k × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

Table 5. External Power Calculations

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	—	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	—	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W

P_{EXT} = 0.074 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:
$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Clock Input

Table 7. Clock Input

Parameter		ADSP-21061 50 MHz, 5 V Min	ADSP-21061 50 MHz, 5 V Max	ADSP-21061L 44 MHz, 3.3 V Min	ADSP-21061L 44 MHz, 3.3 V Max	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Min	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Max	ADSP-21061 33 MHz, 5 V Min	ADSP-21061 33 MHz, 5 V Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	20	100	22.5	100	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		7		7		ns
t_{CKH}	CLKIN Width High	5		5		5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns

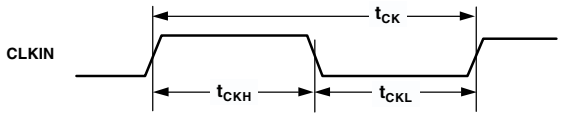

Figure 9. Clock Input

Reset

Table 8. Reset

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including startup time of external clock oscillator).

[2] Only required if multiple ADSP-21061s must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21061s communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

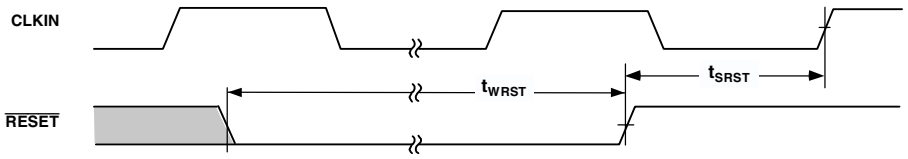

Figure 10. Reset

Flags

Table 11. Flags

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFI}	FLAG3–0 IN Setup Before CLKIN High[1]	8 + 5DT/16		ns
t_{HFI}	FLAG3–0 IN Hold After CLKIN High[1]	0 – 5DT/16		ns
t_{DWRFI}	FLAG3–0 IN Delay After $\overline{RD}$/$\overline{WR}$ Low[1]		5 + 7DT/16	ns
t_{HFIWR}	FLAG3–0 IN Hold After $\overline{RD}$/$\overline{WR}$ Deasserted[1]	0		ns
Switching Characteristics				
t_{DFO}	FLAG3–0 OUT Delay After CLKIN High		16	ns
t_{HFO}	FLAG3–0 OUT Hold After CLKIN High	4		ns
t_{DFOE}	CLKIN High to FLAG3–0 OUT Enable	3		ns
t_{DFOD}	CLKIN High to FLAG3–0 OUT Disable		14	ns

[1] Flag inputs meeting these setup and hold times for Instruction Cycle N will affect conditional instructions in Instruction Cycle N+2.

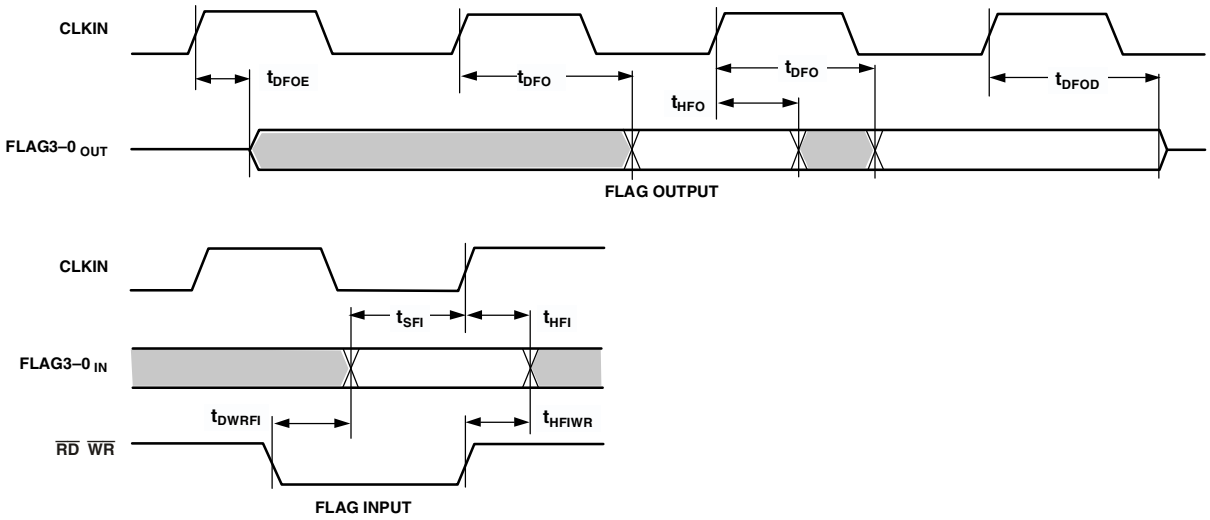

Figure 13. Flags

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-21061 (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read—Bus Master on Page 24 and Memory Write—Bus Master on Page 25). When accessing a slave ADSP-21061, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave on Page 28). The slave ADSP-21061 must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 14. Synchronous Read/Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN (50 MHz, t_{CK} = 20 ns)[1]	2 + DT/8 1.5 + DT/8		ns
t_{HSDATI}	Data Hold After CLKIN	3.5 – DT/8		ns
t_{DAAK}	ACK Delay After Address, Selects[2, 3]		15 + 7DT/8 + W	ns
t_{SACKC}	ACK Setup Before CLKIN[3]	6.5 + DT/4		ns
t_{HACK}	ACK Hold After CLKIN	–1 – DT/4		ns
Switching Characteristics				
t_{DADRO}	Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[2]		6.5 – DT/8	ns
t_{HADRO}	Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	–1 – DT/8		ns
t_{DPGC}	PAGE Delay After CLKIN	9 + DT/8	16 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	–1.5 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN (50 MHz, t_{CK} = 20 ns)	–2.5 – 3DT/16 –1.5 – 3DT/16	4 – 3DT/16 4 – 3DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	8 + DT/4	12 + DT/4	ns
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[4]	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay After CLKIN	4 + DT/8	10 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		ns

[1] This specification applies to the ADSP-21061KS-200 (5 V, 50 MHz) operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] ACK delay/setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).
[4] See Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.

Synchronous Read/Write—Bus Slave

Use these specifications for ADSP-21061 bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Table 15. Synchronous Read/Write—Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	14 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold After CLKIN		5 + DT/2	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup Before CLKIN[1]	8.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold After CLKIN	–4 – 5DT/16	8 + 7DT/16	ns
	44 MHz/50 MHz[2]	–3.5 – 5DT/16	8 + 7DT/16	
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	3		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	3		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[3]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay After Address, $\overline{SW}$[4]		8	ns
t_{ACKTR}	ACK Disable After CLKIN[2]	–1 – DT/8	6 – DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5DT/16 when multiprocessor memory space wait state (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min)= 4 + DT/8.

[2] This specification applies to the ADSP-21061LKS-176 (3.3 V, 44 MHz) and the ADSP-21061KS-200 (5 V, 50 MHz), operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.

[3] See Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.

[4] t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. If the address and inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

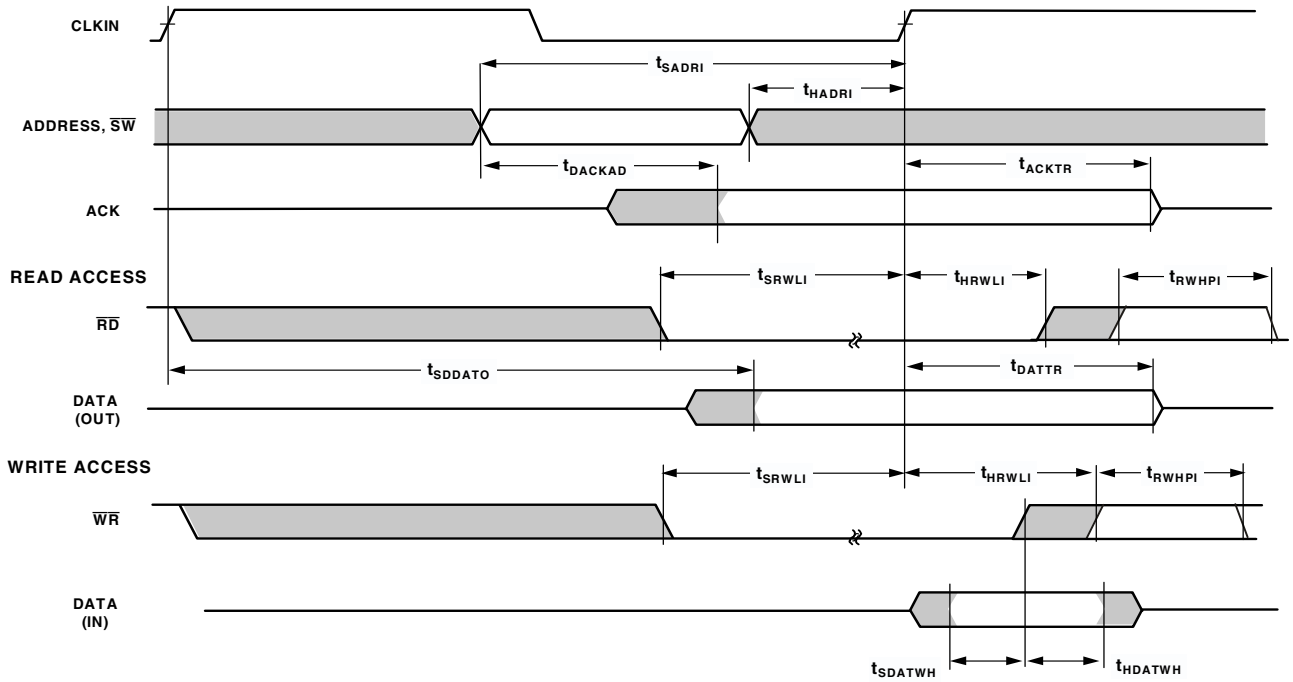

Figure 17. Synchronous Read/Write—Bus Slave

Asynchronous Read/Write—Host to ADSP-21061

Use these specifications for asynchronous host processor accesses of an ADSP-21061, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21061, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21061's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Table 17. Read Cycle

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low[1]	0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$	0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low[2]		10	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	45 + DT		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2	8	ns

[1] Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-21061" section in the *ADSP-2106x SHARC User's Manual*.
[2] For the ADSP-21061L (3.3 V), this specification is 13.5 ns max.

Table 18. Write Cycle

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2		ns
t_{WWRL}	$\overline{WR}$ Low Width	8		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	3		ns
	50 MHz, t_{CK} = 20 ns[1]	2.5		
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low[2]		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write	15		ns
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKIN	1 + 7DT/16	8 + 7DT/16	ns

[1] This specification applies to the ADSP-21061KS-200 (5 V, 50 MHz) operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.
[2] For the ADSP-21061L (3.3 V), this specification is 13.5 ns max.

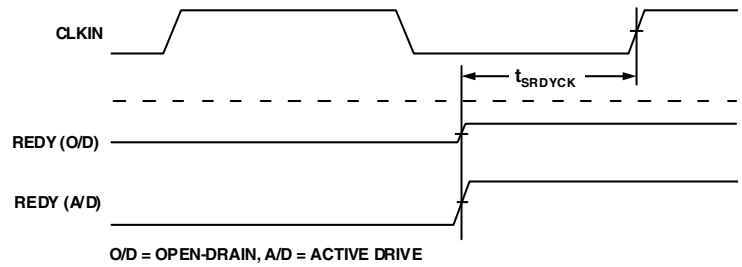

Figure 19. Synchronous REDY Timing

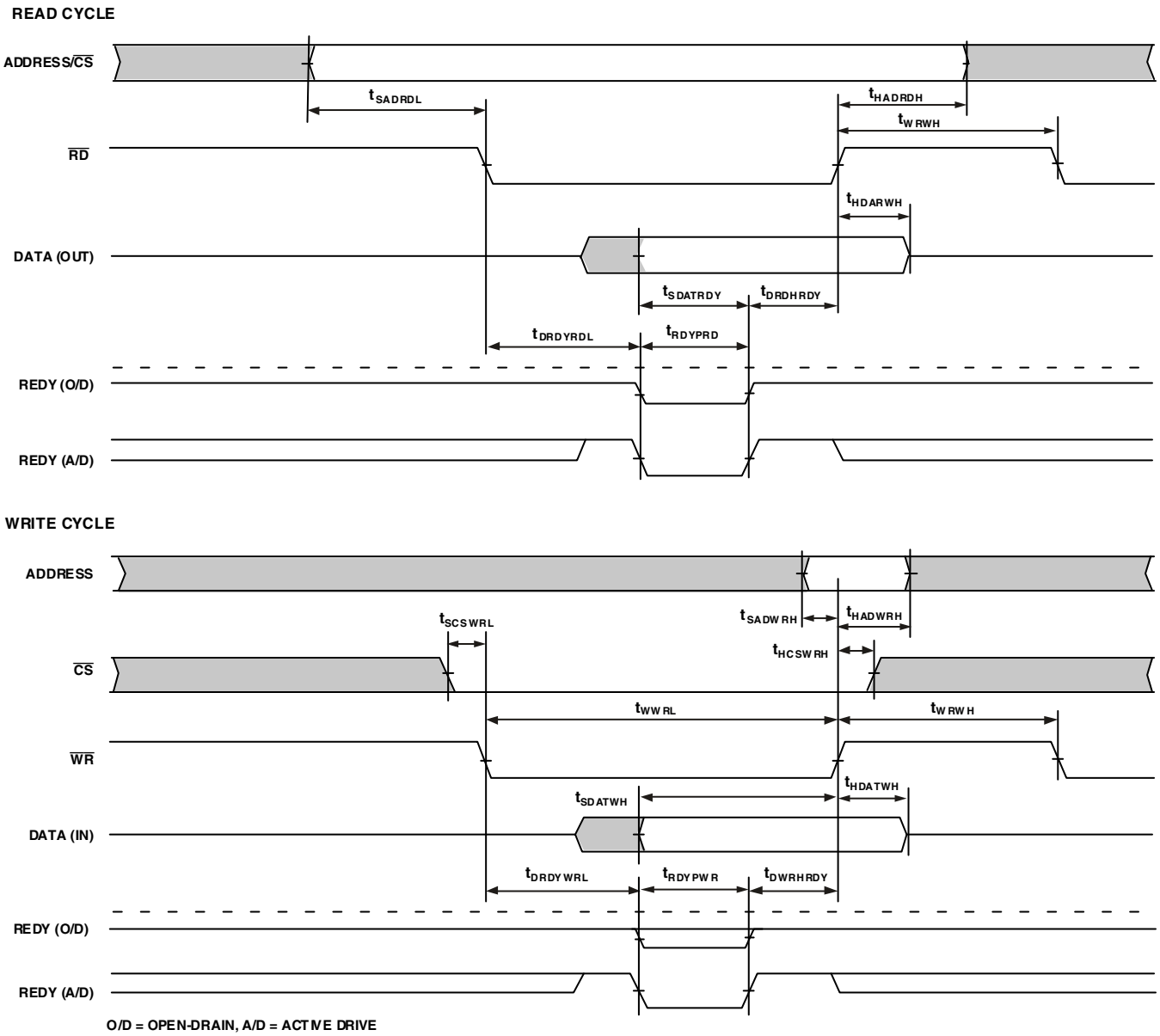

Figure 20. Asynchronous Read/Write—Host to ADSP-21061

Table 25. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width	$t_{SCLK}/2 - 1.5$	$t_{SCLK}/2 + 1.5$	ns

[1] Referenced to drive edge.

Table 26. Serial Ports—Enable and Three-State

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1, 2]	4.5		ns
t_{DDTTE}	Data Disable from External TCLK[1]		10.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1]		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		22 + 3DT/8	ns
t_{DPTR}	SPORT Disable After CLKIN		17	ns

[1] Referenced to drive edge.
[2] For the ADSP-21061L (3.3 V), this specification is 3.5 ns min.

Table 27. Serial Ports—External Late Frame Sync

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1]		12	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	3.5		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

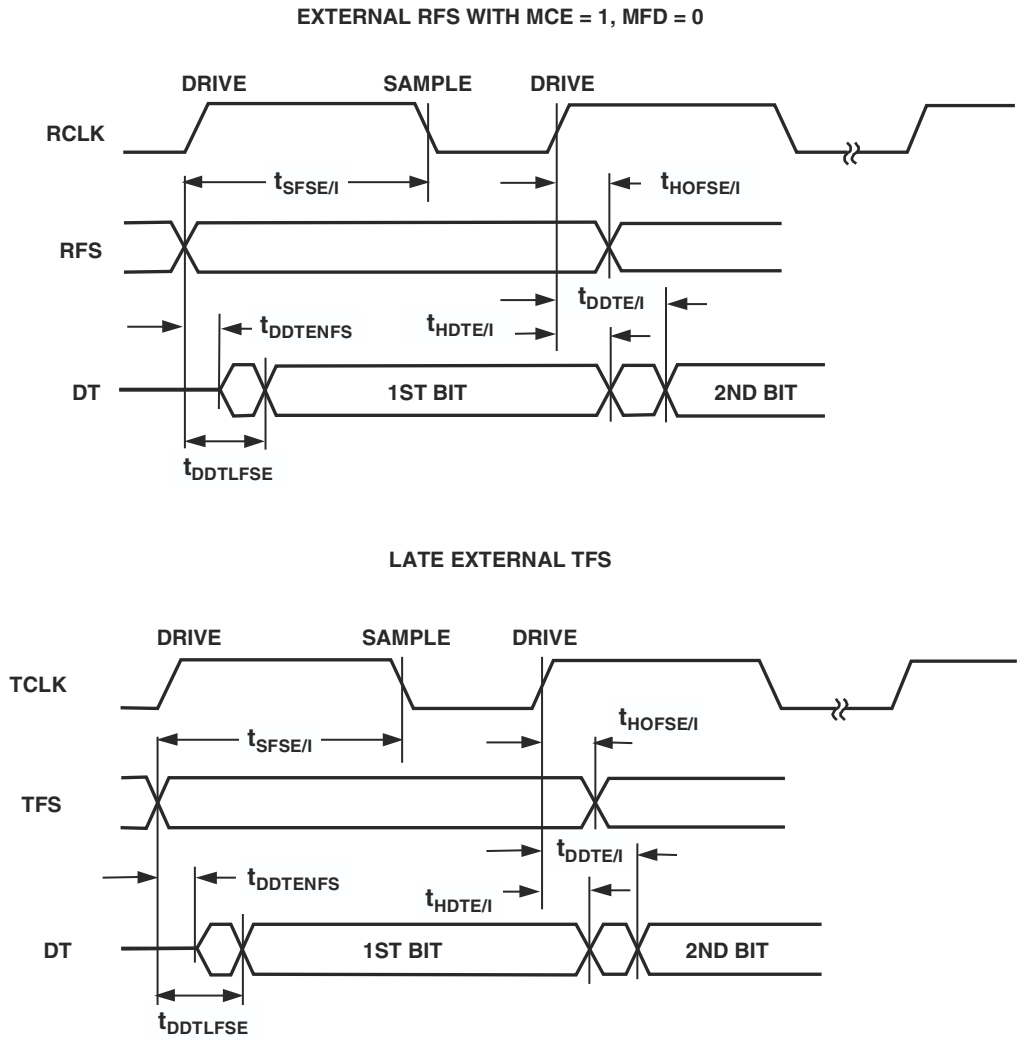

Figure 25. Serial Ports—External Late Frame Sync

JTAG Test Access Port and Emulation

For JTAG Test Access Port and Emulation, see Table 28 and Figure 26.

Table 28. JTAG Test Access Port and Emulation

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	t_{CK}		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		18.5	ns

[1] System Inputs = DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{IRQ2–0}$, FLAG3–0, $\overline{CPA}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.

[2] System Outputs = DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, ADRCLK, CLKOUT, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{CPA}$, FLAG3–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$.

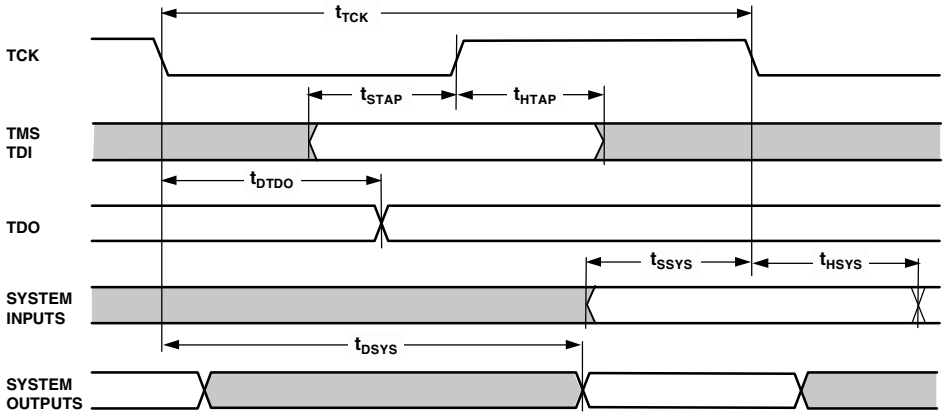

Figure 26. JTAG Test Access Port and Emulation

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21061 is available in 240-lead thermally enhanced MQFP package. The top surface of the thermally enhanced MQFP contains a metal slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the metal slug is internally connected to GND through the device substrate.

The ADSP-21061L is available in 240-lead MQFP and 225-ball plastic BGA packages.

All packages are specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} is not exceeded, a heatsink and/or an airflow source may be used. A heat sink should be attached with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD\ \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

T_{AMB} = Ambient temperature °C

PD =Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} =Value from tables below.

Table 29. ADSP-21061 (5 V Thermally Enhanced ED/MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	10	°C/W
	Airflow = 100	9	
	Airflow = 200	8	
	Airflow = 400	7	
	Airflow = 600	6	

Table 30. ADSP-21061L (3.3 V MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.6	°C/W
	Airflow = 100	17.6	
	Airflow = 200	15.6	
	Airflow = 400	13.9	
	Airflow = 600	12.2	

Table 31. ADSP-21061L (3.3 V PBGA Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.0	°C/W
	Airflow = 200	13.6	
	Airflow = 400	11.2	

OUTLINE DIMENSIONS

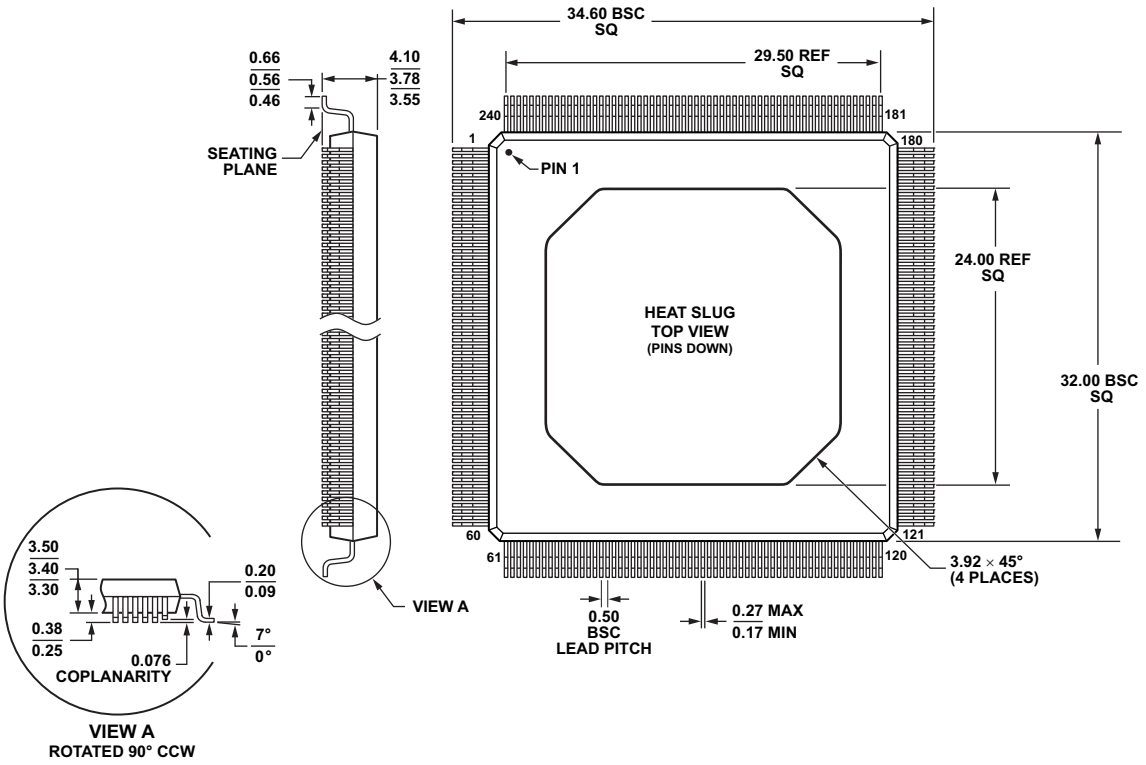

Figure 39. 240-Lead Metric Quad Flat Package, Thermally Enhanced [MQFP/ED] (SP-240-2)

SURFACE-MOUNT DESIGN

Table 34 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 34. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
225-Ball Grid Array (PBGA)	Solder Mask Defined	0.63 mm diameter	0.73 mm diameter

ORDERING GUIDE

Model	Notes	Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Description	Package Option
ADSP-21061KS-133		0°C to 85°C	33 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-133	[1]	0°C to 85°C	33 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KS-160		0°C to 85°C	40 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-160	[1]	0°C to 85°C	40 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KS-200		0°C to 85°C	50 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-200	[1]	0°C to 85°C	50 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061LKB-160		0°C to 85°C	40 MHz	1M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21061LKBZ-160	[1]	0°C to 85°C	40 MHz	1M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21061LKSZ-160	[1]	0°C to 85°C	40 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LASZ-176	[1]	–40°C to +85°C	44 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LKSZ-176	[1]	0°C to 85°C	44 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240

[1] Z = RoHS Compliant Part.