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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	5.00V
Voltage - Core	5.00V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	240-BFQFP Exposed Pad
Supplier Device Package	240-MQFP-EP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21061ksz-160

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REVISION HISTORY

5/13—Rev C to Rev D

Updated Development Tools 7

Added Related Signal Chains 8

Removed the ADSP-21061LAS-176, ADSP-21061LKS-160, and ADSP-21061LKS-176 models from Ordering Guide 52

GENERAL NOTE

This data sheet represents production released specifications for the ADSP-21061 (5 V) and ADSP-21061L (3.3 V) processors for 33 MHz, 40 MHz, 44 MHz, and 50 MHz speed grades. The product name“ADSP-21061” is used throughout this data sheet to represent all devices, except where expressly noted.

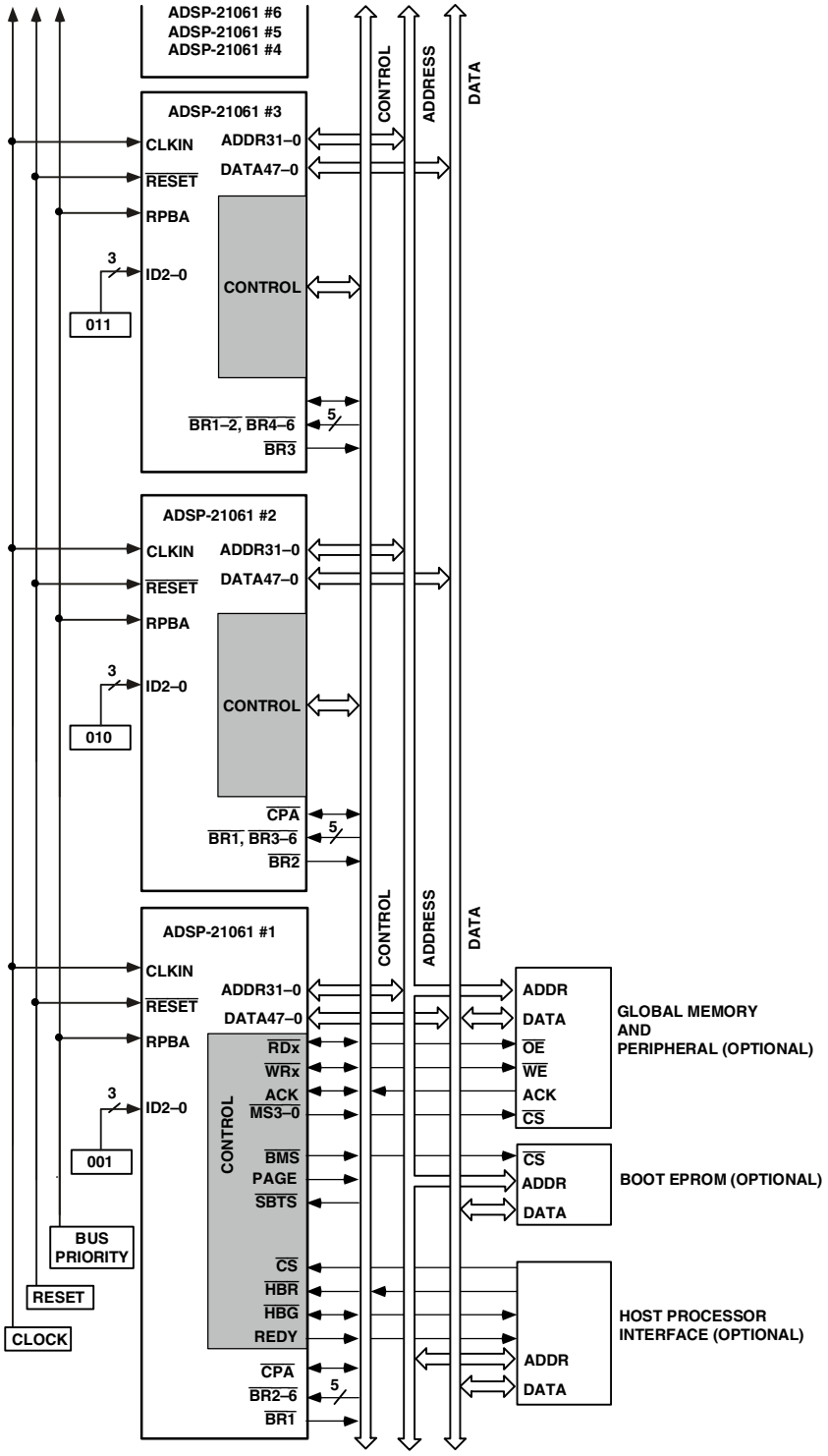

Figure 3. Shared Memory Multiprocessing System

DMA transfers can occur between the ADSP-21061's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21061's internal memory and its serial ports.

DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Program Booting

The internal memory of the ADSP-21061 can be booted at system power-up from either an 8-bit EPROM, or a host processor. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (boot memory select), EBOOT (EPROM boot), and LBOOT (host boot) pins. 32-bit and 16-bit host processors can be used for booting.

PORTING CODE FROM THE ADSP-21060 OR ADSP-21062

The ADSP-21061 is pin compatible with the ADSP-21060/ADSP-21061/ADSP-21062 processors. The ADSP-21061 pins that correspond to the link port pins of the ADSP-21060/ADSP-21062 are no-connects.

The ADSP-21061 is object code compatible with the ADSP-21060/ADSP-21062 processors except for the following functional elements:

- The ADSP-21061 memory is organized into two blocks with eight columns that are 4k deep per block. The ADSP-21060/ADSP-21062 memory has 16 columns per block.
- Link port functions are not available.
- Handshake external port DMA pins DMAR2 and DMAG2 are assigned to external port DMA Channel 6 instead of Channel 8.
- 2-D DMA capability of the SPORT is not available.
- The modify registers in SPORT DMA are not programmable.

On the ADSP-21061, Block 0 starts at the beginning of internal memory, normal word address 0x0002 0000. Block 1 starts at the end of Block 0, with contiguous addresses. The remaining addresses in internal memory are divided into blocks that alias into Block 1. This allows any code or data stored in Block 1 on the ADSP-21062 to retain the same addresses on the ADSP- 21061—these addresses will alias into the actual Block 1 of each processor.

If you develop your application using the ADSP-21062, but will migrate to the ADSP-21061, use only the first eight columns of each memory bank. Limit your application to 8k of instructions or up to 16k of data in each bank of the ADSP-21062, or any combination of instructions or data that does not exceed the memory bank.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

Middleware Packages

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21061 architecture and functionality. For detailed information on the ADSP-21000 Family core architecture and instruction set, refer to the *ADSP- 2106x SHARC User's Manual.*

RELATED SIGNAL CHAINS

A *signal chain* is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/signalchains) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

PIN FUNCTION DESCRIPTIONS

ADSP-21061 pin definitions are listed below. All pins are identical on the ADSP-21061 and ADSP-21061L. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31-0, DATA47-0, FLAG3-0, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTx, DRx, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 2. Pin Descriptions

Pin	Type	Function
$ADDR_{31-0}$	I/O/T	**External Bus Address.** The ADSP-21061 outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/write of the internal memory or IOP registers of other ADSP-21061s. The ADSP-21061 inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
$DATA_{47-0}$	I/O/T	**External Bus Data.** The ADSP-21061 inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over Bits 47 to 16 of the bus. 40-bit extended-precision floating-point data is transferred over Bits 47 to 8 of the bus. 16-bit short word data is transferred over Bits 31 to 16 of the bus. In PROM boot mode, 8-bit data is transferred over Bits 23 to 16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{MS}_{3-0}$	O/T	**Memory Select Lines.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-21061's system control register (SYSCON). The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{3-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{MS}_0$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{MS}_{3-0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** This pin is asserted (low) when the ADSP-21061 reads from external memory devices or from the internal memory of other ADSP-21061s. External devices (including other ADSP-21061s) must assert $\overline{\text{RD}}$ to read from the ADSP-21061's internal memory. In a multiprocessing system $\overline{\text{RD}}$ is output by the bus master and is input by all other ADSP-21061s.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted (low) when the ADSP-21061 writes to external memory devices or to the internal memory of other ADSP-21061s. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21061's internal memory. In a multiprocessing system $\overline{\text{WR}}$ is output by the bus master and is input by all other ADSP-21061s.
PAGE	O/T	**DRAM Page Boundary.** The ADSP-21061 asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-21061's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system PAGE is output by the bus master.
ADRCLK	O/T	**Clock Output Reference.** In a multiprocessing system ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal is used to interface the ADSP-21061 to synchronous memory devices (including other ADSP-21061s). The ADSP-21061 asserts $\overline{\text{SW}}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by all other ADSP-21061s to determine if the multiprocessor memory access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-21061(s).

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
TFSx	I/O	**Transmit Frame Sync (Serial Ports 0, 1).**
RFSx	I/O	**Receive Frame Sync (Serial Ports 0, 1).**
EBOOT	I	**EPROM Boot Select.** When EBOOT is high, the ADSP-21061 is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{\text{BMS}}$ inputs determine booting mode. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot.** Must be tied to GND.
$\overline{\text{BMS}}$	I/O/T*	**Boot Memory Select.** *Output*: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that ADSP-21061 will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). *EBOOT* *LBOOT* *$\overline{\text{BMS}}$* *Booting Mode* 1 0 Output EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.) 0 0 1(Input) Host Processor. 0 0 0 (Input) No Booting. Processor executes from external memory.
CLKIN	I	**Clock In.** External clock input to the ADSP-21061. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the minimum specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-21061 to a known state and begins program execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21061. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O	**Emulation Status.** Must be connected to the ADSP-21061 EZ-ICE target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
ICSA	O	**Reserved.** Leave unconnected.
VDD	P	**Power Supply**. (30 pins). See Operating Conditions (5 V) and Operating Conditions (3.3 V).
GND	G	**Power Supply Return.** (30 pins)
NC		**Do Not Connect.** Reserved pins which must be left open and unconnected.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:
$P_{INT} = I_{DDIN} \times V_{DD}$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- —the number of output pins that switch during each cycle (O)
- —the maximum frequency at which they can switch (f)
- —their load capacitance (C)
- —their voltage swing (V_{DD})

and is calculated by:

$$PEXT = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128k × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

Table 5. External Power Calculations

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	—	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	—	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W

P_{EXT} = 0.074 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:
$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Clock Input

Table 7. Clock Input

Parameter		ADSP-21061 50 MHz, 5 V Min	ADSP-21061 50 MHz, 5 V Max	ADSP-21061L 44 MHz, 3.3 V Min	ADSP-21061L 44 MHz, 3.3 V Max	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Min	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Max	ADSP-21061 33 MHz, 5 V Min	ADSP-21061 33 MHz, 5 V Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	20	100	22.5	100	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		7		7		ns
t_{CKH}	CLKIN Width High	5		5		5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns

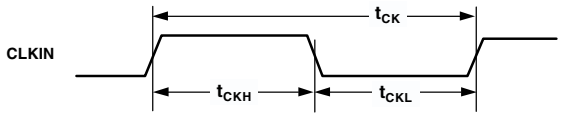

Figure 9. Clock Input

Reset

Table 8. Reset

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including startup time of external clock oscillator).

[2] Only required if multiple ADSP-21061s must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21061s communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

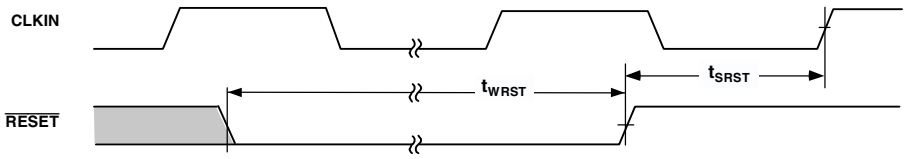

Figure 10. Reset

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 13. Memory Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		15 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	17 + 15DT/16 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulse Width	13 + 9DT/16 + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	7 + DT/2 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	1 + DT/16 + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1 + DT/16 + H	6 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 7DT/16 + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	5 + 3DT/8 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–1 + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] ACK delay/setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] For more information, see Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.

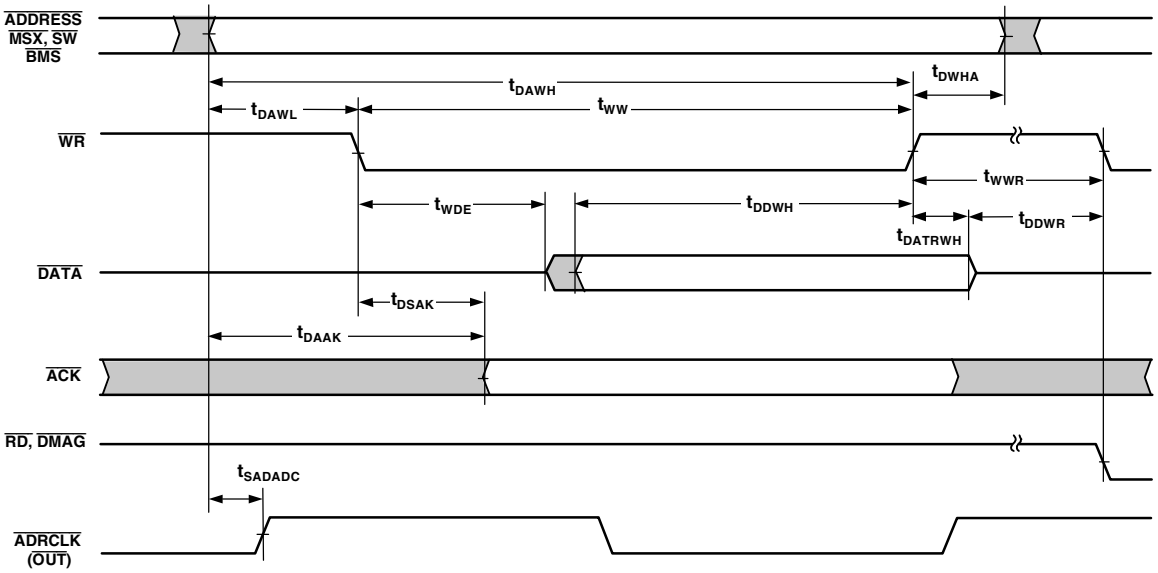

Figure 15. Memory Write—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for ADSP-21061 bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Table 15. Synchronous Read/Write—Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	14 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold After CLKIN		5 + DT/2	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup Before CLKIN[1]	8.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold After CLKIN	–4 – 5DT/16	8 + 7DT/16	ns
	44 MHz/50 MHz[2]	–3.5 – 5DT/16	8 + 7DT/16	
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	3		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	3		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[3]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay After Address, $\overline{SW}$[4]		8	ns
t_{ACKTR}	ACK Disable After CLKIN[2]	–1 – DT/8	6 – DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5DT/16 when multiprocessor memory space wait state (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min)= 4 + DT/8.

[2] This specification applies to the ADSP-21061LKS-176 (3.3 V, 44 MHz) and the ADSP-21061KS-200 (5 V, 50 MHz), operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.

[3] See Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.

[4] t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. If the address and inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

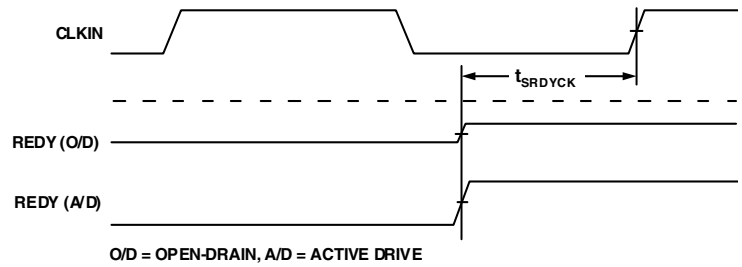

Figure 19. Synchronous REDY Timing

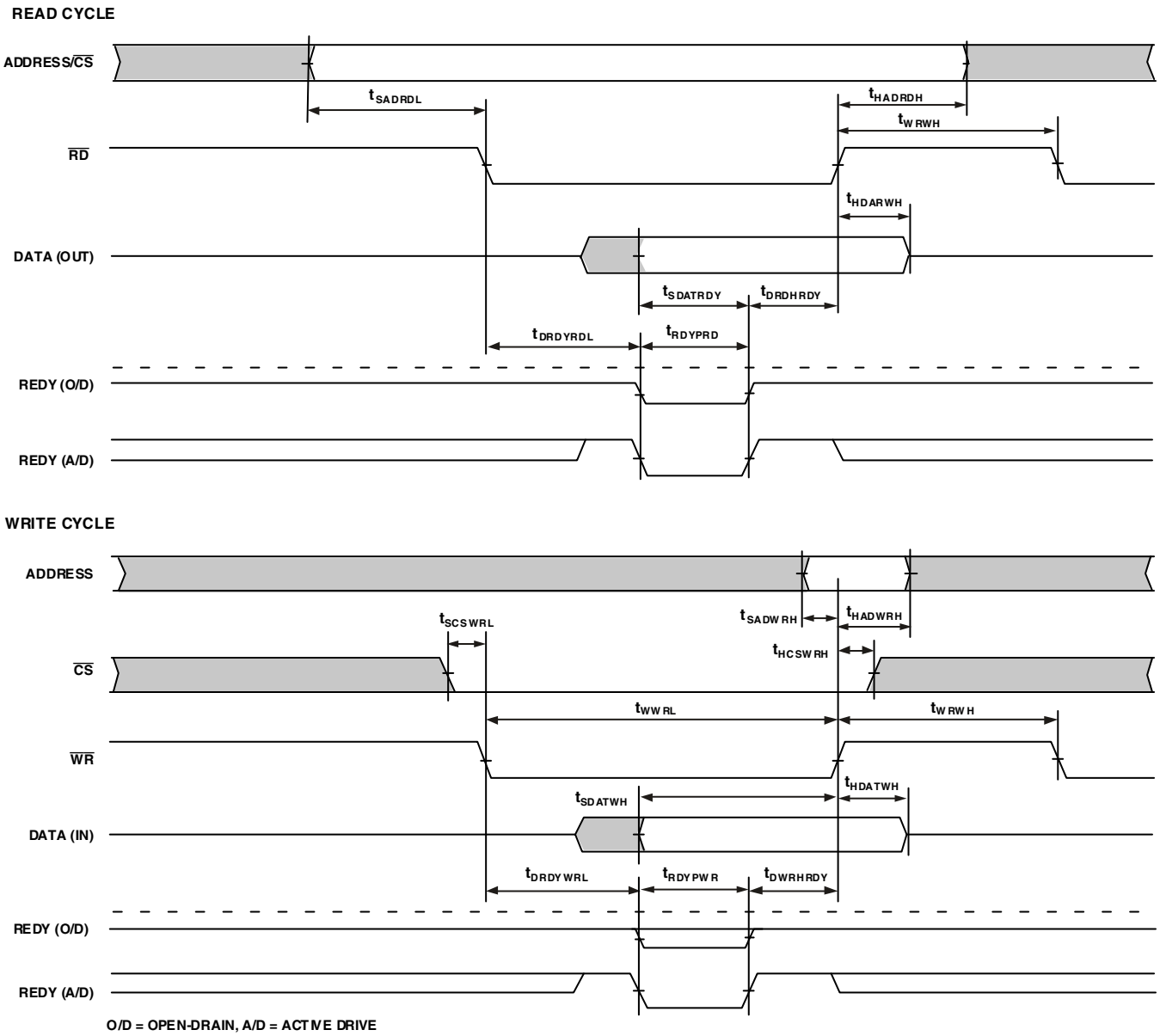

Figure 20. Asynchronous Read/Write—Host to ADSP-21061

Three-State Timing—Bus Master, Bus Slave, HBR, SBTS

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the SBTS pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the SBTS pin.

Table 19. Three-State Timing—Bus Master, Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{STSCK}	SBTS Setup Before CLKIN	12 + DT/2		ns
t_{HTSCK}	SBTS Hold Before CLKIN		6 + DT/2	ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN	–1 – DT/8		ns
t_{MIENS}	Strobes Enable After CLKIN[1]	–1.5 – DT/8		ns
t_{MIENHG}	HBG Enable After CLKIN	–1.5 – DT/8		ns
t_{MITRA}	Address/Select Disable After CLKIN		0 – DT/4	ns
t_{MITRS}	Strobes Disable After CLKIN[1]		1.5 – DT/4	ns
t_{MITRHG}	HBG Disable After CLKIN		2.0 – DT/4	ns
t_{DATEN}	Data Enable After CLKIN[2]	9 + 5DT/16		ns
t_{DATTR}	Data Disable After CLKIN[2]	0 – DT/8	7 – DT/8	ns
t_{ACKEN}	ACK Enable After CLKIN[2]	7.5 + DT/4		ns
t_{ACKTR}	ACK Disable After CLKIN[2]	–1 – DT/8	6 – DT/8	ns
t_{ADCEN}	ADRCLK Enable After CLKIN	–2 – DT/8		ns
t_{ADCTR}	ADRCLK Disable After CLKIN		8 – DT/4	ns
t_{MTRHBG}	Memory Interface Disable Before HBG Low[3]	0 + DT/8		ns
t_{MENHBG}	Memory Interface Enable After HBG High[3]	19 + DT		ns

[1] Strobes = RD, WR, PAGE, DMAGx, MSx, BMS, SW.
[2] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[3] Memory Interface = Address, RD, WR, MSx, SW, PAGE, DMAGx, and BMS (in EPROM boot mode).

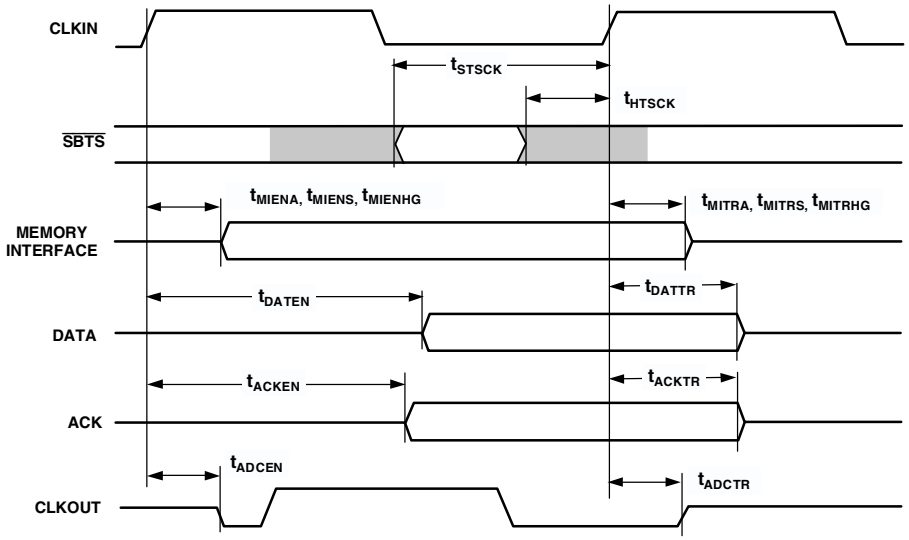

Figure 21. Three-State Timing (Bus Transition Cycle, SBTS Assertion)

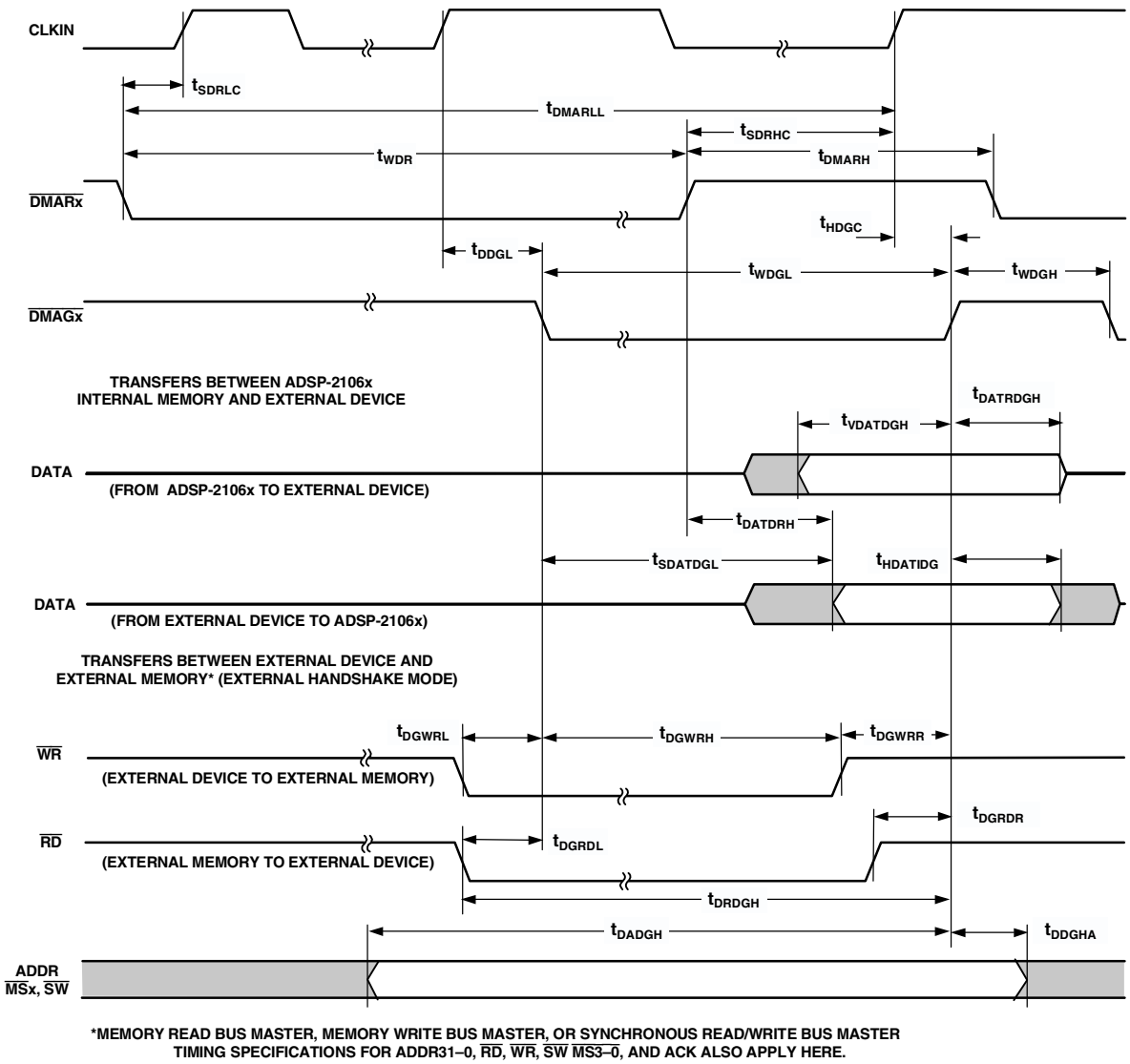

Figure 23. DMA Handshake

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 21. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	3.5		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4		ns
t_{SCLKW}	TCLK/RCLK Width	9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 22. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	8		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	1		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 23. Serial Ports—External or Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[1]		13	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[1]	3		ns

[1] Referenced to drive edge.

Table 24. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[1]		13	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[1]	3		ns
t_{DDTE}	Transmit Data Delay After TCLK[1]		16	ns
t_{HODTE}	Transmit Data Hold After TCLK[1]	5		ns

[1] Referenced to drive edge.

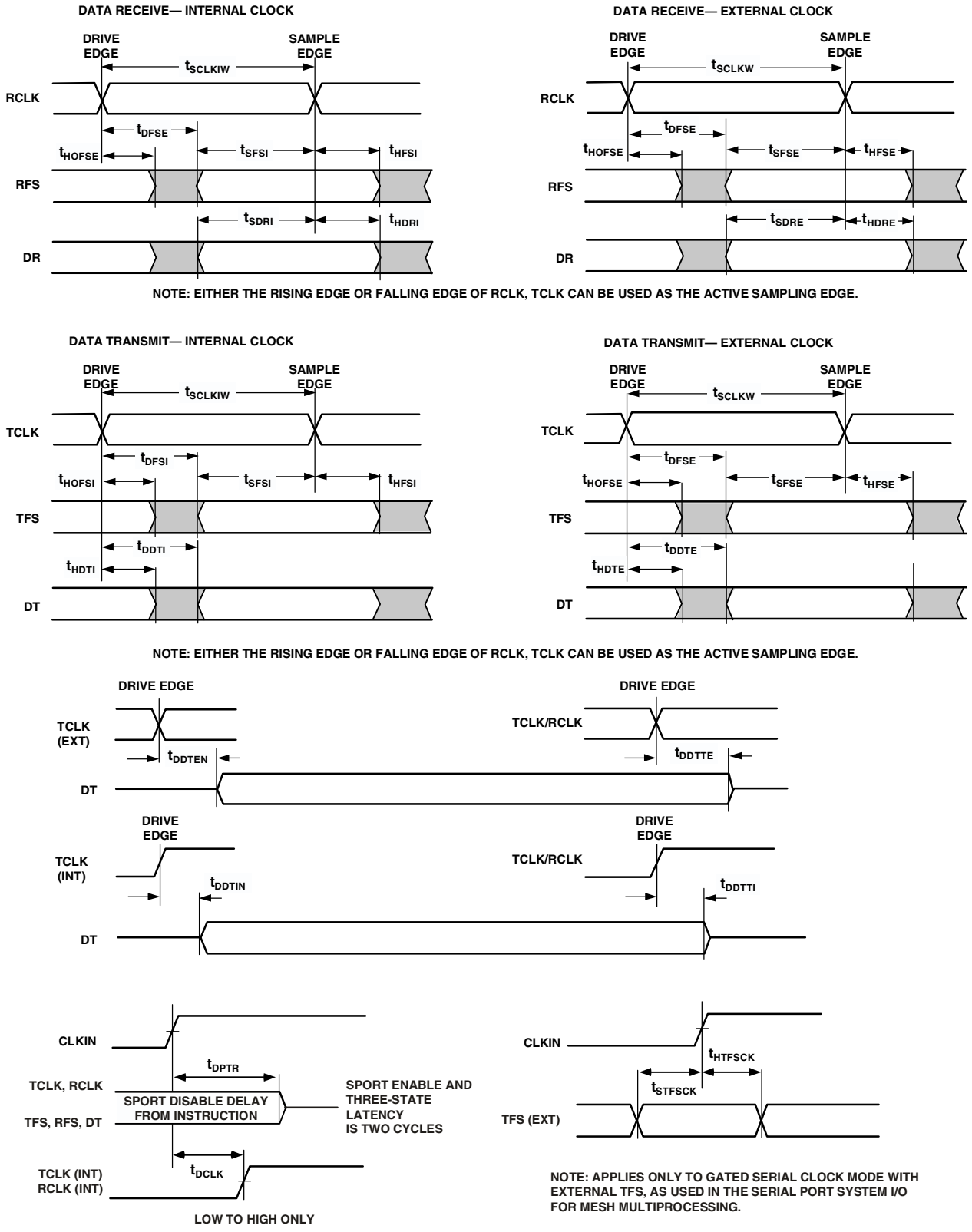

Figure 24. Serial Ports

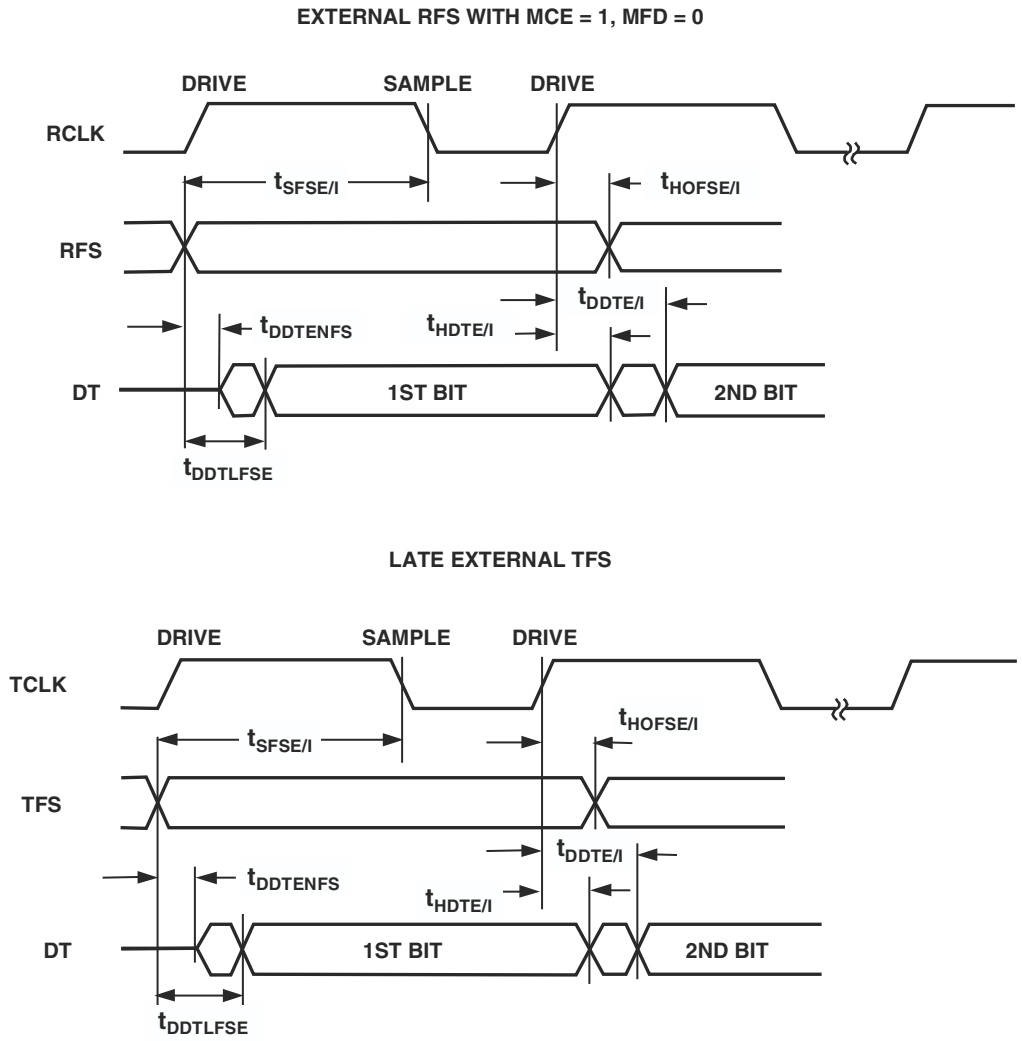

Figure 25. Serial Ports—External Late Frame Sync

JTAG Test Access Port and Emulation

For JTAG Test Access Port and Emulation, see Table 28 and Figure 26.

Table 28. JTAG Test Access Port and Emulation

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	t_{CK}		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		18.5	ns

[1] System Inputs = DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{IRQ2–0}$, FLAG3–0, $\overline{CPA}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.

[2] System Outputs = DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, ADRCLK, CLKOUT, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{CPA}$, FLAG3–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$.

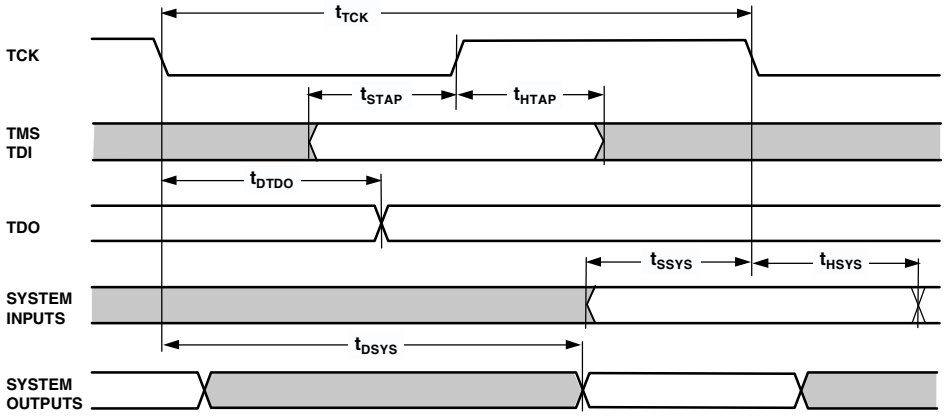

Figure 26. JTAG Test Access Port and Emulation

Output Characteristics (5 V)

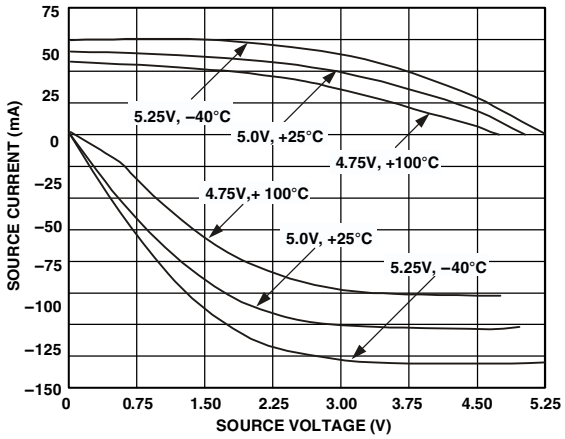

Figure 30. Typical Output Drive Currents (V_{DD} = 5 V)

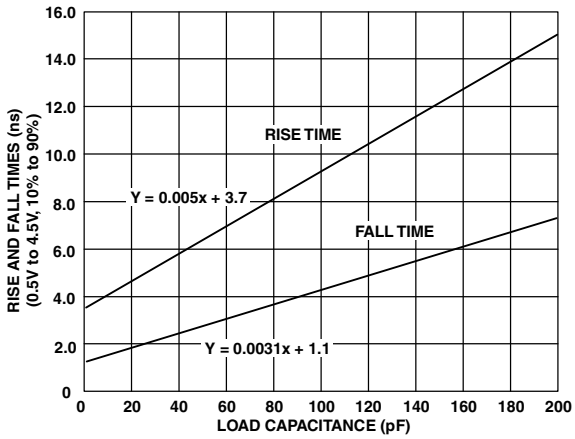

Figure 31. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

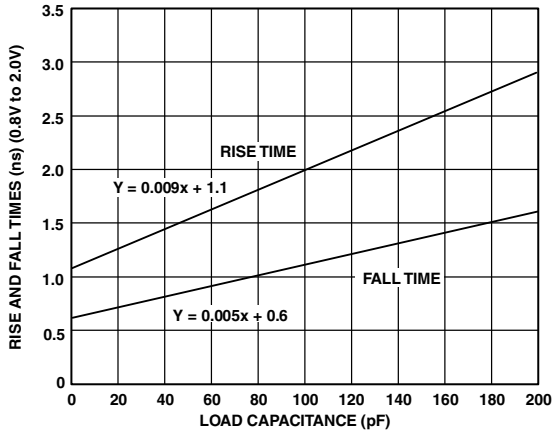

Figure 32. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

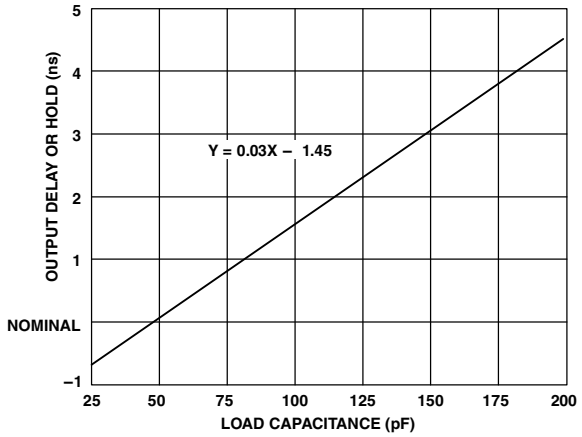

Figure 33. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

225-BALL PBGA PIN CONFIGURATIONS

Table 32. ADSP-21061L 225-Lead Metric PBGA (B-225-2) Pin Assignments

Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number
$\overline{BMS}$	A01	ADDR25	D01	ADDR14	G01	ADDR6	K01	$\overline{EMU}$	N01
ADDR30	A02	ADDR26	D02	ADDR15	G02	ADDR5	K02	TDO	N02
$\overline{DMAR2}$	A03	$\overline{MS2}$	D03	ADDR16	G03	ADDR3	K03	$\overline{IRQ0}$	N03
DT1	A04	ADDR29	D04	ADDR19	G04	ADDR0	K04	$\overline{IRQ1}$	N04
RCLK1	A05	$\overline{DMAR1}$	D05	GND	G05	ICSA	K05	ID2	N05
TCLK0	A06	TFS1	D06	V_{DD}	G06	GND	K06	NC	N06
RCLK0	A07	$\overline{CPA}$	D07	V_{DD}	G07	V_{DD}	K07	NC	N07
ADRCLK	A08	$\overline{HBG}$	D08	V_{DD}	G08	V_{DD}	K08	NC	N08
$\overline{CS}$	A09	$\overline{DMAG2}$	D09	V_{DD}	G09	V_{DD}	K09	NC	N09
CLKIN	A10	$\overline{BR5}$	D10	V_{DD}	G10	GND	K10	NC	N10
PAGE	A11	$\overline{BR1}$	D11	GND	G11	GND	K11	NC	N11
$\overline{BR3}$	A12	DATA40	D12	DATA22	G12	DATA8	K12	NC	N12
DATA47	A13	DATA37	D13	DATA25	G13	DATA11	K13	NC	N13
DATA44	A14	DATA35	D14	DATA24	G14	DATA13	K14	DATA1	N14
DATA42	A15	DATA34	D15	DATA23	G15	DATA14	K15	DATA3	N15
$\overline{MS0}$	B01	ADDR21	E01	ADDR12	H01	ADDR2	L01	$\overline{TRST}$	P01
$\overline{SW}$	B02	ADDR22	E02	ADDR11	H02	ADDR1	L02	TMS	P02
ADDR31	B03	ADDR24	E03	ADDR13	H03	FLAG0	L03	EBOOT	P03
$\overline{HBR}$	B04	ADDR27	E04	ADDR10	H04	FLAG3	L04	ID0	P04
DR1	B05	GND	E05	GND	H05	RPBA	L05	NC	P05
DT0	B06	GND	E06	V_{DD}	H06	GND	L06	NC	P06
DR0	B07	GND	E07	V_{DD}	H07	GND	L07	NC	P07
REDY	B08	GND	E08	V_{DD}	H08	GND	L08	NC	P08
$\overline{RD}$	B09	GND	E09	V_{DD}	H09	GND	L09	NC	P09
ACK	B10	GND	E10	V_{DD}	H10	GND	L10	NC	P10
$\overline{BR6}$	B11	NC	E11	GND	H11	NC	L11	NC	P11
$\overline{BR2}$	B12	DATA33	E12	DATA18	H12	DATA4	L12	NC	P12
DATA45	B13	DATA30	E13	DATA19	H13	DATA7	L13	NC	P13
DATA43	B14	DATA32	E14	DATA21	H14	DATA9	L14	NC	P14
DATA39	B15	DATA31	E15	DATA20	H15	DATA10	L15	DATA0	P15
$\overline{MS3}$	C01	ADDR17	F01	ADDR9	J01	FLAG1	M01	TCK	R01
$\overline{MS1}$	C02	ADDR18	F02	ADDR8	J02	FLAG2	M02	$\overline{IRQ2}$	R02
ADDR28	C03	ADDR20	F03	ADDR7	J03	TIMEXP	M03	$\overline{RESET}$	R03
$\overline{SBTS}$	C04	ADDR23	F04	ADDR4	J04	TDI	M04	ID1	R04
TCLK1	C05	GND	F05	GND	J05	LBOOT (GND)	M05	NC	R05
RFS1	C06	GND	F06	V_{DD}	J06	NC	M06	NC	R06
TFS0	C07	V_{DD}	F07	V_{DD}	J07	NC	M07	NC	R07
RFS0	C08	V_{DD}	F08	V_{DD}	J08	NC	M08	NC	R08
$\overline{WR}$	C09	V_{DD}	F09	V_{DD}	J09	NC	M09	NC	R09
$\overline{DMAG1}$	C10	GND	F10	V_{DD}	J10	NC	M10	NC	R10
$\overline{BR4}$	C11	GND	F11	GND	J11	NC	M11	NC	R11
DATA46	C12	DATA29	F12	DATA12	J12	NC	M12	NC	R12

240-LEAD MQFP PIN CONFIGURATIONS

Table 33. ADSP-21061 MQFP/ED (SP-240); ADSP-21061L MQFP (S-240) Pin Assignments

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	NC	201
$\overline{TRST}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	NC	202
V_{DD}	3	$\overline{GND}$	43	DR0	83	DATA39	123	DATA12	163	NC	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{EMU}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	NC	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	NC	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	NC	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	NC	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	NC	210
FLAG0	11	ADDR26	51	$\overline{HBG}$	91	DATA34	131	DATA6	171	NC	211
GND	12	ADDR27	52	$\overline{CS}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{RD}$	93	V_{DD}	133	DATA5	173	NC	213
ADDR1	14	$\overline{MS3}$	54	$\overline{WR}$	94	V_{DD}	134	DATA4	174	NC	214
V_{DD}	15	$\overline{MS2}$	55	GND	95	GND	135	DATA3	175	NC	215
ADDR2	16	$\overline{MS1}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	NC	216
ADDR3	17	$\overline{MS0}$	57	GND	97	DATA31	137	DATA2	177	NC	217
ADDR4	18	$\overline{SW}$	58	CLKIN	98	DATA30	138	DATA1	178	NC	218
GND	19	$\overline{BMS}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{DMAG2}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{DMAG1}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	NC	182	NC	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	NC	183	NC	223
ADDR8	24	ADDR29	64	$\overline{BR6}$	104	V_{DD}	144	NC	184	NC	224
ADDR9	25	ADDR30	65	$\overline{BR5}$	105	DATA26	145	NC	185	NC	225
ADDR10	26	ADDR31	66	$\overline{BR4}$	106	DATA25	146	NC	186	NC	226
GND	27	GND	67	$\overline{BR3}$	107	DATA24	147	NC	187	NC	227
ADDR11	28	$\overline{SBTS}$	68	$\overline{BR2}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{DMAR2}$	69	$\overline{BR1}$	109	DATA23	149	NC	189	ID2	229
ADDR13	30	$\overline{DMAR1}$	70	GND	110	DATA22	150	NC	190	ID1	230
V_{DD}	31	$\overline{HBR}$	71	V_{DD}	111	DATA21	151	NC	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	NC	192	LBOOT (GND)	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	NC	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	NC	194	$\overline{RESET}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{IRQ2}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{IRQ1}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	NC	198	$\overline{IRQ0}$	238
V_{DD}	39	$\overline{CPA}$	79	DATA42	119	DATA15	159	NC	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	NC	200	TMS	240