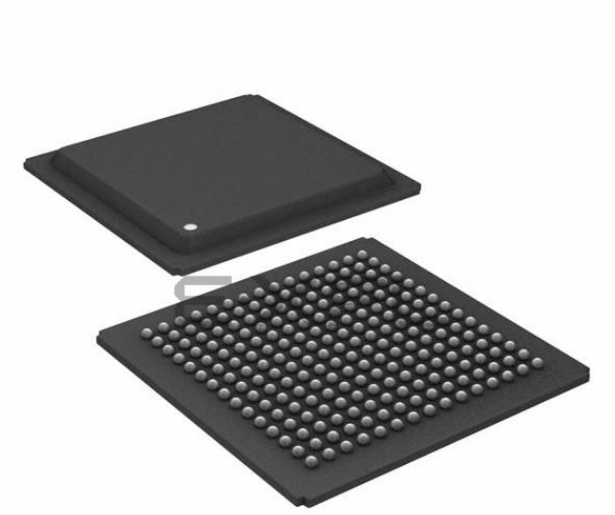

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Floating Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	225-BBGA
Supplier Device Package	225-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21061lkb-160

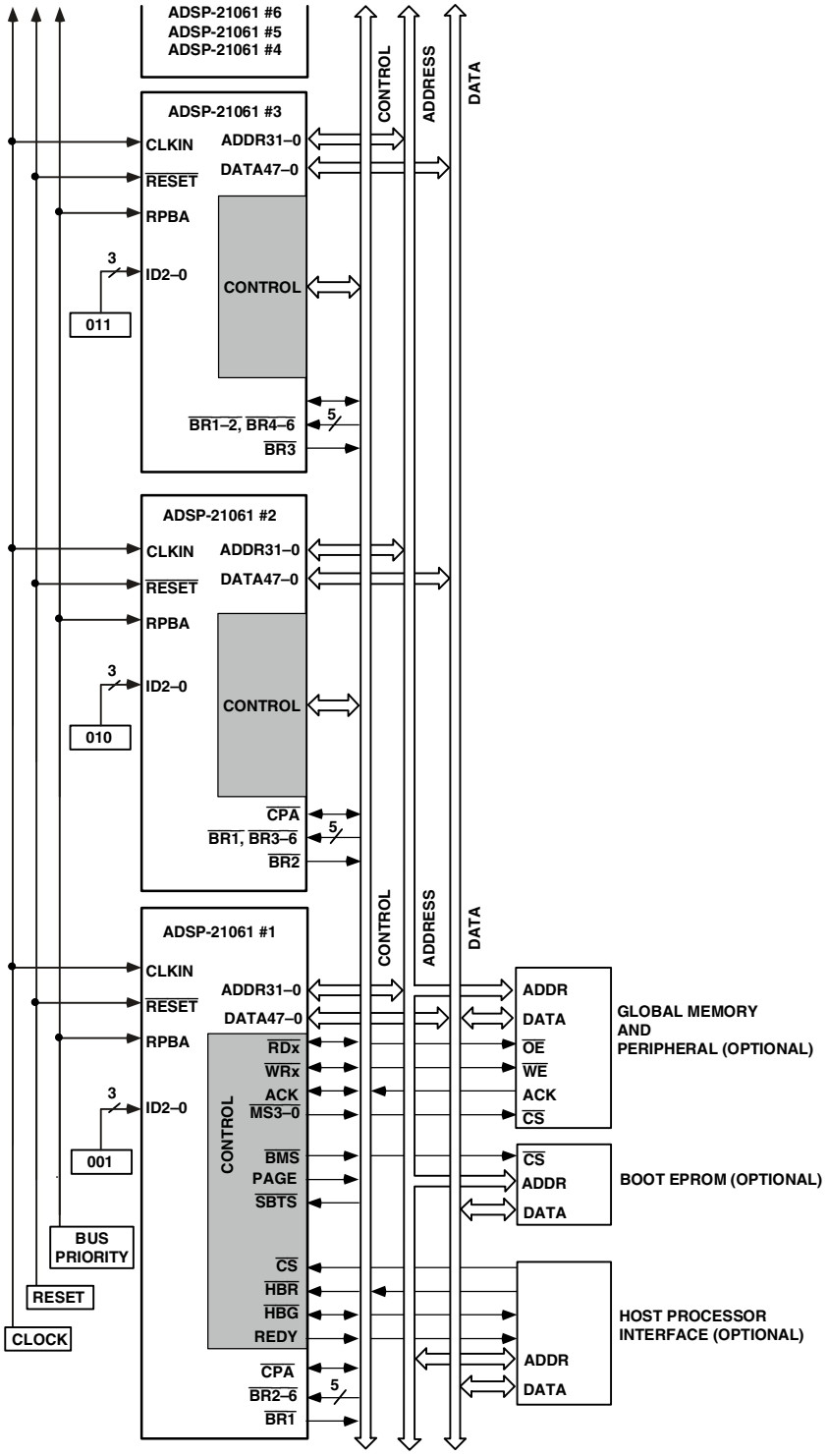

Figure 3. Shared Memory Multiprocessing System

DMA transfers can occur between the ADSP-21061's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21061's internal memory and its serial ports.

DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Program Booting

The internal memory of the ADSP-21061 can be booted at system power-up from either an 8-bit EPROM, or a host processor. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (boot memory select), EBOOT (EPROM boot), and LBOOT (host boot) pins. 32-bit and 16-bit host processors can be used for booting.

PORTING CODE FROM THE ADSP-21060 OR ADSP-21062

The ADSP-21061 is pin compatible with the ADSP-21060/ADSP-21061/ADSP-21062 processors. The ADSP-21061 pins that correspond to the link port pins of the ADSP-21060/ADSP-21062 are no-connects.

The ADSP-21061 is object code compatible with the ADSP-21060/ADSP-21062 processors except for the following functional elements:

- The ADSP-21061 memory is organized into two blocks with eight columns that are 4k deep per block. The ADSP-21060/ADSP-21062 memory has 16 columns per block.
- Link port functions are not available.
- Handshake external port DMA pins DMAR2 and DMAG2 are assigned to external port DMA Channel 6 instead of Channel 8.
- 2-D DMA capability of the SPORT is not available.
- The modify registers in SPORT DMA are not programmable.

On the ADSP-21061, Block 0 starts at the beginning of internal memory, normal word address 0x0002 0000. Block 1 starts at the end of Block 0, with contiguous addresses. The remaining addresses in internal memory are divided into blocks that alias into Block 1. This allows any code or data stored in Block 1 on the ADSP-21062 to retain the same addresses on the ADSP- 21061—these addresses will alias into the actual Block 1 of each processor.

If you develop your application using the ADSP-21062, but will migrate to the ADSP-21061, use only the first eight columns of each memory bank. Limit your application to 8k of instructions or up to 16k of data in each bank of the ADSP-21062, or any combination of instructions or data that does not exceed the memory bank.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on “ezkit” or “ezextender”.

EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user’s PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

ADSP-21061 SPECIFICATIONS

OPERATING CONDITIONS (5 V)

Parameter	Description	K Grade			Unit
		Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
T_{CASE}	Case Operating Temperature	0		85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0		V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2		V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5		+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (5 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	4.1		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" on Page 44 for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups:DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

ADSP-21061L SPECIFICATIONS

OPERATING CONDITIONS (3.3 V)

Parameter	Description	A Grade			K Grade			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	3.15	3.3	3.45	3.15	3.3	3.45	V
T_{CASE}	Case Operating Temperature	–40		+85	0		+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0		V_{DD} + 0.5	2.0		V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2		V_{DD} + 0.5	2.2		V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5		+0.8	–0.5		+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1,2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" on Page 45 for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

INTERNAL POWER DISSIPATION (3.3 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios:

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = power\ consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 25 ns, V_{DD} = Max	480	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	535	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 25 ns, V_{DD} = Max	380	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	425	mA
$I_{DDINLOW}$ Supply Current (Internal)[3]	t_{CK} = 25 ns, V_{DD} = Max	220	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	245	mA
I_{DDIDLE} Supply Current (Idle)[4]	V_{DD} = Max	180	mA
I_{DDIDLE} Supply Current (Idle)[5]	V_{DD} = Max	50	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[4] Idle denotes ADSP-21061L state during execution of IDLE instruction.

[5] Idle16 denotes ADSP-21061L state during execution of IDLE16 instruction.

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:
$P_{INT} = I_{DDIN} \times V_{DD}$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- —the number of output pins that switch during each cycle (O)
- —the maximum frequency at which they can switch (f)
- —their load capacitance (C)
- —their voltage swing (V_{DD})

and is calculated by:

$$PEXT = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128k × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

Table 5. External Power Calculations

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	—	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	—	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W

P_{EXT} = 0.074 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:
$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 3.3\ V)$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Interrupts

Table 9. Interrupts

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	18 + 3DT/4		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold Before CLKIN High[1]		12 + 3DT/4	ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

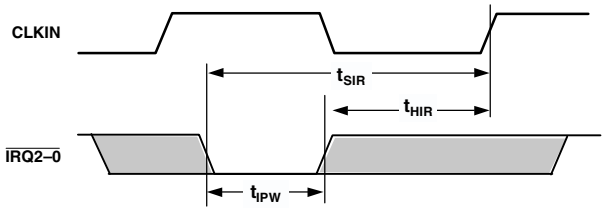

Figure 11. Interrupts

Timer

Table 10. Timer

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP		15	ns

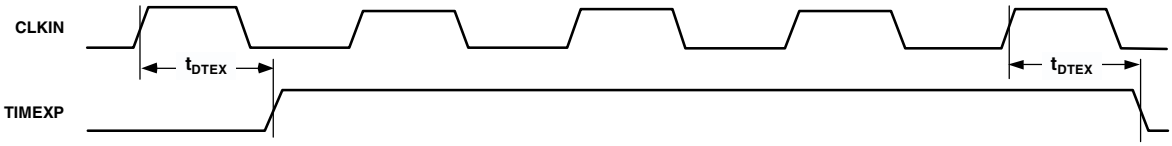

Figure 12. Timer

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 12. Memory Read—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address, Selects[3]	0.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 4]		15 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DRHA}	Address, Selects Hold After $\overline{RD}$ High	0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[2]	2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup Before ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data delay/setup: user must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] Data hold: user must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}. See Example System Hold Time Calculation on Page 43 for the calculation of hold times given capacitive and dc loads.
[4] ACK delay/setup: user must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} (Table 13 on Page 25) for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).

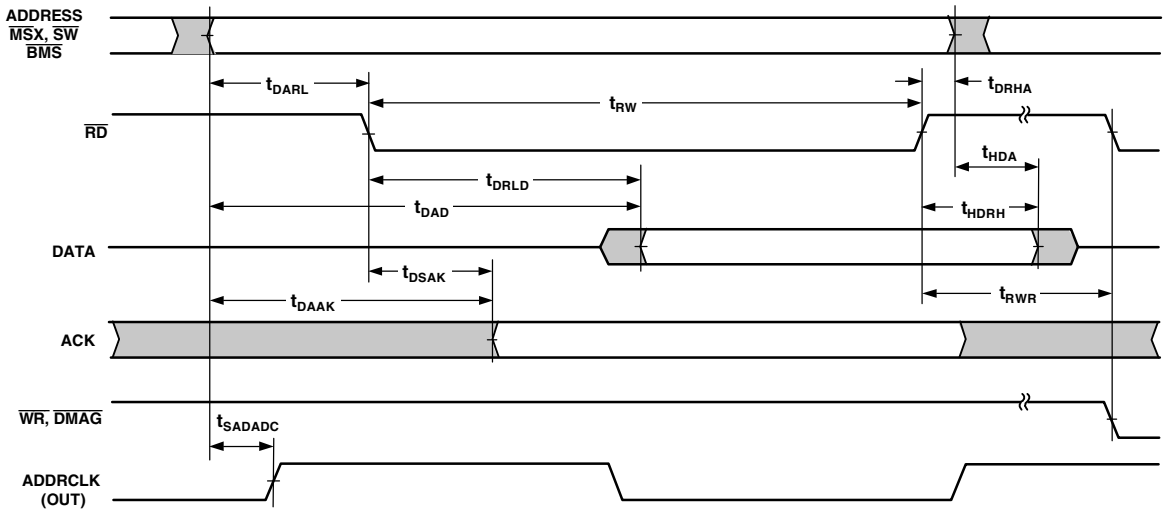

Figure 14. Memory Read—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-21061 (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read—Bus Master on Page 24 and Memory Write—Bus Master on Page 25). When accessing a slave ADSP-21061, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave on Page 28). The slave ADSP-21061 must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 14. Synchronous Read/Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN (50 MHz, t_{CK} = 20 ns)[1]	2 + DT/8 1.5 + DT/8		ns
t_{HSDATI}	Data Hold After CLKIN	3.5 – DT/8		ns
t_{DAAK}	ACK Delay After Address, Selects[2, 3]		15 + 7DT/8 + W	ns
t_{SACKC}	ACK Setup Before CLKIN[3]	6.5 + DT/4		ns
t_{HACK}	ACK Hold After CLKIN	–1 – DT/4		ns
Switching Characteristics				
t_{DADRO}	Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[2]		6.5 – DT/8	ns
t_{HADRO}	Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	–1 – DT/8		ns
t_{DPGC}	PAGE Delay After CLKIN	9 + DT/8	16 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	–1.5 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN (50 MHz, t_{CK} = 20 ns)	–2.5 – 3DT/16 –1.5 – 3DT/16	4 – 3DT/16 4 – 3DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	8 + DT/4	12 + DT/4	ns
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[4]	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay After CLKIN	4 + DT/8	10 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		ns

[1] This specification applies to the ADSP-21061KS-200 (5 V, 50 MHz) operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] ACK delay/setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).
[4] See Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21061s ($\overline{BRx}$) or a host processor, both synchronous and asynchronous ($\overline{HBR}$, $\overline{HBG}$).

Table 16. Multiprocessor Bus Request and Host Bus Request

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		20 + 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[2]		14 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN High		6 + DT/2	ns
t_{SBRI}	$\overline{BRx}$, $\overline{CPA}$ Setup Before CLKIN[3]	13 + DT/2		ns
t_{HBRI}	$\overline{BRx}$, $\overline{CPA}$ Hold After CLKIN High		6 + DT/2	ns
t_{SRPBAI}	RPBA Setup Before CLKIN	20 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold After CLKIN		12 + 3DT/4	ns
Switching Characteristics				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	–2 – DT/8		ns
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN		5.5 – DT/8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN	–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay After CLKIN[4]		6.5 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable After CLKIN	–2 – DT/8	4.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[5, 6]		8	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[5, 7]	44 + 27DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[5]		10	ns

[1] For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-21061" section in the *ADSP-2106x SHARC User's Manual*.

[2] Only required for recognition in the current cycle.

[3] $\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

[4] For the ADSP-21061L (3.3 V), this specification is 8.5 – DT/8 ns max.

[5] (O/D) = open drain, (A/D) = active drive.

[6] For the ADSP-21061L (3.3 V), this specification is 12 ns max.

[7] For the ADSP-21061L (3.3 V), this specification is 40 + 23DT/16 ns min.

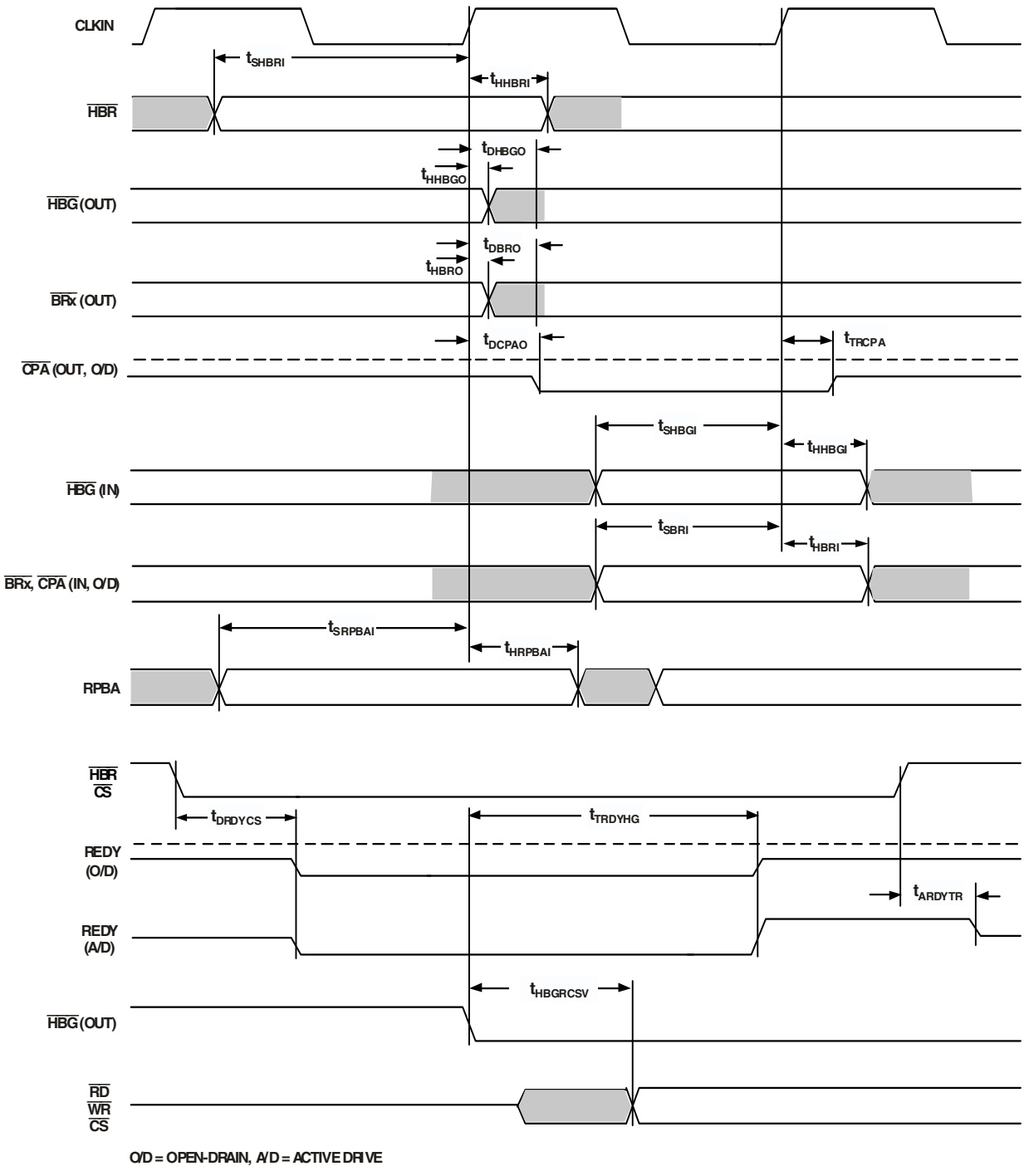

Figure 18. Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write—Host to ADSP-21061

Use these specifications for asynchronous host processor accesses of an ADSP-21061, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21061, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21061's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Table 17. Read Cycle

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low[1]	0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$	0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low[2]		10	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	45 + DT		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2	8	ns

[1] Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-21061" section in the *ADSP-2106x SHARC User's Manual*.
[2] For the ADSP-21061L (3.3 V), this specification is 13.5 ns max.

Table 18. Write Cycle

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2		ns
t_{WWRL}	$\overline{WR}$ Low Width	8		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	3		ns
	50 MHz, t_{CK} = 20 ns[1]	2.5		
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low[2]		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write	15		ns
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKIN	1 + 7DT/16	8 + 7DT/16	ns

[1] This specification applies to the ADSP-21061KS-200 (5 V, 50 MHz) operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.
[2] For the ADSP-21061L (3.3 V), this specification is 13.5 ns max.

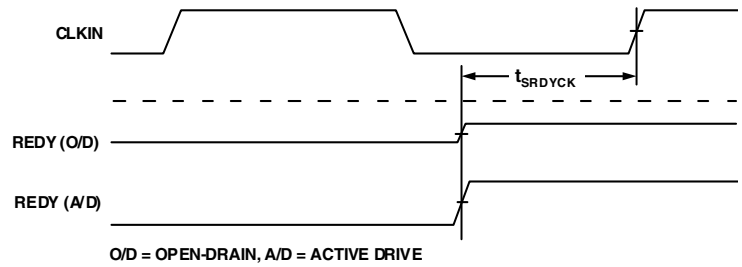

Figure 19. Synchronous REDY Timing

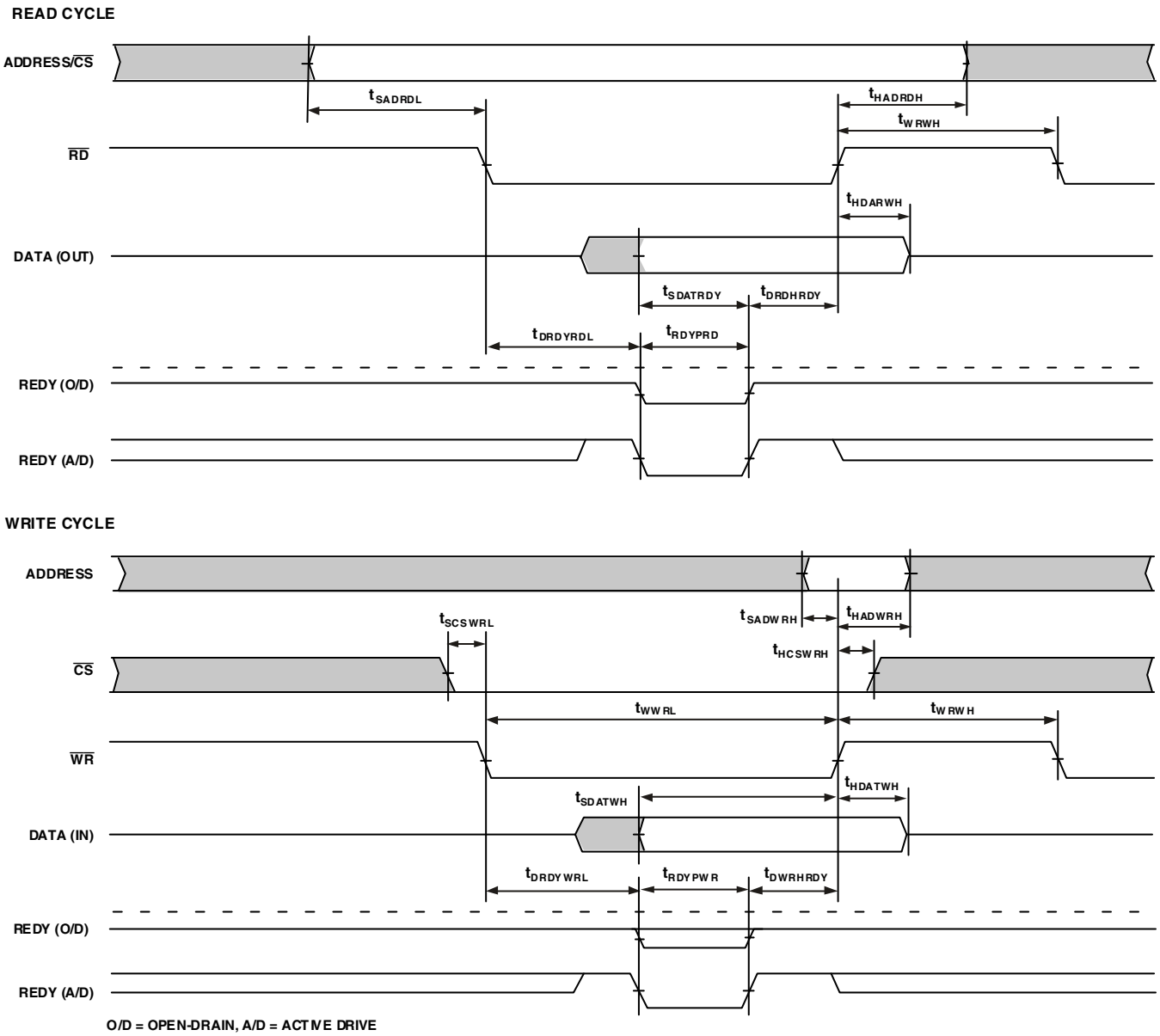

Figure 20. Asynchronous Read/Write—Host to ADSP-21061

Three-State Timing—Bus Master, Bus Slave, HBR, SBTS

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the SBTS pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the SBTS pin.

Table 19. Three-State Timing—Bus Master, Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{STSCK}	SBTS Setup Before CLKIN	12 + DT/2		ns
t_{HTSCK}	SBTS Hold Before CLKIN		6 + DT/2	ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN	–1 – DT/8		ns
t_{MIENS}	Strobes Enable After CLKIN[1]	–1.5 – DT/8		ns
t_{MIENHG}	HBG Enable After CLKIN	–1.5 – DT/8		ns
t_{MITRA}	Address/Select Disable After CLKIN		0 – DT/4	ns
t_{MITRS}	Strobes Disable After CLKIN[1]		1.5 – DT/4	ns
t_{MITRHG}	HBG Disable After CLKIN		2.0 – DT/4	ns
t_{DATEN}	Data Enable After CLKIN[2]	9 + 5DT/16		ns
t_{DATTR}	Data Disable After CLKIN[2]	0 – DT/8	7 – DT/8	ns
t_{ACKEN}	ACK Enable After CLKIN[2]	7.5 + DT/4		ns
t_{ACKTR}	ACK Disable After CLKIN[2]	–1 – DT/8	6 – DT/8	ns
t_{ADCEN}	ADRCLK Enable After CLKIN	–2 – DT/8		ns
t_{ADCTR}	ADRCLK Disable After CLKIN		8 – DT/4	ns
t_{MTRHBG}	Memory Interface Disable Before HBG Low[3]	0 + DT/8		ns
t_{MENHBG}	Memory Interface Enable After HBG High[3]	19 + DT		ns

[1] Strobes = RD, WR, PAGE, DMAGx, MSx, BMS, SW.
[2] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[3] Memory Interface = Address, RD, WR, MSx, SW, PAGE, DMAGx, and BMS (in EPROM boot mode).

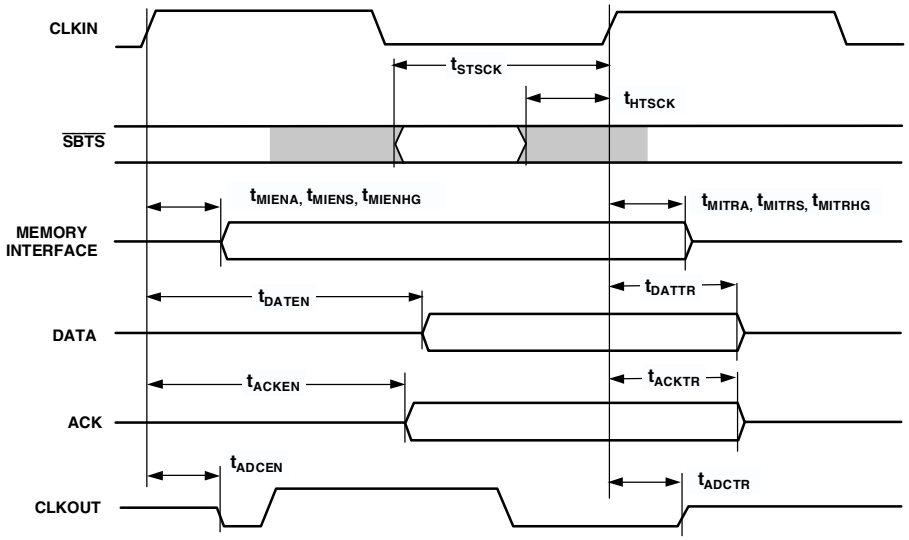

Figure 21. Three-State Timing (Bus Transition Cycle, SBTS Assertion)

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For Handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For External Handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAGx}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, $\overline{\text{SW}}$, PAGE, DATA47–0, and ACK also apply.

Table 20. DMA Handshake

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SDRLC}	$\overline{\text{DMARx}}$ Low Setup Before CLKIN[1]	5		ns
t_{SDRHC}	$\overline{\text{DMARx}}$ High Setup Before CLKIN[1]	5		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)	6		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[2]		10 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMARx}}$ High[2]		16 + 7DT/8	ns
t_{DMARLL}	$\overline{\text{DMARx}}$ Low Edge to Low Edge[3]	23 + 7DT/8		ns
t_{DMARH}	$\overline{\text{DMARx}}$ Width High	6		ns
Switching Characteristics				
t_{DDGL}	$\overline{\text{DMAGx}}$ Low Delay After CLKIN	9 + DT/4	15 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAGx}}$ High Width	6 + 3DT/8		ns
t_{WDGL}	$\overline{\text{DMAGx}}$ Low Width	12 + 5DT/8		ns
t_{HDGC}	$\overline{\text{DMAGx}}$ High Delay After CLKIN	–2 – DT/8	6 – DT/8	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAGx}}$ High[4]	8 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAGx}}$ High[5]	0	7	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DGWRH}	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WR}}$ High	10 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High Before $\overline{\text{DMAGx}}$ High	1 + DT/16	3 + DT/16	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ High	11 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High Before $\overline{\text{DMAGx}}$ High	0	3	ns
t_{DGWR}	$\overline{\text{DMAGx}}$ High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAGx}}$ Low	5 + 3DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAGx}}$ High	17 + DT		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAGx}}$ High[6]	–0.5		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.
[3] For the ADSP-21061L (3.3 V), this specification is 23.5 + 7DT/8 ns min.
[4] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - .25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
[5] See Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.
[6] For the ADSP-21061L (3.3 V), this specification is –1.0 ns min.

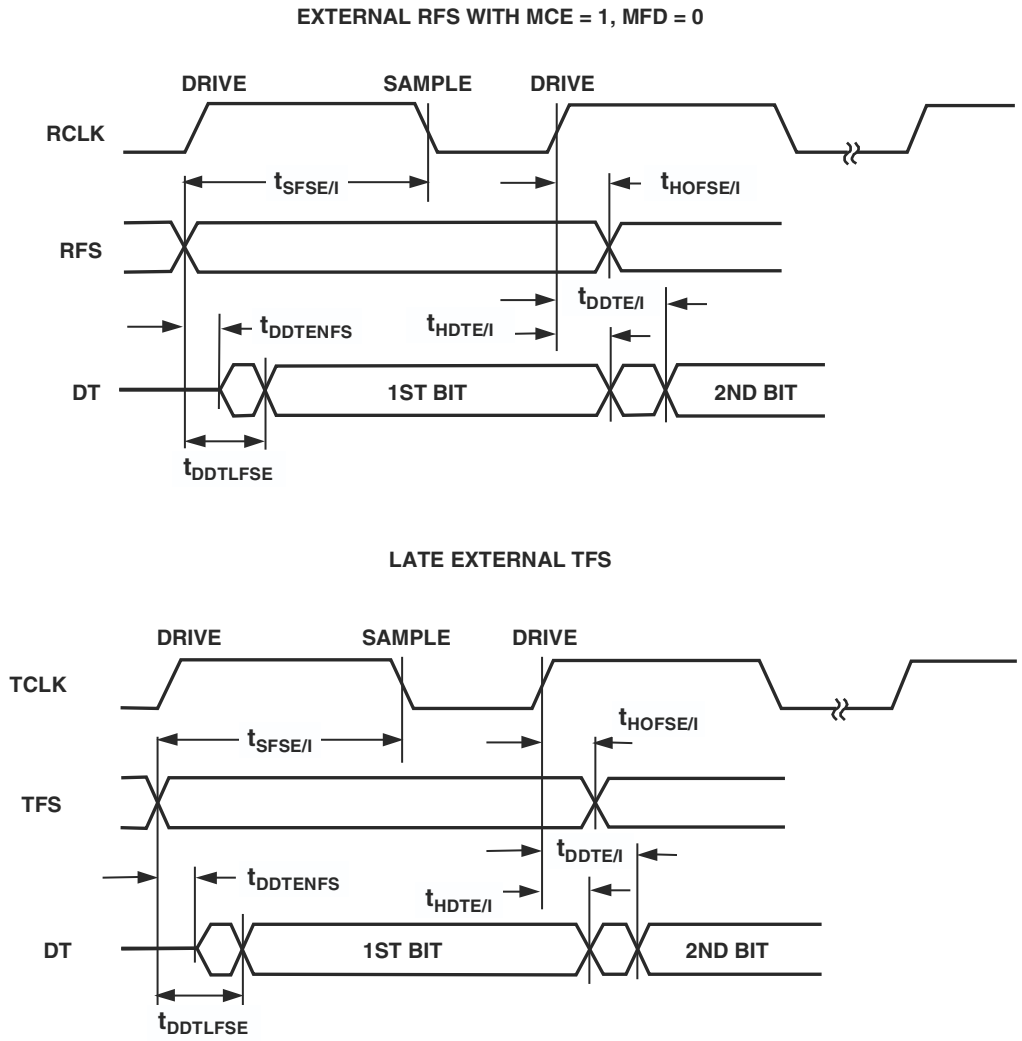

Figure 25. Serial Ports—External Late Frame Sync

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$P_{EXT} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 27. The time $t_{MEASURED}$is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 27). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21061's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

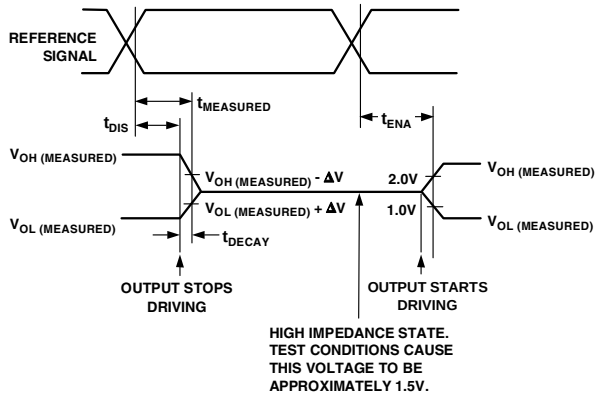

Figure 27. Output Enable/Disable

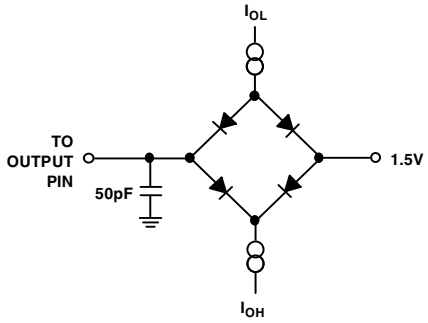

Figure 28. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 29. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Drive Characteristics

Figure 30 through Figure 37 show typical characteristics for the output drivers of the ADSP-21061 (5 V) and ADSP-21061L (3 V). The curves represent the current drive capability and switching behavior of the output drivers as a function of resistive and capacitive loading.

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 28). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 31, Figure 32, Figure 35, and Figure 36 show how output rise time varies with capacitance. Figure 33 and Figure 37 show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of Figure 31, Figure 32, Figure 35, and Figure 36 may not be linear outside the ranges shown.

Input/Output Characteristics (3.3 V)

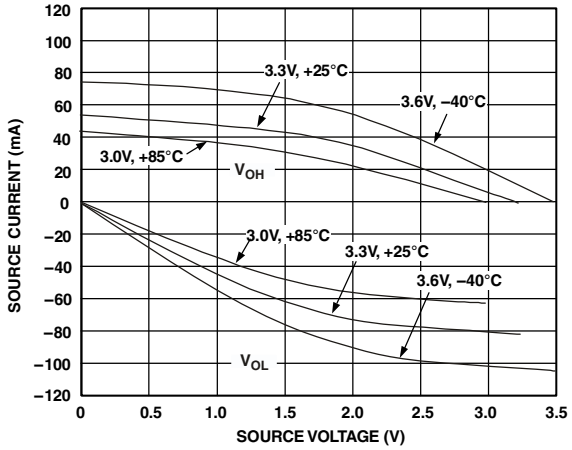

Figure 34. Typical Drive Currents (V_{DD} = 3.3 V)

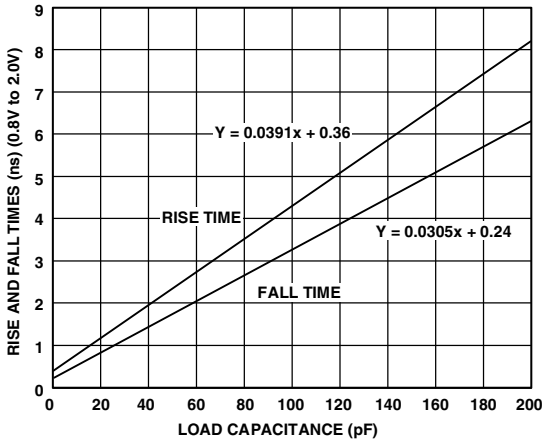

Figure 36. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

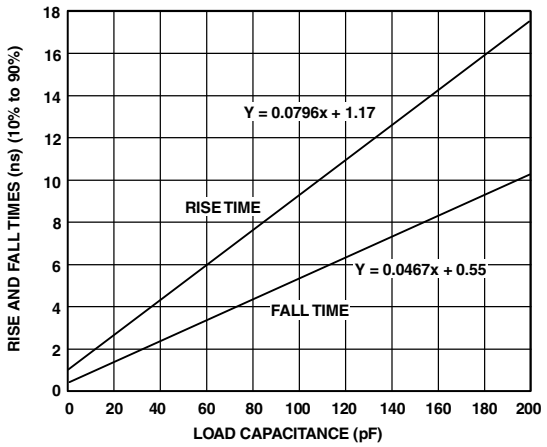

Figure 35. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

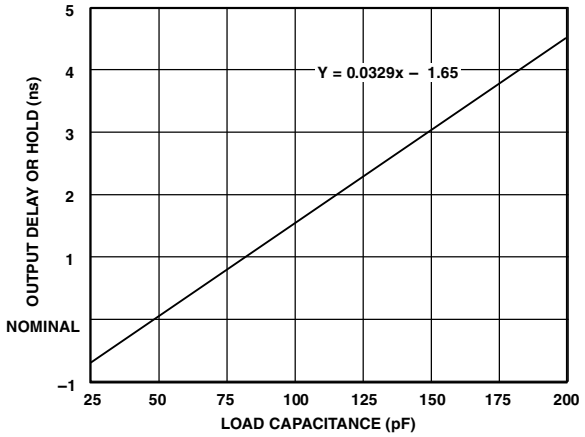

Figure 37. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 3.3 V)

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21061 is available in 240-lead thermally enhanced MQFP package. The top surface of the thermally enhanced MQFP contains a metal slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the metal slug is internally connected to GND through the device substrate.

The ADSP-21061L is available in 240-lead MQFP and 225-ball plastic BGA packages.

All packages are specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} is not exceeded, a heatsink and/or an airflow source may be used. A heat sink should be attached with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD\ \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

T_{AMB} = Ambient temperature °C

PD =Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} =Value from tables below.

Table 29. ADSP-21061 (5 V Thermally Enhanced ED/MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	10	°C/W
	Airflow = 100	9	
	Airflow = 200	8	
	Airflow = 400	7	
	Airflow = 600	6	

Table 30. ADSP-21061L (3.3 V MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.6	°C/W
	Airflow = 100	17.6	
	Airflow = 200	15.6	
	Airflow = 400	13.9	
	Airflow = 600	12.2	

Table 31. ADSP-21061L (3.3 V PBGA Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.0	°C/W
	Airflow = 200	13.6	
	Airflow = 400	11.2	

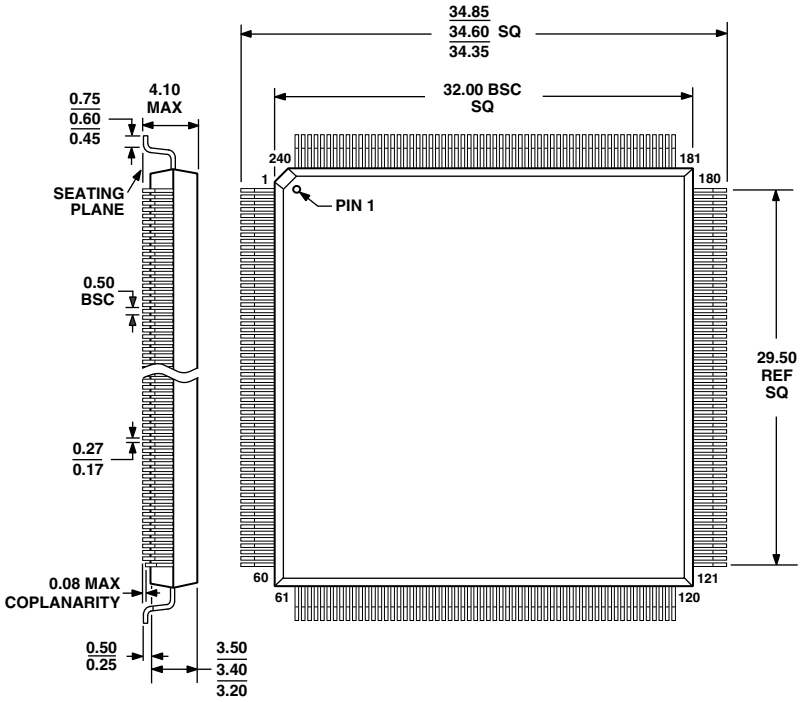

Figure 40. 240-Lead Metric Quad Flat Package, [MQFP] (S-240)

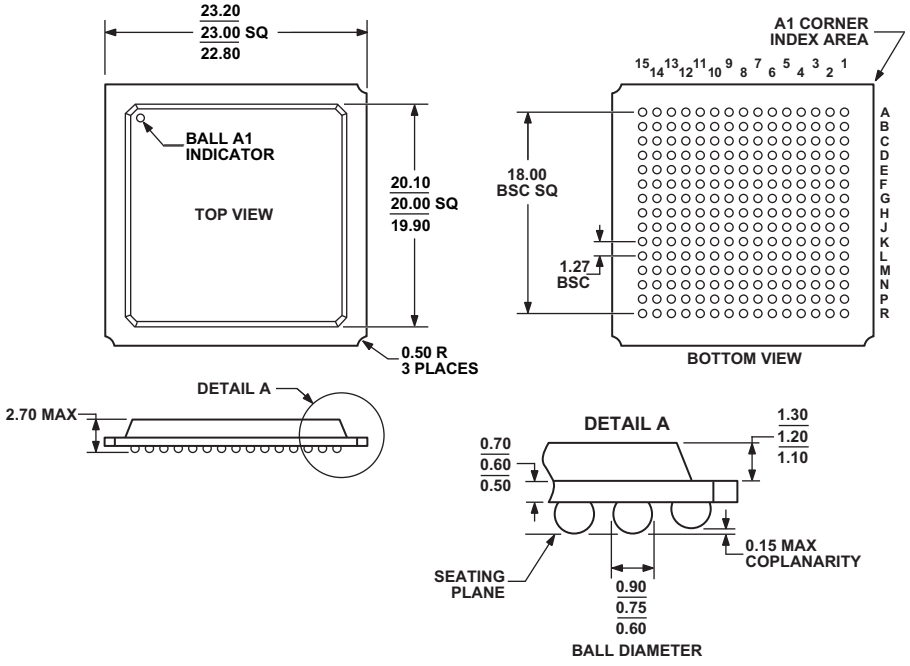

Figure 41. 225-Ball Plastic Ball Grid Array [PBGA] (B-225-2)