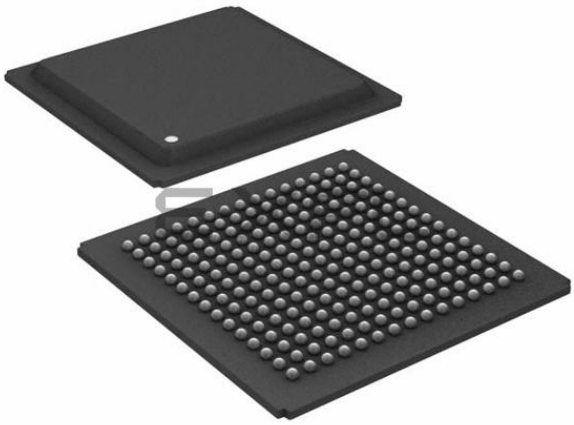

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Floating Point
Interface	Synchronous Serial Port (SSP)
Clock Rate	40MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	3.30V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	225-BBGA
Supplier Device Package	225-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21061lkbz-160

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REVISION HISTORY

5/13—Rev C to Rev D

Updated Development Tools 7

Added Related Signal Chains 8

Removed the ADSP-21061LAS-176, ADSP-21061LKS-160, and ADSP-21061LKS-176 models from Ordering Guide 52

GENERAL NOTE

This data sheet represents production released specifications for the ADSP-21061 (5 V) and ADSP-21061L (3.3 V) processors for 33 MHz, 40 MHz, 44 MHz, and 50 MHz speed grades. The product name“ADSP-21061” is used throughout this data sheet to represent all devices, except where expressly noted.

Single-Cycle Fetch of Instruction and Two Operands

The ADSP-21061 features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (Figure 1 on Page 1). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21061 includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-21061's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21061 contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21061 can conditionally execute a multiply, an add, a subtract, and a branch, all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-21061 processors add the following architectural features to the SHARC family core.

Dual-Ported On-Chip Memory

The ADSP-21061 contains one megabit of on-chip SRAM, organized as two blocks of 0.5M bits each. Each bank has eight 16-bit columns with 4k 16-bit words per column. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21061 memory map).

On the ADSP-21061, the memory can be configured as a maximum of 32k words of 32-bit data, 64k words for 16-bit data, 16k words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 1 megabit. All the memory can be accessed as 16-bit, 32-bit, or 48-bit.

A 16-bit floating-point storage format is supported, which effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-21061's external port.

Off-Chip Memory and Peripherals Interface

The ADSP-21061's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-21061's unified address space. The separate on-chip buses—for program memory, data memory, and I/O—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus. The on-chip Super Harvard Architecture provides three-bus performance, while the off-chip unified address space gives flexibility to the designer.

Addressing of external memory devices is facilitated by on-chip decoding of high order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-21061 provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

Host Processor Interface

The ADSP-21061's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-21061's external port and is memory-mapped into the unified address space. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21061's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-21061, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

DMA Controller

The ADSP-21061's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

Six channels of DMA are available on the ADSP-21061—four via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21061s, memory or I/O transfers). Programs can be downloaded to the ADSP-21061 using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA request/grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Serial Ports

The ADSP-21061 features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of up to 50 Mbps. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports offers TDM multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and key mask features to enhance interprocessor communication.

Multiprocessing

The ADSP-21061 offers powerful features tailored to multiprocessor DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-21061's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21061s and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 500 Mbps over the external port. Broadcast writes allow simultaneous transmission of data to all ADSP-21061s and can be used to implement reflective semaphores.

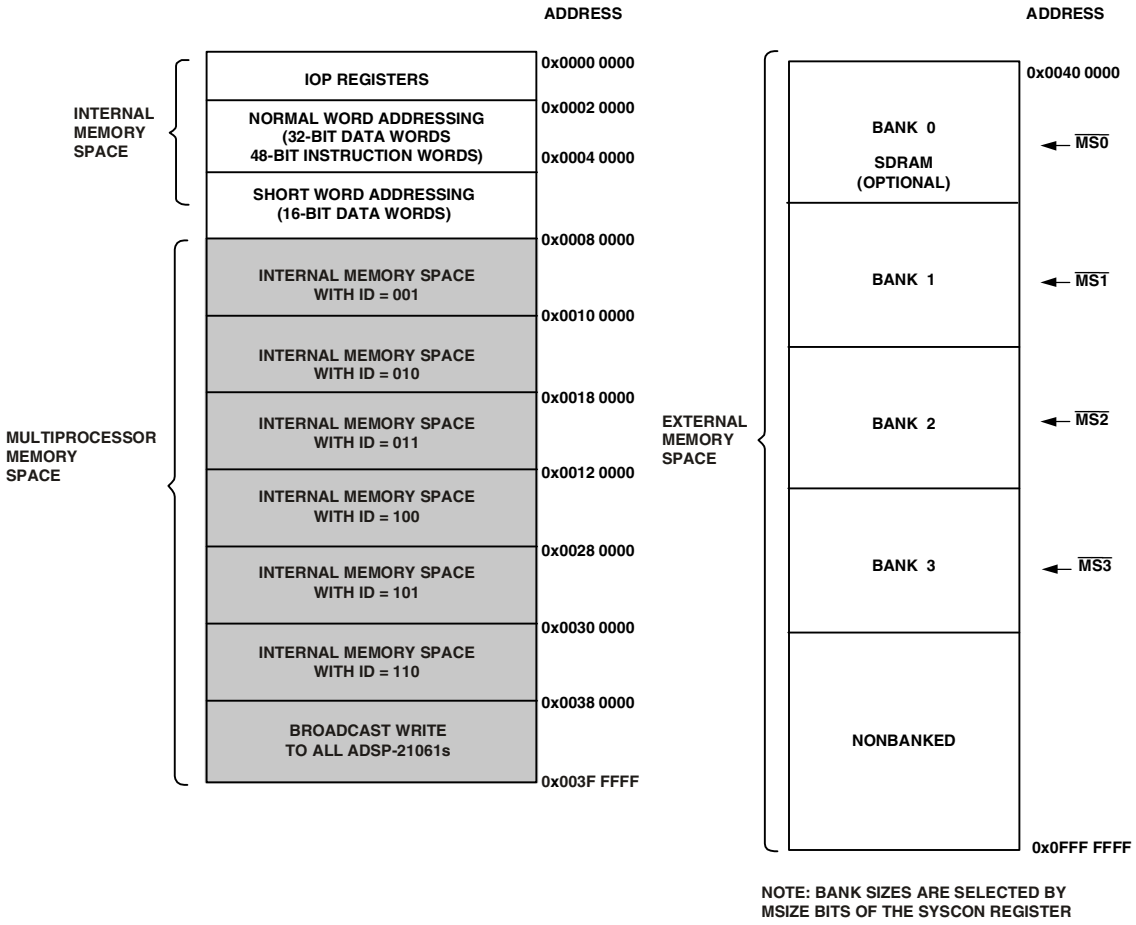

Figure 4. Memory Map

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, TDI, TDO, and GND signals be made accessible on the target system via a 14-pin connector (a 2-row, 7-pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the farthest device sharing the EZ-ICE JTAG pin should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

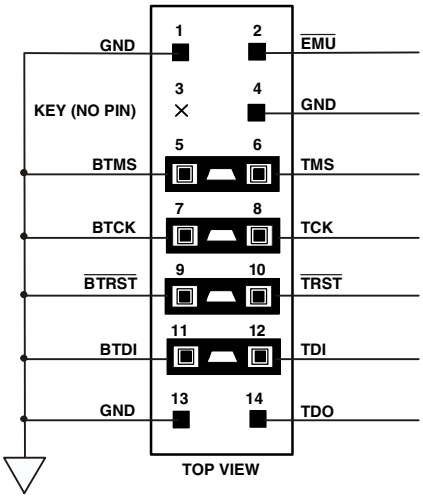

Figure 5. Target Board Connector For ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inches in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec. The BTMS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing.

When the connector is not being used for emulation, place jumpers between the Bxxx pins and the xxx pins as shown in Figure 5. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted (pulsed low) after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, and 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as shown in Table 3.

Table 3. Core Instruction Rate/CLKIN Ratio Selection

Signal	Termination
TMS	Driven Through 22 Ω Resistor (16 mA Driver)
TCK	Driven at 10 MHz Through 22 Ω Resistor (16 mA Driver)
$\overline{\text{TRST}}$[1]	Active Low Driven Through 22 Ω Resistor (16 mA Driver) (Pulled Up by On-Chip 20 kΩ Resistor)
TDI	Driven by 22 Ω Resistor (16 mA Driver)
TDO	One TTL Load, Split Termination (160/220)
CLKIN	One TTL Load, Split Termination (160/220)
$\overline{\text{EMU}}$	Active Low, 4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP)

[1] $\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software startup. After software startup, is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-21061 processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN, and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-21061s (more than eight) in your system, then treat them as a "clock tree" using multiple drivers to minimize skew. (See Figure 7 below and "JTAG Clock Tree" and "Clock Distribution" in the "High Frequency Design Considerations" section of the *ADSP-2106x SHARC User's Manual*.)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$, and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

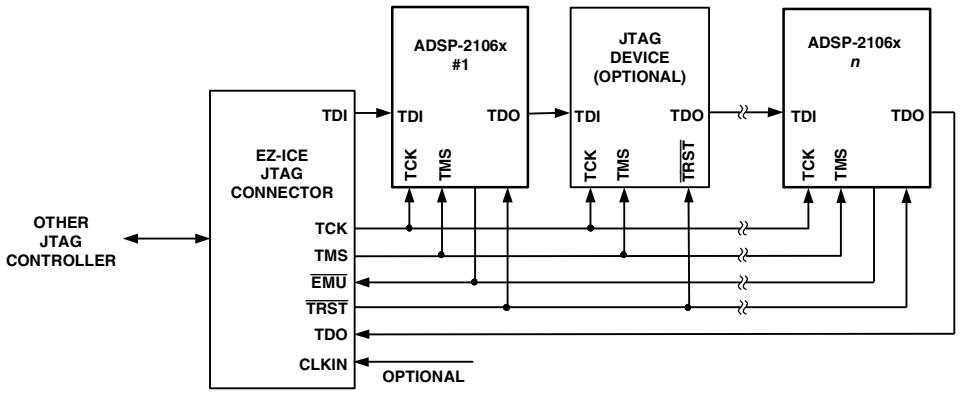

Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

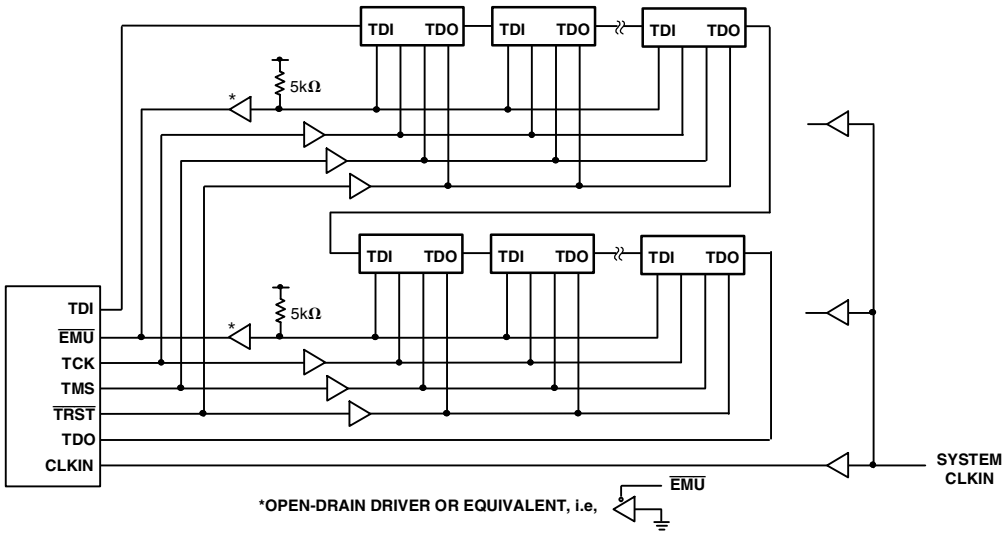

Figure 7. JTAG Clock Tree for Multiple ADSP-2106x Systems

ADSP-21061 SPECIFICATIONS

OPERATING CONDITIONS (5 V)

Parameter	Description	K Grade			Unit
		Min	Nom	Max	
V_{DD}	Supply Voltage	4.75	5.0	5.25	V
T_{CASE}	Case Operating Temperature	0		85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0		V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2		V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5		+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (5 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	4.1		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" on Page 44 for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups:DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

ADSP-21061L SPECIFICATIONS

OPERATING CONDITIONS (3.3 V)

Parameter	Description	A Grade			K Grade			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage	3.15	3.3	3.45	3.15	3.3	3.45	V
T_{CASE}	Case Operating Temperature	–40		+85	0		+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0		V_{DD} + 0.5	2.0		V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2		V_{DD} + 0.5	2.2		V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5		+0.8	–0.5		+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1,2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" on Page 45 for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

INTERNAL POWER DISSIPATION (3.3 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios:

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = power\ consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 25 ns, V_{DD} = Max	480	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	535	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 25 ns, V_{DD} = Max	380	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	425	mA
$I_{DDINLOW}$ Supply Current (Internal)[3]	t_{CK} = 25 ns, V_{DD} = Max	220	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	245	mA
I_{DDIDLE} Supply Current (Idle)[4]	V_{DD} = Max	180	mA
I_{DDIDLE} Supply Current (Idle)[5]	V_{DD} = Max	50	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.

[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[3] $I_{DDINLOW}$ is a composite average based on a range of low activity code.

[4] Idle denotes ADSP-21061L state during execution of IDLE instruction.

[5] Idle16 denotes ADSP-21061L state during execution of IDLE16 instruction.

Clock Input

Table 7. Clock Input

Parameter		ADSP-21061 50 MHz, 5 V Min	ADSP-21061 50 MHz, 5 V Max	ADSP-21061L 44 MHz, 3.3 V Min	ADSP-21061L 44 MHz, 3.3 V Max	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Min	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Max	ADSP-21061 33 MHz, 5 V Min	ADSP-21061 33 MHz, 5 V Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	20	100	22.5	100	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		7		7		ns
t_{CKH}	CLKIN Width High	5		5		5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns

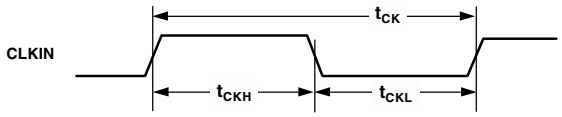

Figure 9. Clock Input

Reset

Table 8. Reset

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including startup time of external clock oscillator).

[2] Only required if multiple ADSP-21061s must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21061s communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

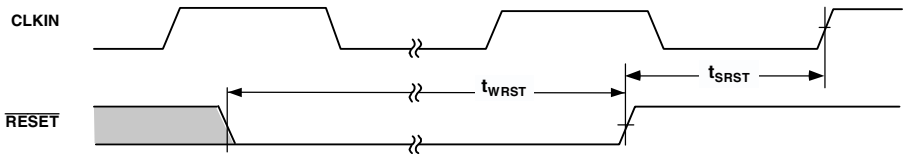

Figure 10. Reset

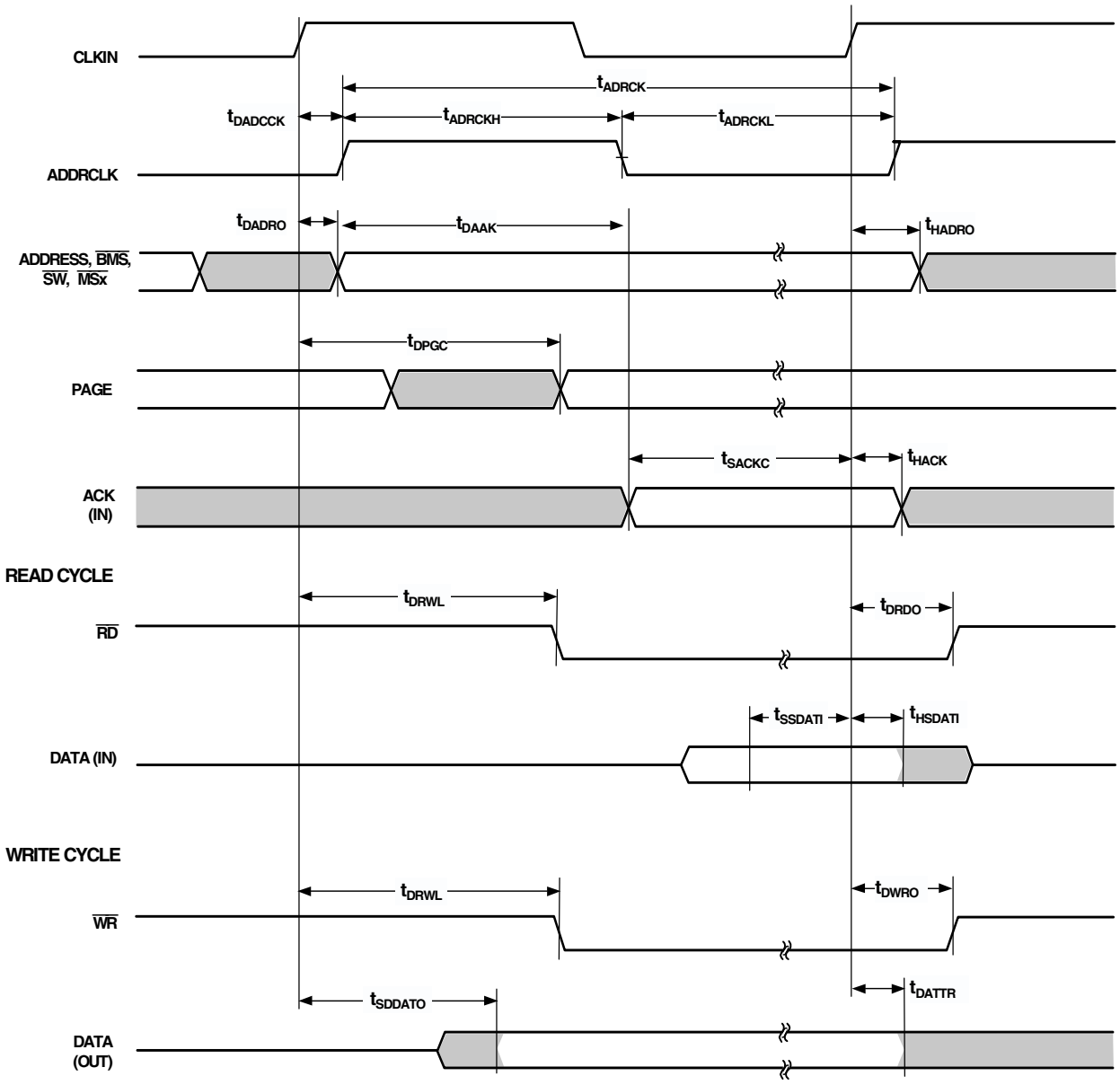

Figure 16. Synchronous Read/Write—Bus Master

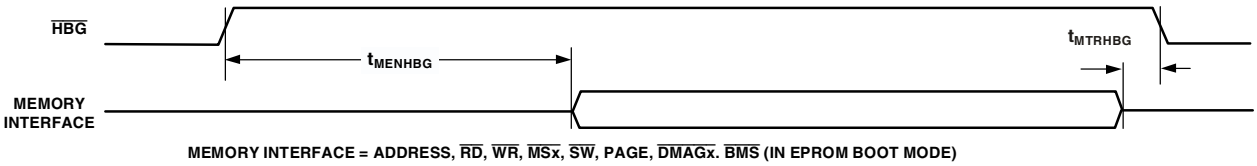

Figure 22. Three-State Timing (Bus Transition Cycle, SBTS Assertion)

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For Handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For External Handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAGx}}$ signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, $\overline{\text{SW}}$, PAGE, DATA47–0, and ACK also apply.

Table 20. DMA Handshake

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SDRLC}	$\overline{\text{DMARx}}$ Low Setup Before CLKIN[1]	5		ns
t_{SDRHC}	$\overline{\text{DMARx}}$ High Setup Before CLKIN[1]	5		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)	6		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[2]		10 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMARx}}$ High[2]		16 + 7DT/8	ns
t_{DMARLL}	$\overline{\text{DMARx}}$ Low Edge to Low Edge[3]	23 + 7DT/8		ns
t_{DMARH}	$\overline{\text{DMARx}}$ Width High	6		ns
Switching Characteristics				
t_{DDGL}	$\overline{\text{DMAGx}}$ Low Delay After CLKIN	9 + DT/4	15 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAGx}}$ High Width	6 + 3DT/8		ns
t_{WDGL}	$\overline{\text{DMAGx}}$ Low Width	12 + 5DT/8		ns
t_{HDGC}	$\overline{\text{DMAGx}}$ High Delay After CLKIN	–2 – DT/8	6 – DT/8	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAGx}}$ High[4]	8 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAGx}}$ High[5]	0	7	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DGWRH}	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WR}}$ High	10 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High Before $\overline{\text{DMAGx}}$ High	1 + DT/16	3 + DT/16	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ High	11 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High Before $\overline{\text{DMAGx}}$ High	0	3	ns
t_{DGWR}	$\overline{\text{DMAGx}}$ High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAGx}}$ Low	5 + 3DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAGx}}$ High	17 + DT		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAGx}}$ High[6]	–0.5		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.
[3] For the ADSP-21061L (3.3 V), this specification is 23.5 + 7DT/8 ns min.
[4] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - .25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
[5] See Example System Hold Time Calculation on Page 43 for calculation of hold times given capacitive and dc loads.
[6] For the ADSP-21061L (3.3 V), this specification is –1.0 ns min.

Table 25. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width	$t_{SCLK}/2 - 1.5$	$t_{SCLK}/2 + 1.5$	ns

[1] Referenced to drive edge.

Table 26. Serial Ports—Enable and Three-State

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1, 2]	4.5		ns
t_{DDTTE}	Data Disable from External TCLK[1]		10.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1]		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		22 + 3DT/8	ns
t_{DPTR}	SPORT Disable After CLKIN		17	ns

[1] Referenced to drive edge.
[2] For the ADSP-21061L (3.3 V), this specification is 3.5 ns min.

Table 27. Serial Ports—External Late Frame Sync

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1]		12	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	3.5		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

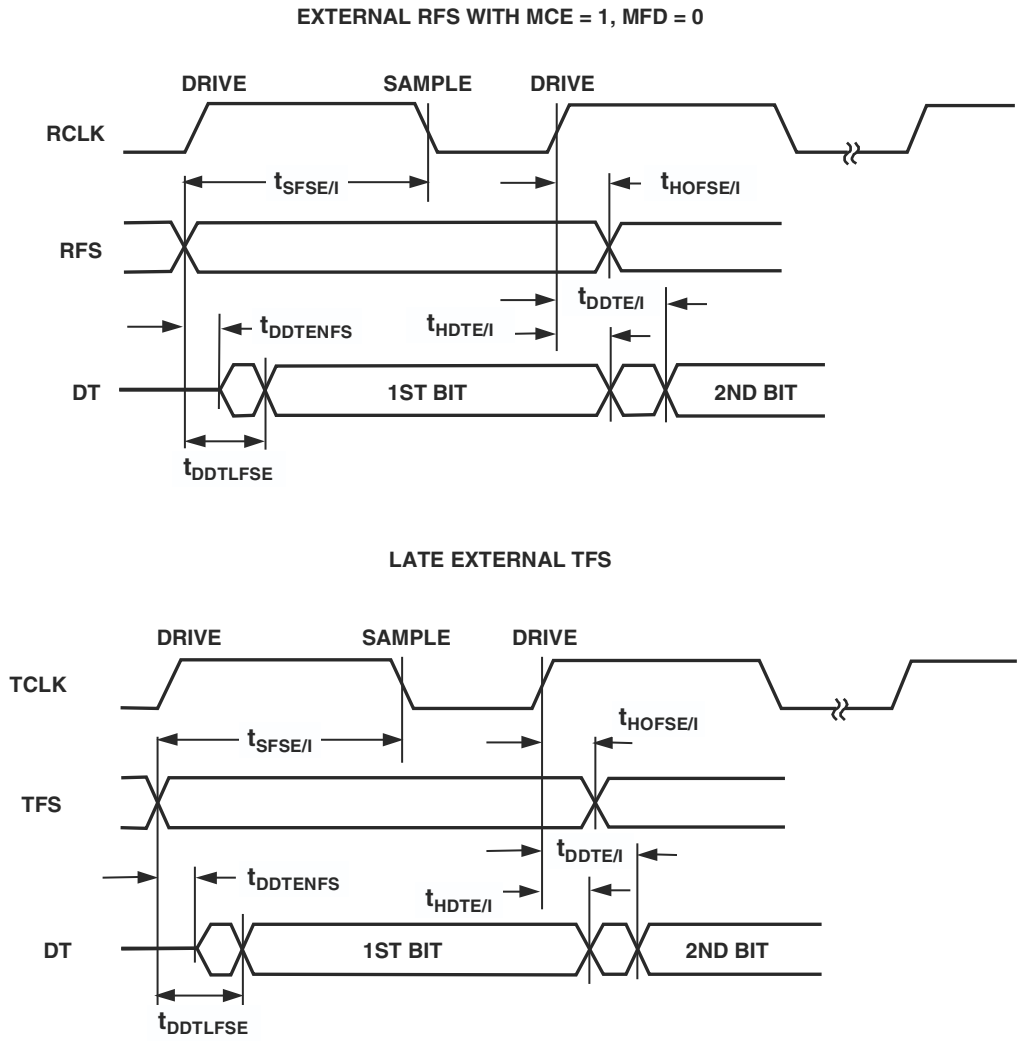

Figure 25. Serial Ports—External Late Frame Sync

Output Characteristics (5 V)

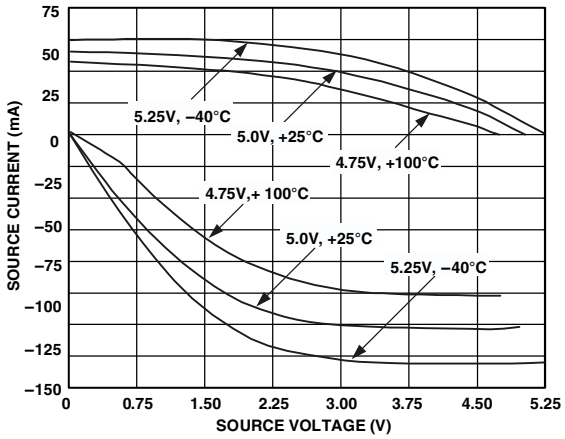

Figure 30. Typical Output Drive Currents (V_{DD} = 5 V)

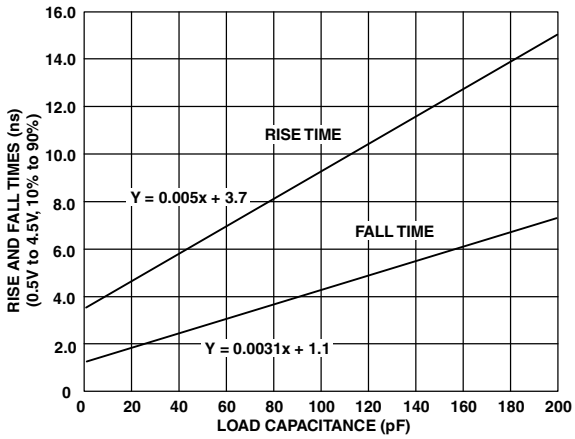

Figure 31. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

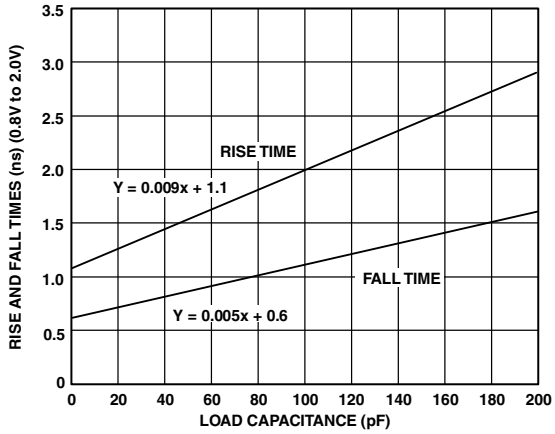

Figure 32. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

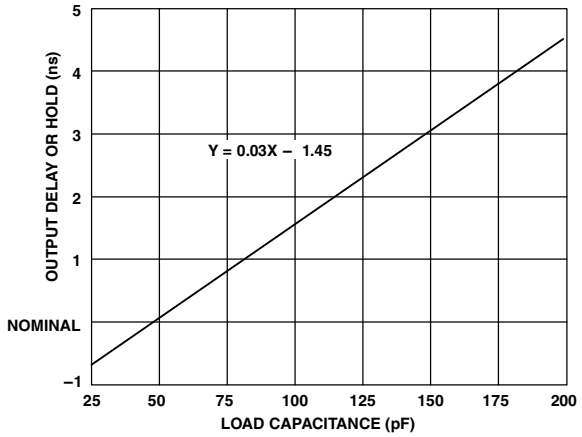

Figure 33. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

Input/Output Characteristics (3.3 V)

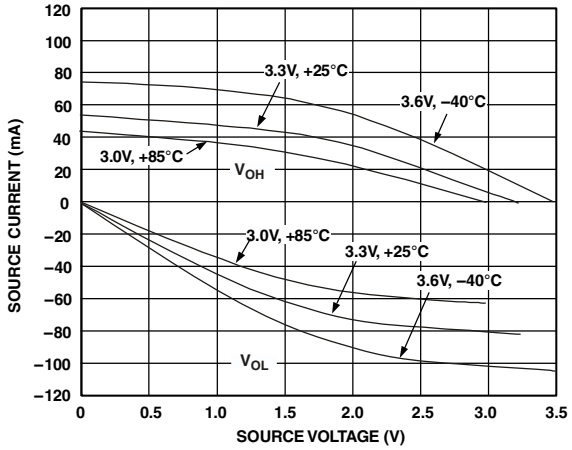

Figure 34. Typical Drive Currents (V_{DD} = 3.3 V)

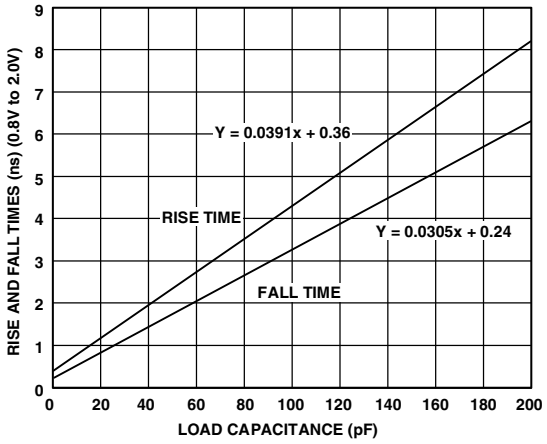

Figure 36. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

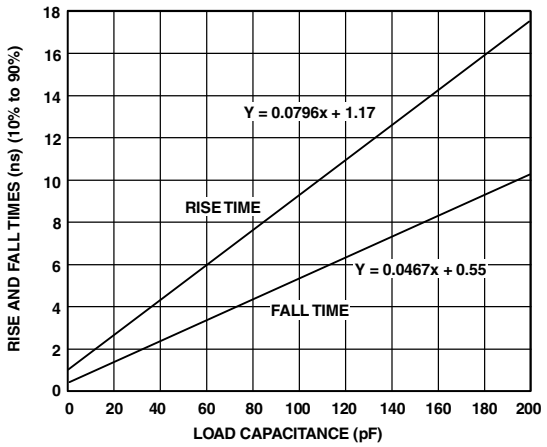

Figure 35. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

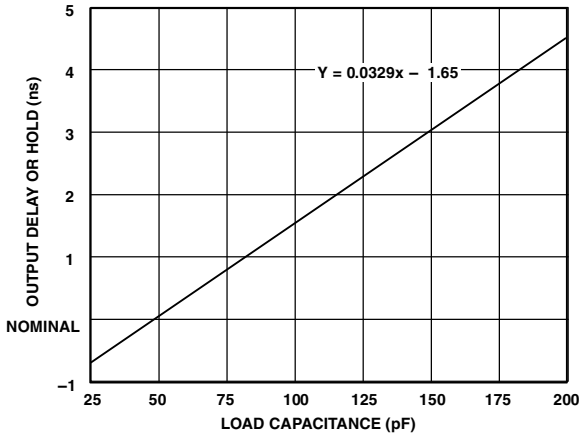

Figure 37. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 3.3 V)

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21061 is available in 240-lead thermally enhanced MQFP package. The top surface of the thermally enhanced MQFP contains a metal slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the metal slug is internally connected to GND through the device substrate.

The ADSP-21061L is available in 240-lead MQFP and 225-ball plastic BGA packages.

All packages are specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} is not exceeded, a heatsink and/or an airflow source may be used. A heat sink should be attached with a thermal adhesive.

$$T_{CASE} = T_{AMB} + (PD\ \theta_{CA})$$

T_{CASE} = Case temperature (measured on top surface of package)

T_{AMB} = Ambient temperature °C

PD =Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} =Value from tables below.

Table 29. ADSP-21061 (5 V Thermally Enhanced ED/MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	10	°C/W
	Airflow = 100	9	
	Airflow = 200	8	
	Airflow = 400	7	
	Airflow = 600	6	

Table 30. ADSP-21061L (3.3 V MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.6	°C/W
	Airflow = 100	17.6	
	Airflow = 200	15.6	
	Airflow = 400	13.9	
	Airflow = 600	12.2	

Table 31. ADSP-21061L (3.3 V PBGA Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.0	°C/W
	Airflow = 200	13.6	
	Airflow = 400	11.2	

225-BALL PBGA PIN CONFIGURATIONS

Table 32. ADSP-21061L 225-Lead Metric PBGA (B-225-2) Pin Assignments

Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number
$\overline{BMS}$	A01	ADDR25	D01	ADDR14	G01	ADDR6	K01	$\overline{EMU}$	N01
ADDR30	A02	ADDR26	D02	ADDR15	G02	ADDR5	K02	TDO	N02
$\overline{DMAR2}$	A03	$\overline{MS2}$	D03	ADDR16	G03	ADDR3	K03	$\overline{IRQ0}$	N03
DT1	A04	ADDR29	D04	ADDR19	G04	ADDR0	K04	$\overline{IRQ1}$	N04
RCLK1	A05	$\overline{DMAR1}$	D05	GND	G05	ICSA	K05	ID2	N05
TCLK0	A06	TFS1	D06	V_{DD}	G06	GND	K06	NC	N06
RCLK0	A07	$\overline{CPA}$	D07	V_{DD}	G07	V_{DD}	K07	NC	N07
ADRCLK	A08	$\overline{HBG}$	D08	V_{DD}	G08	V_{DD}	K08	NC	N08
$\overline{CS}$	A09	$\overline{DMAG2}$	D09	V_{DD}	G09	V_{DD}	K09	NC	N09
CLKIN	A10	$\overline{BR5}$	D10	V_{DD}	G10	GND	K10	NC	N10
PAGE	A11	$\overline{BR1}$	D11	GND	G11	GND	K11	NC	N11
$\overline{BR3}$	A12	DATA40	D12	DATA22	G12	DATA8	K12	NC	N12
DATA47	A13	DATA37	D13	DATA25	G13	DATA11	K13	NC	N13
DATA44	A14	DATA35	D14	DATA24	G14	DATA13	K14	DATA1	N14
DATA42	A15	DATA34	D15	DATA23	G15	DATA14	K15	DATA3	N15
$\overline{MS0}$	B01	ADDR21	E01	ADDR12	H01	ADDR2	L01	$\overline{TRST}$	P01
$\overline{SW}$	B02	ADDR22	E02	ADDR11	H02	ADDR1	L02	TMS	P02
ADDR31	B03	ADDR24	E03	ADDR13	H03	FLAG0	L03	EBOOT	P03
$\overline{HBR}$	B04	ADDR27	E04	ADDR10	H04	FLAG3	L04	ID0	P04
DR1	B05	GND	E05	GND	H05	RPBA	L05	NC	P05
DT0	B06	GND	E06	V_{DD}	H06	GND	L06	NC	P06
DR0	B07	GND	E07	V_{DD}	H07	GND	L07	NC	P07
REDY	B08	GND	E08	V_{DD}	H08	GND	L08	NC	P08
$\overline{RD}$	B09	GND	E09	V_{DD}	H09	GND	L09	NC	P09
ACK	B10	GND	E10	V_{DD}	H10	GND	L10	NC	P10
$\overline{BR6}$	B11	NC	E11	GND	H11	NC	L11	NC	P11
$\overline{BR2}$	B12	DATA33	E12	DATA18	H12	DATA4	L12	NC	P12
DATA45	B13	DATA30	E13	DATA19	H13	DATA7	L13	NC	P13
DATA43	B14	DATA32	E14	DATA21	H14	DATA9	L14	NC	P14
DATA39	B15	DATA31	E15	DATA20	H15	DATA10	L15	DATA0	P15
$\overline{MS3}$	C01	ADDR17	F01	ADDR9	J01	FLAG1	M01	TCK	R01
$\overline{MS1}$	C02	ADDR18	F02	ADDR8	J02	FLAG2	M02	$\overline{IRQ2}$	R02
ADDR28	C03	ADDR20	F03	ADDR7	J03	TIMEXP	M03	$\overline{RESET}$	R03
$\overline{SBTS}$	C04	ADDR23	F04	ADDR4	J04	TDI	M04	ID1	R04
TCLK1	C05	GND	F05	GND	J05	LBOOT (GND)	M05	NC	R05
RFS1	C06	GND	F06	V_{DD}	J06	NC	M06	NC	R06
TFS0	C07	V_{DD}	F07	V_{DD}	J07	NC	M07	NC	R07
RFS0	C08	V_{DD}	F08	V_{DD}	J08	NC	M08	NC	R08
$\overline{WR}$	C09	V_{DD}	F09	V_{DD}	J09	NC	M09	NC	R09
$\overline{DMAG1}$	C10	GND	F10	V_{DD}	J10	NC	M10	NC	R10
$\overline{BR4}$	C11	GND	F11	GND	J11	NC	M11	NC	R11
DATA46	C12	DATA29	F12	DATA12	J12	NC	M12	NC	R12

240-LEAD MQFP PIN CONFIGURATIONS

Table 33. ADSP-21061 MQFP/ED (SP-240); ADSP-21061L MQFP (S-240) Pin Assignments

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	NC	201
$\overline{TRST}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	NC	202
V_{DD}	3	$\overline{GND}$	43	DR0	83	DATA39	123	DATA12	163	NC	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{EMU}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	NC	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	NC	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	NC	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	NC	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	NC	210
FLAG0	11	ADDR26	51	$\overline{HBG}$	91	DATA34	131	DATA6	171	NC	211
GND	12	ADDR27	52	$\overline{CS}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{RD}$	93	V_{DD}	133	DATA5	173	NC	213
ADDR1	14	$\overline{MS3}$	54	$\overline{WR}$	94	V_{DD}	134	DATA4	174	NC	214
V_{DD}	15	$\overline{MS2}$	55	GND	95	GND	135	DATA3	175	NC	215
ADDR2	16	$\overline{MS1}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	NC	216
ADDR3	17	$\overline{MS0}$	57	GND	97	DATA31	137	DATA2	177	NC	217
ADDR4	18	$\overline{SW}$	58	CLKIN	98	DATA30	138	DATA1	178	NC	218
GND	19	$\overline{BMS}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{DMAG2}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{DMAG1}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	NC	182	NC	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	NC	183	NC	223
ADDR8	24	ADDR29	64	$\overline{BR6}$	104	V_{DD}	144	NC	184	NC	224
ADDR9	25	ADDR30	65	$\overline{BR5}$	105	DATA26	145	NC	185	NC	225
ADDR10	26	ADDR31	66	$\overline{BR4}$	106	DATA25	146	NC	186	NC	226
GND	27	GND	67	$\overline{BR3}$	107	DATA24	147	NC	187	NC	227
ADDR11	28	$\overline{SBTS}$	68	$\overline{BR2}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{DMAR2}$	69	$\overline{BR1}$	109	DATA23	149	NC	189	ID2	229
ADDR13	30	$\overline{DMAR1}$	70	GND	110	DATA22	150	NC	190	ID1	230
V_{DD}	31	$\overline{HBR}$	71	V_{DD}	111	DATA21	151	NC	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	NC	192	LBOOT (GND)	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	NC	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	NC	194	$\overline{RESET}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{IRQ2}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{IRQ1}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	NC	198	$\overline{IRQ0}$	238
V_{DD}	39	$\overline{CPA}$	79	DATA42	119	DATA15	159	NC	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	NC	200	TMS	240

SURFACE-MOUNT DESIGN

Table 34 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 34. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
225-Ball Grid Array (PBGA)	Solder Mask Defined	0.63 mm diameter	0.73 mm diameter

ORDERING GUIDE

Model	Notes	Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Description	Package Option
ADSP-21061KS-133		0°C to 85°C	33 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-133	[1]	0°C to 85°C	33 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KS-160		0°C to 85°C	40 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-160	[1]	0°C to 85°C	40 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KS-200		0°C to 85°C	50 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-200	[1]	0°C to 85°C	50 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061LKB-160		0°C to 85°C	40 MHz	1M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21061LKBZ-160	[1]	0°C to 85°C	40 MHz	1M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21061LKSZ-160	[1]	0°C to 85°C	40 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LASZ-176	[1]	–40°C to +85°C	44 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LKSZ-176	[1]	0°C to 85°C	44 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240

[1] Z = RoHS Compliant Part.