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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	120KB (60K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-LQFP
Supplier Device Package	160-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f807py80e

2.2 Power and Ground Signals

Table 2-2 Power Inputs

No. of Pins	Signal Name	Signal Description
8	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
3	V_{DDA}	**Analog Power**—These pins is a dedicated power pin for the analog portion of the chip and should be connected to a low noise 3.3V supply.

Table 2-3 Grounds

No. of Pins	Signal Name	Signal Description
9	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip and should all be attached to V_{SS}.
3	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
1	**TCS**	**TCS**—This Schmitt pin is reserved for factory use and must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.

Table 2-4 Supply Capacitors and VPP

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**VCAPC**	Supply	Supply	**VCAPC**—Connect each pin to a 2.2uF or greater bypass capacitor in order to bypass the core logic voltage regulator (required for proper chip operation). For more information, please refer to **Section 5.2**
2	**VPP**	Input	Input	**VPP**—This pin should be left unconnected as an open circuit for normal functionality.

Table 2-7 Data Bus Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
16	**D0–D15**	Input/Output	Tri-stated	**Data Bus**— D0–D15 specify the data for external program or data memory accesses. D0–D15 are tri-stated when the external bus is inactive. Internal pullups may be active.

Table 2-8 Bus Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{PS}}$**	Output	Tri-stated	**Program Memory Select**—$\overline{\text{PS}}$ is asserted low for external program memory access.
1	**$\overline{\text{DS}}$**	Output	Tri-stated	**Data Memory Select**—$\overline{\text{DS}}$ is asserted low for external data memory access.
1	**$\overline{\text{WR}}$**	Output	Tri-stated	**Write Enable**—$\overline{\text{WR}}$ is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted low, pins D0–D15 become outputs and the device puts data on the bus. When $\overline{\text{WR}}$ is deasserted high, the external data is latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0–A15, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a Static RAM.
1	**$\overline{\text{RD}}$**	Output	Tri-stated	**Read Enable**—$\overline{\text{RD}}$ is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low, pins D0–D15 become inputs and an external device is enabled onto the device's data bus. When $\overline{\text{RD}}$ is deasserted high, the external data is latched inside the device. When $\overline{\text{RD}}$ is asserted, it qualifies the A0–A15, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a Static RAM or ROM.

2.5 Interrupt and Program Control Signals

Table 2-9 Interrupt and Program Control Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**$\overline{\text{IRQA}}$**	Input (Schmitt)	Input	**External Interrupt Request A**—The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.
1	**$\overline{\text{IRQB}}$**	Input (Schmitt)	Input	**External Interrupt Request B**—The $\overline{\text{IRQB}}$ input is an external interrupt request that indicates that an external device is requesting service. It can be programmed to be level-sensitive or negative-edge-triggered.

Table 2-9 Interrupt and Program Control Signals (Continued)

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**RSTO**	Output	Output	**Reset Output**—This output reflects the internal reset state of the chip.
1	**RESET**	Input (Schmitt)	Input	**Reset**—This input is a direct hardware reset on the processor. When RESET is asserted low, the device is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the RESET pin is deasserted, the initial chip operating mode is latched from the EXTBOOT pin. The internal reset signal will be deasserted synchronous with the internal clocks, after a fixed number of internal clocks. To ensure complete hardware reset, RESET and TRST should be asserted together. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert RESET, but do not assert TRST.
1	**EXTBOOT**	Input (Schmitt)	Input	**External Boot**—This input is tied to V_{DD} to force device to boot from off-chip memory. Otherwise, it is tied to VSS.

2.6 GPIO Signals

Table 2-10 Dedicated General Purpose Input/Output (GPIO) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
8	**GPIOB0-GPIOB7**	Input or Output	Input	**Port B GPIO**—These eight pins are dedicated General Purpose I/O (GPIO) pins that can individually be programmed as input or output pins. After reset, the default state is GPIO input.
6	**GPIOD0-GPIOD5**	Input or Output	Input	**Port D GPIO**—These six pins are dedicated GPIO pins that can individually be programmed as an input or output pins. After reset, the default state is GPIO input.

2.8 Serial Peripheral Interface (SPI) Signals

Table 2-12 Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO**	Input/ Output	Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOE6	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MISO.
1	**MOSI**	Input/ Output	Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOE5	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MOSI.
1	**SCLK**	Input/Output	Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
	GPIOE4	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCLK.
1	**$\overline{\text{SS}}$**	Input	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
	GPIOE7	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is $\overline{\text{SS}}$.

2.14 JTAG/OnCE

Table 2-19 JTAG/On-Chip Emulation (OnCE) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TCK**	Input (Schmitt)	Input, pulled low internally	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
1	**TMS**	Input (Schmitt)	Input, pulled high internally	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
1	**TDI**	Input (Schmitt)	Input, pulled high internally	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDO**	Output	Tri-stated	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
1	**$\overline{\text{TRST}}$**	Input (Schmitt)	Input, pulled high internally	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted at power-up and whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
1	**$\overline{\text{DE}}$**	Output	Output	**Debug Event**—$\overline{\text{DE}}$ provides a low pulse on recognized debug events.

Part 3 Specifications

3.1 General Characteristics

The 56F807 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 3-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent

damage to the device.

The 56F807 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Analog inputs, ANA0-7 and VREF	V_{IN}	V_{SSA}– 0.3	V_{DDA}+ 0.3	V
Analog inputs EXTAL and XTAL	V_{IN}	V_{SSA}– 0.3	V_{SSA}+ 3.0	V
Current drain per pin excluding V_{DD}, V_{SS}, PWM outputs, TCS, VPP, V_{DDA}, V_{SSA}	I	—	10	mA

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, digital	V_{DD}	3.0	3.3	3.6	V
Supply Voltage, analog	V_{DDA}	3.0	3.3	3.6	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V

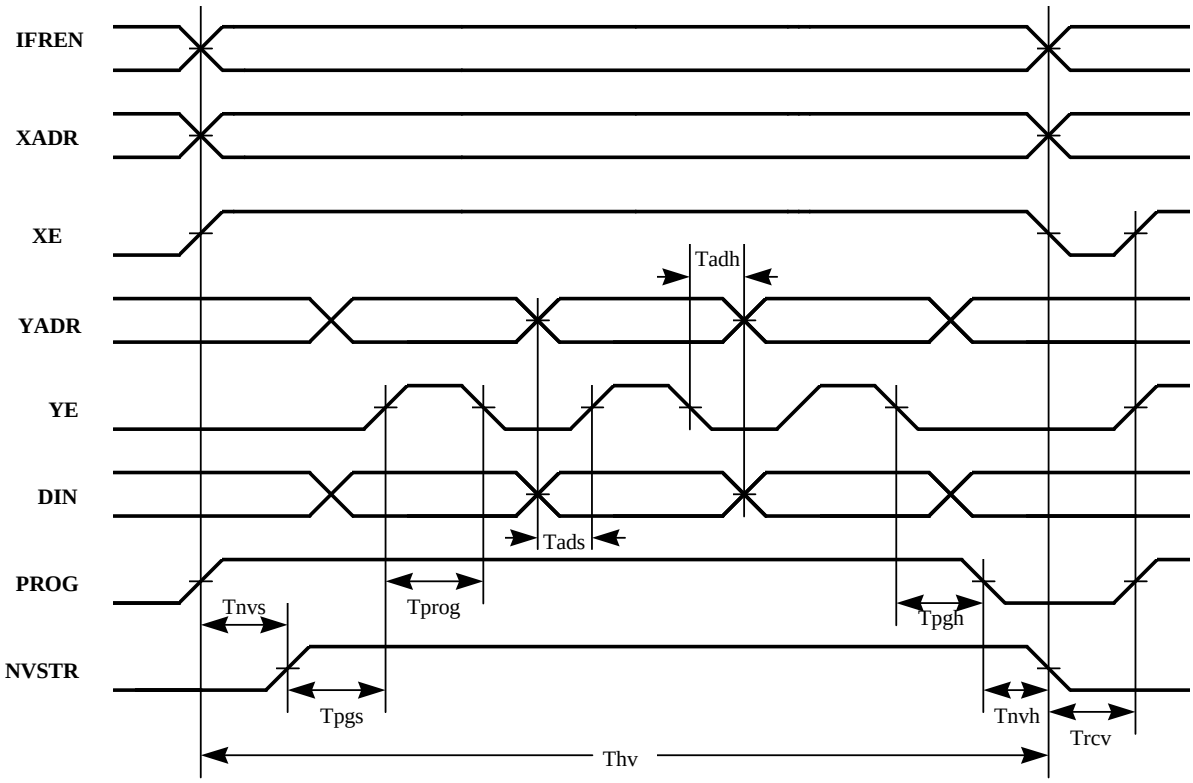


Figure 3-4 Flash Program Cycle

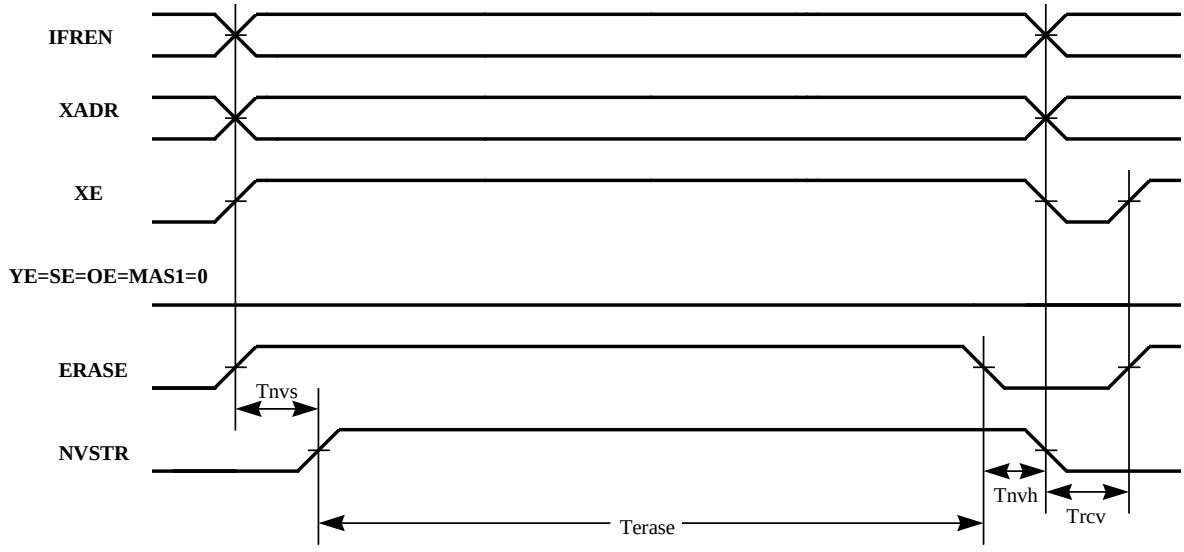


Figure 3-5 Flash Erase Cycle

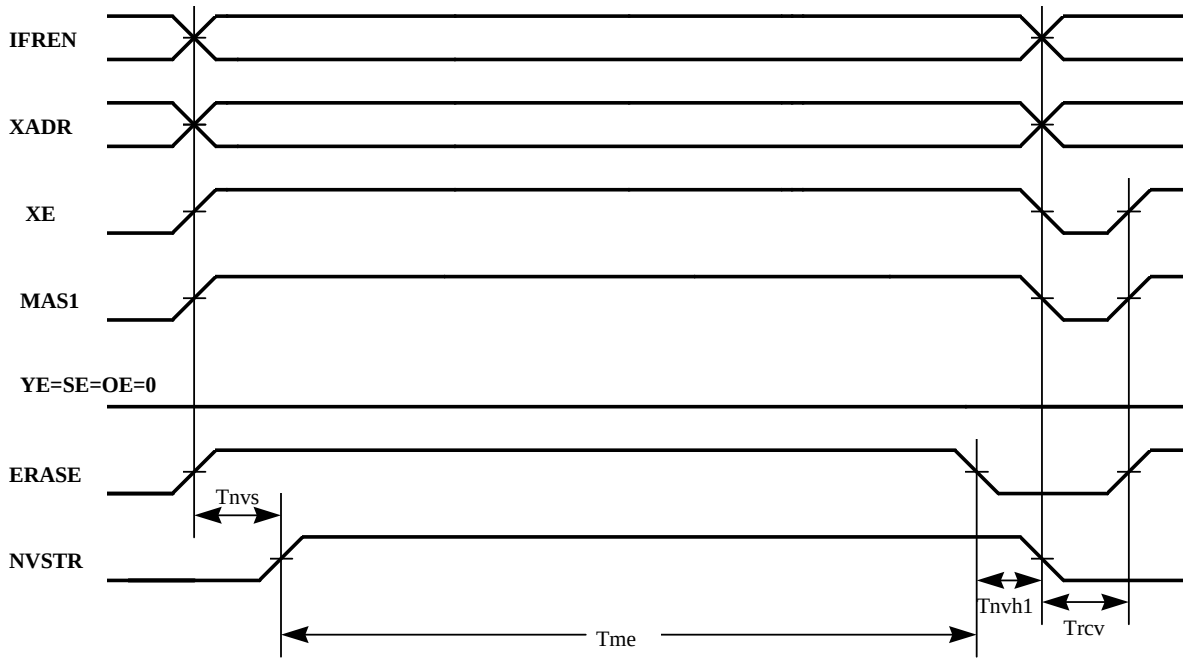


Figure 3-6 Flash Mass Erase Cycle

3.4 External Clock Operation

The 56F807 system clock can be derived from an external crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

3.4.1 Crystal Oscillator

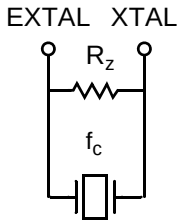
The internal oscillator is also designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 3-9**. In **Figure 3-7** a recommended crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time. The internal 56F80x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 3-8** no external load capacitors should be used.

The 56F80x components internally are modeled as a parallel resonant oscillator circuit to provide a capacitive load on each of the oscillator pins (XTAL and EXTAL) of 10pF to 13pF over temperature and process variations. Using a typical value of internal capacitance on these pins of 12pF and a value of 3pF

as a typical circuit board trace capacitance the parallel load capacitance presented to the crystal is 9pF as determined by the following equation:

$$CL = \frac{CL1 * CL2}{CL1 + CL2} + Cs = \frac{12 * 12}{12 + 12} + 3 = 6 + 3 = 9pF$$

This is the value load capacitance that should be used when selecting a crystal and determining the actual frequency of operation of the crystal oscillator circuit.

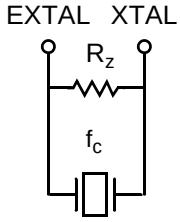


Recommended External Crystal Parameters:
R_z = 1 to 3 MΩ
f_c = 8MHz (optimized for 8MHz)

Figure 3-7 Connecting to a Crystal Oscillator

3.4.2 Ceramic Resonator

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. In **Figure 3-8**, a typical ceramic resonator circuit is shown. Refer to supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as close as possible to the EXTAL and XTAL pins. The internal 56F80x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 3-7** no external load capacitors should be used.



Recommended Ceramic Resonator Parameters:
R_z = 1 to 3 MΩ
f_c = 8MHz (optimized for 8MHz)

Figure 3-8 Connecting a Ceramic Resonator

Note: Freescale recommends only two terminal ceramic resonators vs. three terminal resonators (which contain an internal bypass capacitor to ground).

3.5 External Bus Asynchronous Timing

Table 3-10 External Bus Asynchronous Timing[1,2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	6.5	—	ns
$\overline{WR}$ Width Asserted Wait states = 0 Wait states > 0	t_{WR}	 7.5 (T*WS)+7.5	 — —	 ns ns
$\overline{WR}$ Asserted to D0–D15 Out Valid	t_{WRD}	—	T + 4.2	ns
Data Out Hold Time from $\overline{WR}$ Deasserted	t_{DOH}	4.8	—	ns
Data Out Set Up Time to $\overline{WR}$ Deasserted Wait states = 0 Wait states > 0	t_{DOS}	 2.2 (T*WS)+6.4	 — —	 ns ns
$\overline{RD}$ Deasserted to Address Not Valid	t_{RDA}	0	—	ns
Address Valid to $\overline{RD}$ Deasserted Wait states = 0 Wait states > 0	t_{ARDD}	 18.7 (T*WS) + 18.7	—	 ns ns
Input Data Hold to $\overline{RD}$ Deasserted	t_{DRD}	0	—	ns
$\overline{RD}$ Assertion Width Wait states = 0 Wait states > 0	t_{RD}	 19 (T*WS)+19	 — —	 ns ns
Address Valid to Input Data Valid Wait states = 0 Wait states > 0	t_{AD}	 — —	 1 (T*WS)+1	 ns ns
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}	-4.4	—	ns
$\overline{RD}$ Asserted to Input Data Valid Wait states = 0 Wait states > 0	t_{RDD}	 — —	 2.4 (T*WS) + 2.4	 ns ns
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}	6.8	—	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}	0	—	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	14.1	—	ns
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}	12.8	—	ns

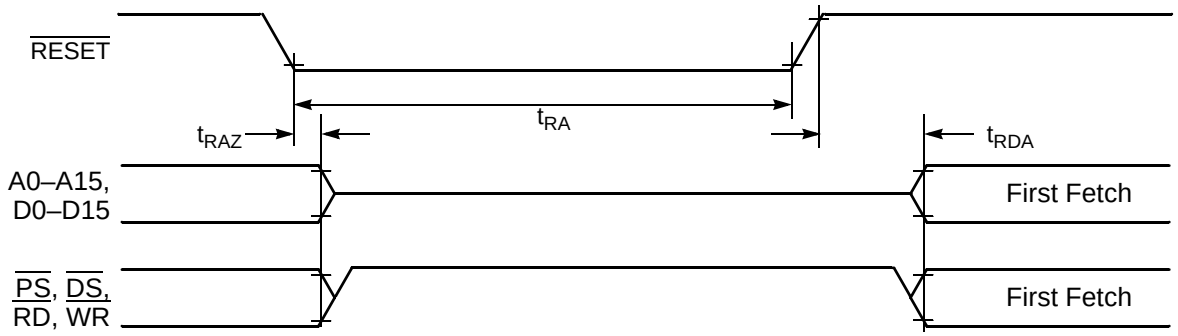


Figure 3-12 Asynchronous Reset Timing

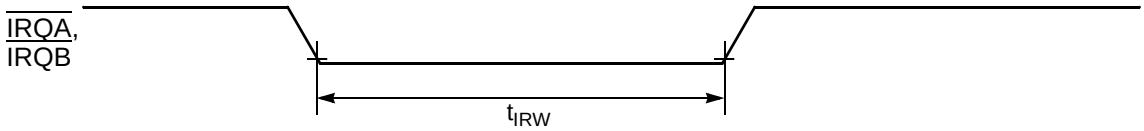


Figure 3-13 External Interrupt Timing (Negative-Edge-Sensitive)

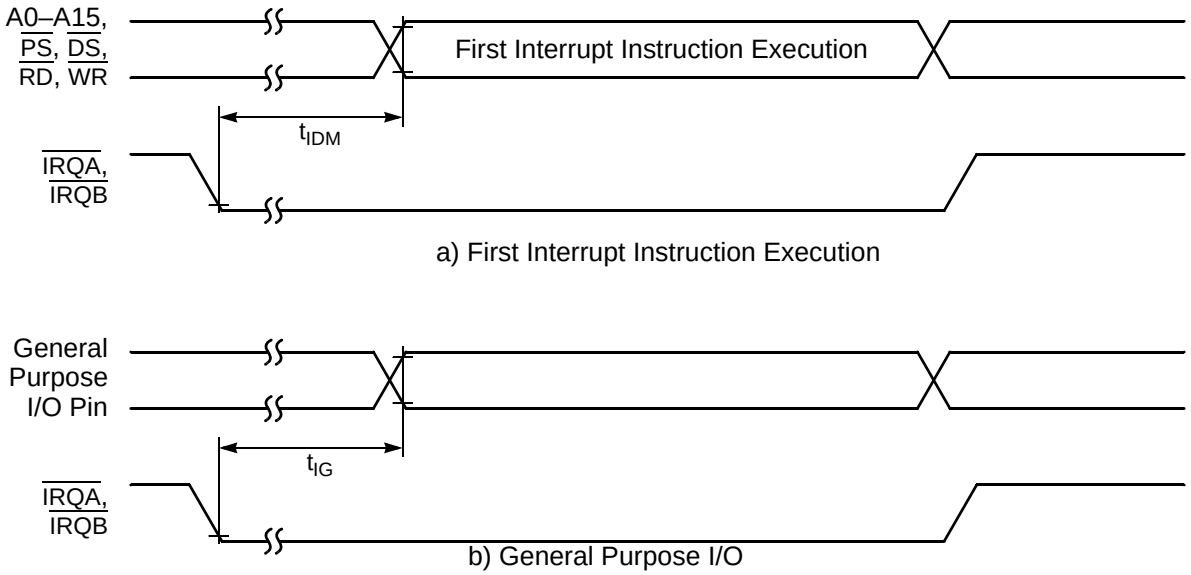


Figure 3-14 External Level-Sensitive Interrupt Timing

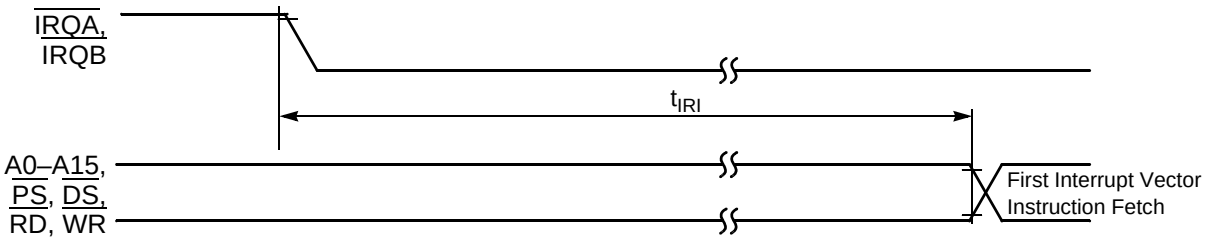


Figure 3-15 Interrupt from Wait State Timing

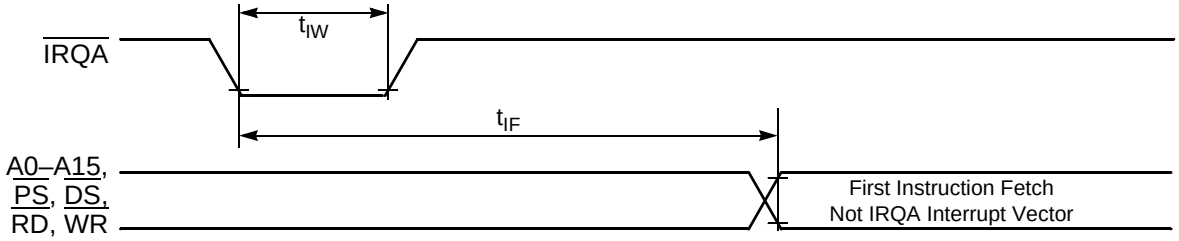


Figure 3-16 Recovery from Stop State Using Asynchronous Interrupt Timing

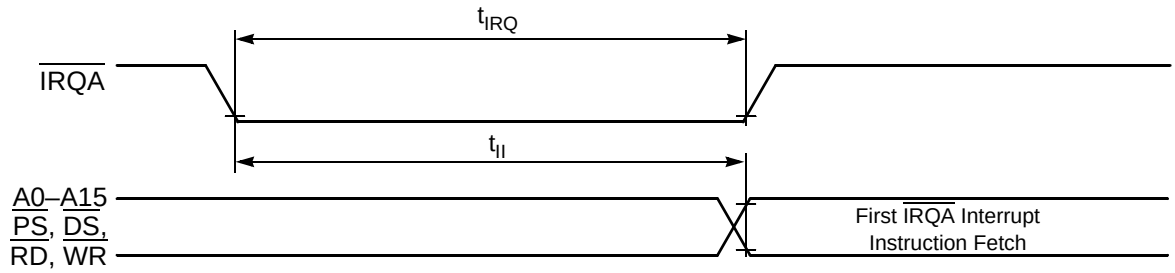


Figure 3-17 Recovery from Stop State Using IRQA Interrupt Service

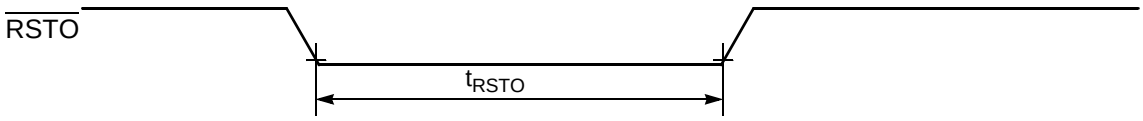


Figure 3-18 Reset Output Timing

3.7 Serial Peripheral Interface (SPI) Timing

Table 3-12 SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	3-19-3-22
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	3-22
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	3-22
Clock (SCK) high time Master Slave	t_{CH}	 17.6 12.5	 — —	 ns ns	3-19, 3-20, 3-21, 3-22
Clock (SCK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	3-22
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	3-19, 3-20, 3-21, 3-22
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	3-19, 3-20, 3-21, 3-22
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	3-22
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	3-22
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	3-19, 3-20, 3-21, 3-22
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	3-19, 3-20, 3-21, 3-22
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	3-19, 3-20, 3-21, 3-22
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	3-19, 3-20, 3-21, 3-22

1. Parameters listed are guaranteed by design.

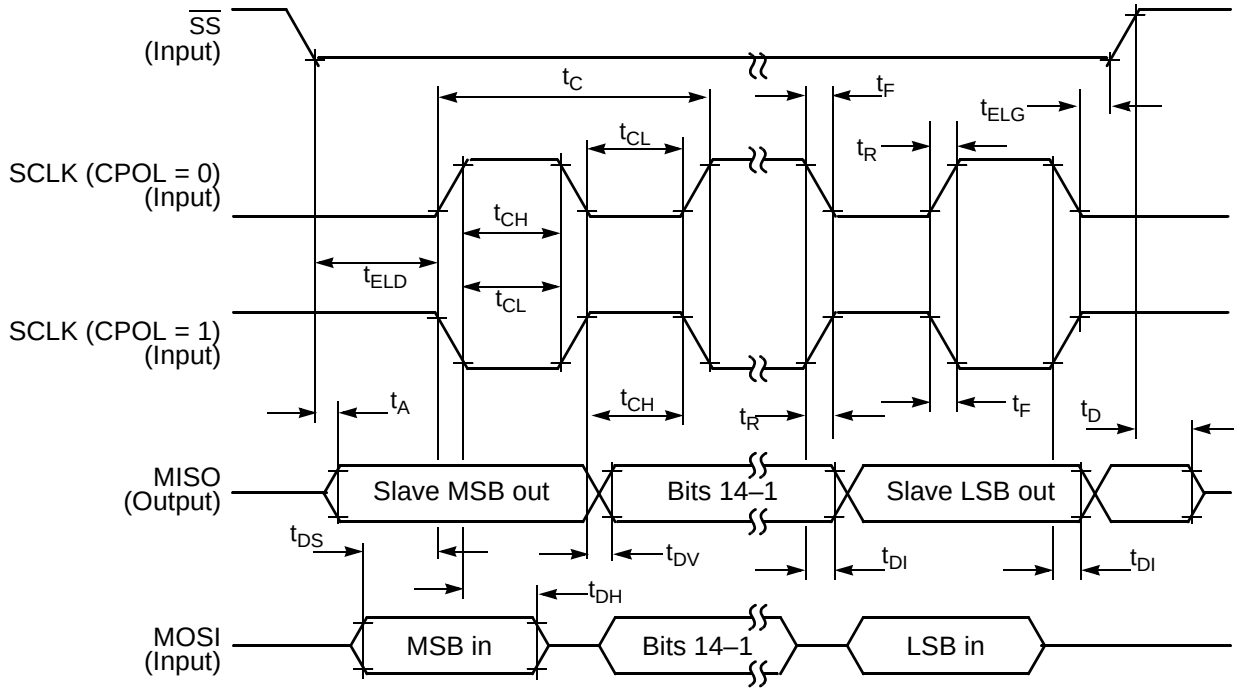


Figure 3-21 SPI Slave Timing (CPHA = 0)

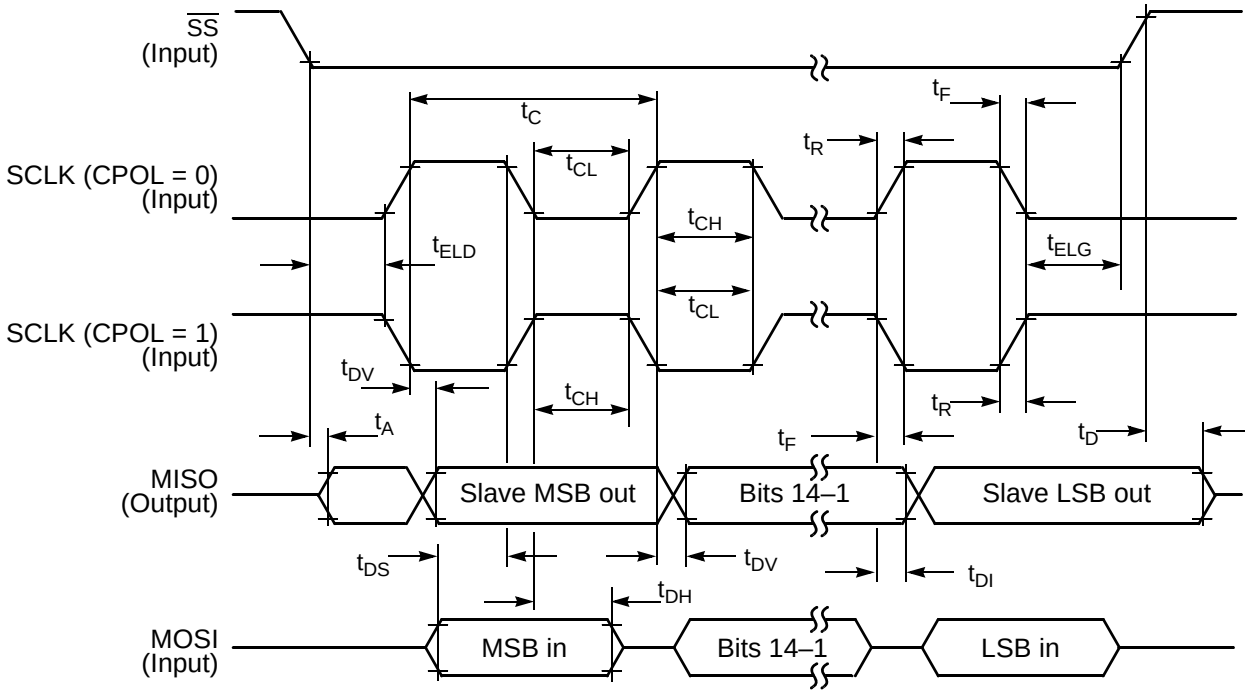
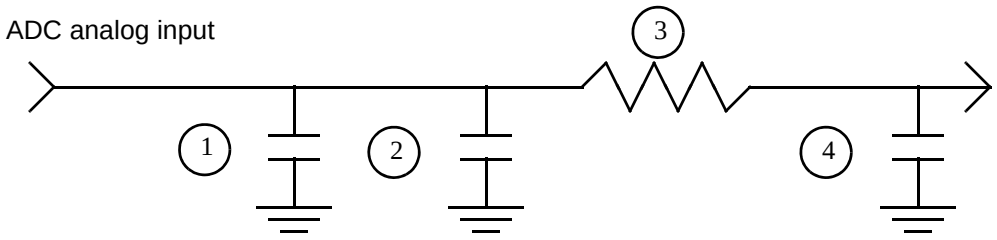


Figure 3-22 SPI Slave Timing (CPHA = 1)

.



1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. (1.8pf)
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. (2.04pf)
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. (500 ohms)
4. Sampling capacitor at the sample and hold circuit. Capacitor 4 is normally disconnected from the input and is only connected to it at sampling time. (1pf)

Figure 3-27 Equivalent Analog Input Circuit

3.12 Controller Area Network (CAN) Timing

Table 3-17 CAN Timing[2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, MSCAN Clock = 30MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
Bus Wakeup detection [1]	T_{WAKEUP}	5	—	µs

1. If Wakeup glitch filter is enabled during the design initialization and also CAN is put into SLEEP mode then, any bus event (on MSCAN_RX pin) whose duration is less than 5 microseconds is filtered away. However, a valid CAN bus wakeup detection takes place for a wakeup pulse equal to or greater than 5 microseconds. The number 5 microseconds originates from the fact that the CAN wakeup message consists of 5 dominant bits at the highest possible baud rate of 1Mbps.
2. Parameters listed are guaranteed by design

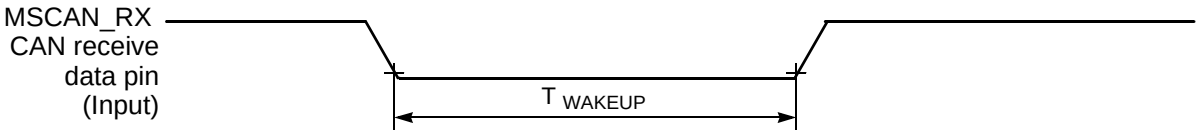


Figure 3-28 Bus Wakeup Detection

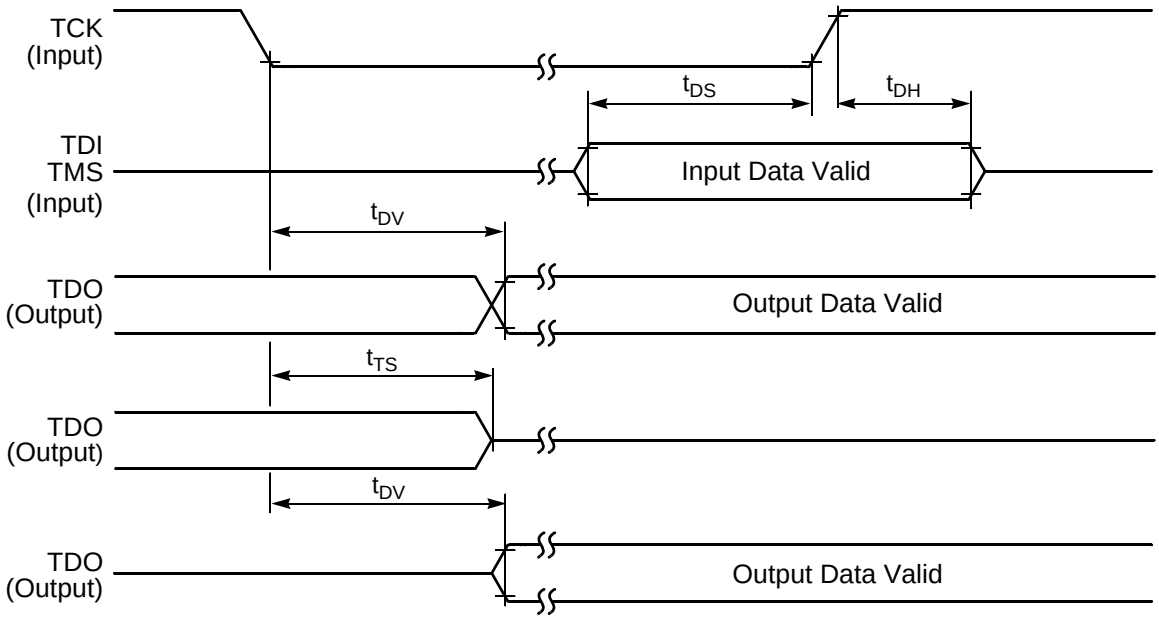
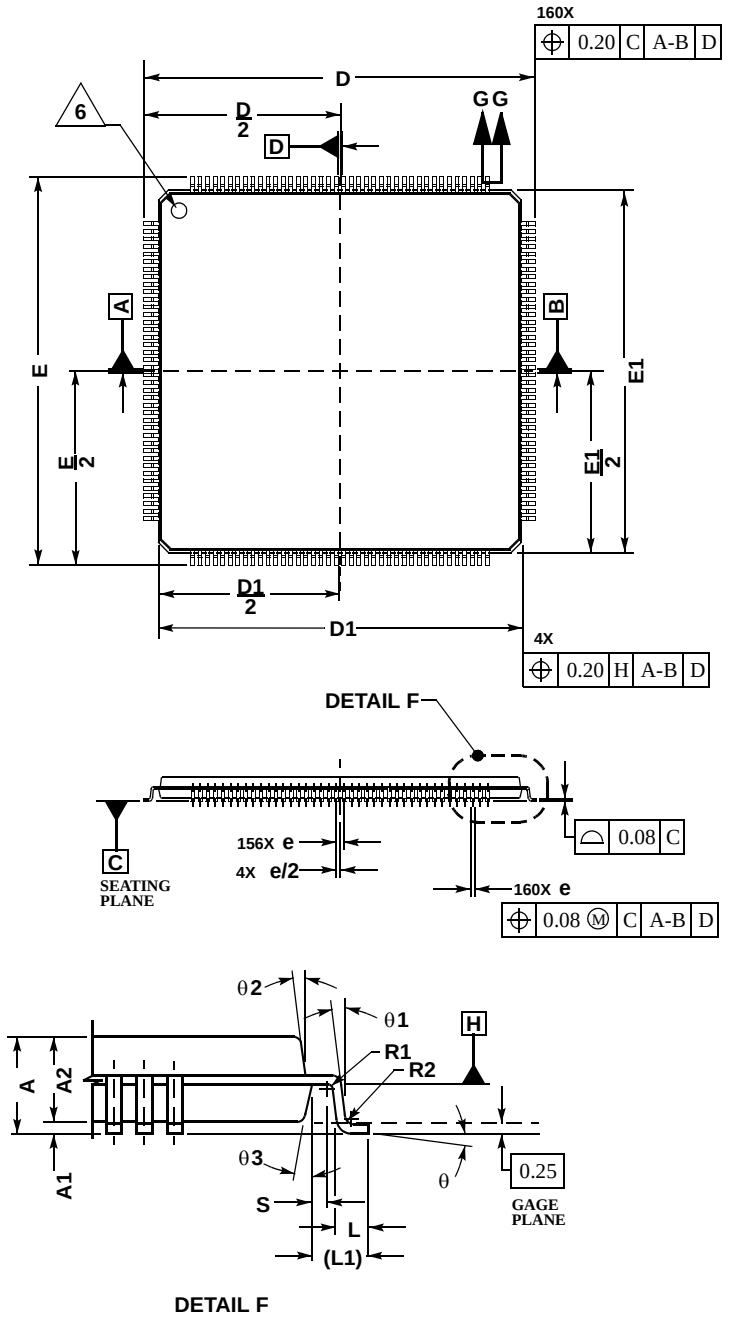
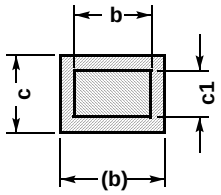


Figure 3-30 Test Access Port Timing Diagram

Figure 3-31 $\overline{\text{TRST}}$ Timing Diagram

Figure 3-32 OnCE—Debug Event





SECTION G-G

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. EXACT SHAPE OF CORNERS MAY VARY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	26.00 BSC	
D1	24.00 BSC	
e	0.50 BSC	
E	26.00 BSC	
E1	24.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	---
R2	0.08	0.20
S	0.20	---
θ	0°	7°
θ1	0°	---
θ2	11°	13°
θ3	11°	13°

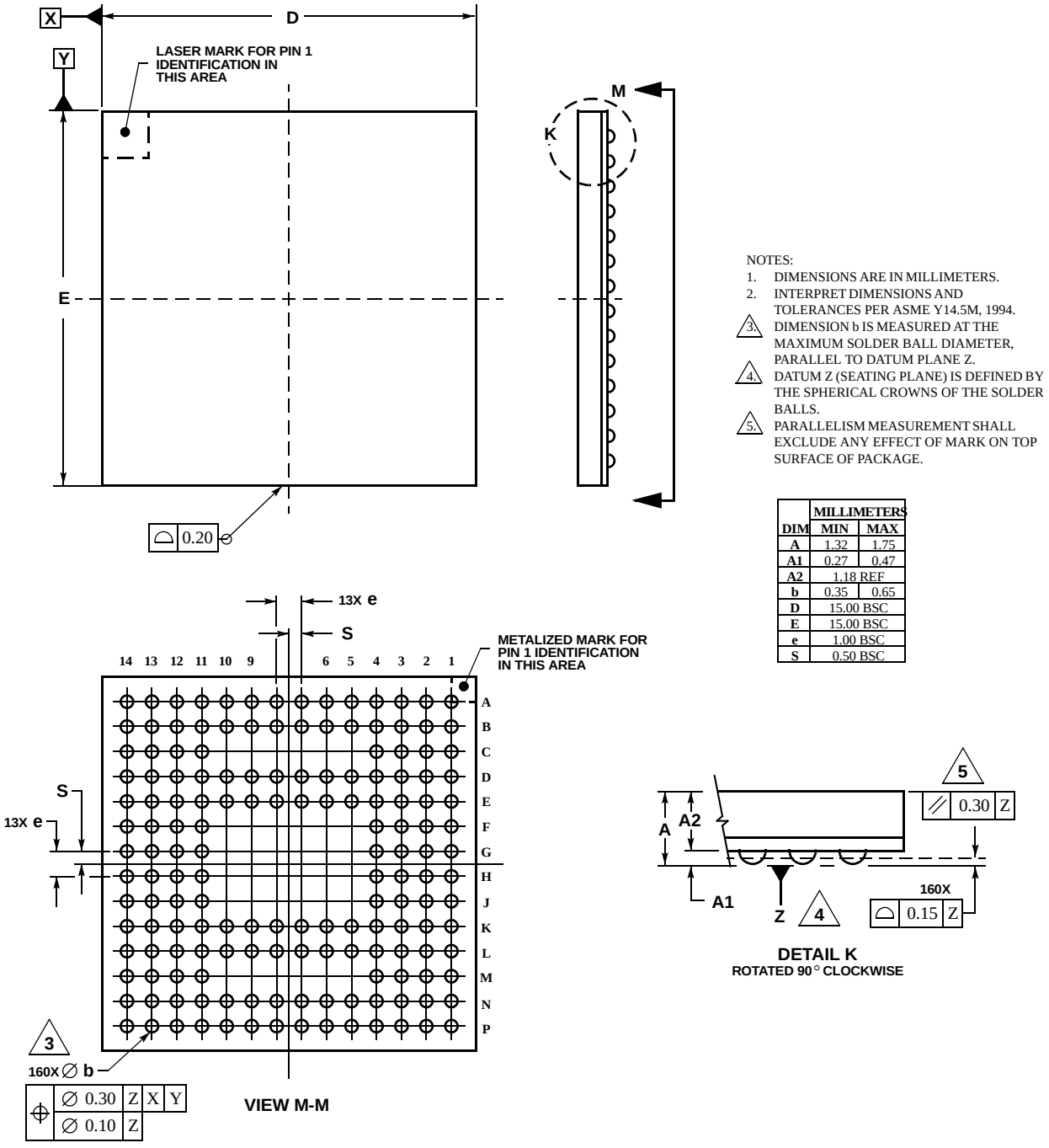
CASE 1259-01
ISSUE O

Figure 4-2 160-pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.

Table 4-1 56F807 LQFP Package Pin Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
31	D8	71	FAULTB0	111	V_{DDA}	151	PHA1
32	D9	72	FAULTB1	112	V_{SSA}	152	PHB1
33	D10	73	FAULTB2	113	ANB0	153	V_{DD}
34	V_{DD}	74	FAULTB3	114	ANB1	154	INDEX1
35	D11	75	PWMA0	115	ANB2	155	HOME1
36	D12	76	V_{SS}	116	ANB3	156	VPP
37	D13	77	PWMA1	117	ANB4	157	V_{SS}
38	D14	78	PWMA2	118	ANB5	158	CLKO
39	D15	79	PWMA3	119	ANB6	159	TXD0
40	GPIOB0	80	PWMA4	120	ANB7	160	RXD0



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.32	1.75
A1	0.27	0.47
A2	1.18 REF	
b	0.35	0.65
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

CASE 1268-01
ISSUE O

Figure 4-3 160 MAPBGA Mechanical Information

Please see **www.freescale.com** for the most current case outline.

- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the controller, and from the board ground to each V_{SS} pin.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.