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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	120KB (60K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BGA
Supplier Device Package	160-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f807vf80

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description and proper design with the 56F807. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com**.

Table 1-1 56F807 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F803, 56F805, and 56F807	DSP56F801-7UM
56F807 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F807
56F807 Errata	Details any chip issues that might be present	56F807E

1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

2.2 Power and Ground Signals

Table 2-2 Power Inputs

No. of Pins	Signal Name	Signal Description
8	V_{DD}	**Power**—These pins provide power to the internal structures of the chip, and should all be attached to V_{DD}.
3	V_{DDA}	**Analog Power**—These pins is a dedicated power pin for the analog portion of the chip and should be connected to a low noise 3.3V supply.

Table 2-3 Grounds

No. of Pins	Signal Name	Signal Description
9	V_{SS}	**GND**—These pins provide grounding for the internal structures of the chip and should all be attached to V_{SS}.
3	V_{SSA}	**Analog Ground**—This pin supplies an analog ground.
1	**TCS**	**TCS**—This Schmitt pin is reserved for factory use and must be tied to V_{SS} for normal use. In block diagrams, this pin is considered an additional V_{SS}.

Table 2-4 Supply Capacitors and VPP

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**VCAPC**	Supply	Supply	**VCAPC**—Connect each pin to a 2.2uF or greater bypass capacitor in order to bypass the core logic voltage regulator (required for proper chip operation). For more information, please refer to **Section 5.2**
2	**VPP**	Input	Input	**VPP**—This pin should be left unconnected as an open circuit for normal functionality.

2.8 Serial Peripheral Interface (SPI) Signals

Table 2-12 Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO**	Input/ Output	Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOE6	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MISO.
1	**MOSI**	Input/ Output	Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOE5	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MOSI.
1	**SCLK**	Input/Output	Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
	GPIOE4	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCLK.
1	**$\overline{\text{SS}}$**	Input	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
	GPIOE7	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is $\overline{\text{SS}}$.

2.10 Serial Communications Interface (SCI) Signals

Table 2-14 Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO**	Input/ Output	Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOE6	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MISO.
1	**MOSI**	Input/ Output	Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOE5	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MOSI.
1	**SCLK**	Input/Output	Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
	GPIOE4	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCLK.
1	**$\overline{\text{SS}}$**	Input	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
	GPIOE7	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is $\overline{\text{SS}}$.

2.12 Analog-to-Digital Converter (ADC) Signals

Table 2-17 Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANA0-3**	Input	Input	**ANA0-3**—Analog inputs to ADCA channel 1
4	**ANA4-7**	Input	Input	**ANA4-7**—Analog inputs to ADCA channel 2
2	**VREF**	Input	Input	**VREF**—Analog reference voltage for ADC. Must be set to V_{DDA}-0.3V for optimal performance.
4	**ANB0-3**	Input	Input	**ANB0-3**—Analog inputs to ADCB, channel 1
4	**ANB4-7**	Input	Input	**ANB4-7**—Analog inputs to ADCB, channel 2

2.13 Quad Timer Module Signals

Table 2-18 Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**TC0-1**	Input/Output	Input	**TC0-1**—Timer C Channels 0 and 1
4	**TD0-3**	Input/Output	Input	**TD0-3**—Timer D Channels 0, 1, 2, and 3

2.14 JTAG/OnCE

Table 2-19 JTAG/On-Chip Emulation (OnCE) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TCK**	Input (Schmitt)	Input, pulled low internally	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
1	**TMS**	Input (Schmitt)	Input, pulled high internally	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
1	**TDI**	Input (Schmitt)	Input, pulled high internally	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDO**	Output	Tri-stated	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
1	**$\overline{\text{TRST}}$**	Input (Schmitt)	Input, pulled high internally	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted at power-up and whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
1	**$\overline{\text{DE}}$**	Output	Output	**Debug Event**—$\overline{\text{DE}}$ provides a low pulse on recognized debug events.

Part 3 Specifications

3.1 General Characteristics

The 56F807 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 3-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent

Table 3-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Output Low Voltage (at IOL)	V_{OL}	—	—	0.4	V
Output source current	I_{OH}	4	—	—	mA
Output source current	I_{OL}	4	—	—	mA
PWM pin output source current[3]	I_{OHP}	10	—	—	mA
PWM pin output sink current[4]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current	I_{DDT}[5]				
Run [6]		—	195	220	mA
Wait[7]		—	170	200	mA
Stop		—	115	145	mA
Low Voltage Interrupt, external power supply[8]	V_{EIO}	2.4	2.7	3.0	V
Low Voltage Interrupt, internal power supply[9]	V_{EIC}	2.0	2.2	2.4	V
Power on Reset[10]	V_{POR}	—	1.7	2.0	V

1. Schmitt Trigger inputs are: EXTBOOT, IRQA, IRQB, RESET, TCS, ISA0-2, FAULTA0-3, ISB0-2, FAULTB0-3, TCK, TRST, TMS, TDI, and MSCAN_RX

2. Analog inputs are: ANA[0:7], XTAL and EXTAL. Specification assumes ADC is not sampling.

3. PWM pin output source current measured with 50% duty cycle.

4. PWM pin output sink current measured with 50% duty cycle.

5. $I_{DDT} = I_{DD} + I_{DDA}$ (Total supply current for $V_{DD} + V_{DDA}$)

6. Run (operating) I_{DD} measured using 8MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.

7. Wait I_{DD} measured using external square wave clock source (f_{osc} = 8MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50pF on all outputs. C_L = 20pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.

8. This low voltage interrupt monitors the V_{DDA} external power supply. V_{DDA} is generally connected to the same potential as V_{DD} via separate traces. If V_{DDA} drops below V_{EIO}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DDA} \geq V_{EIO}$ (between the minimum specified V_{DD} and the point when the V_{EIO} interrupt is generated).

9. This low voltage interrupt monitors the internally regulated core power supply. If the output from the internal voltage is regulator drops below V_{EIC}, an interrupt is generated. Since the core logic supply is internally regulated, this interrupt will not be generated unless the external power supply drops below the minimum specified value (3.0V).

10. Power–on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active as long as the internal 2.5V is below 1.5V typical, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

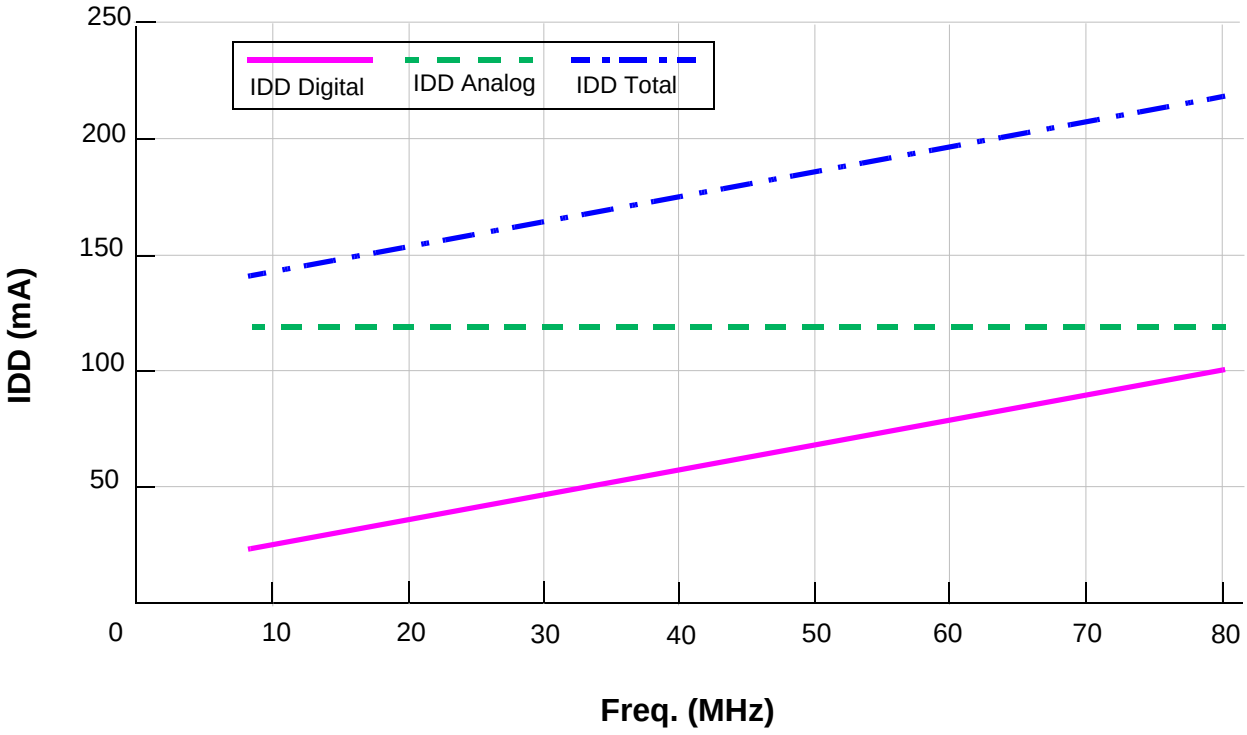
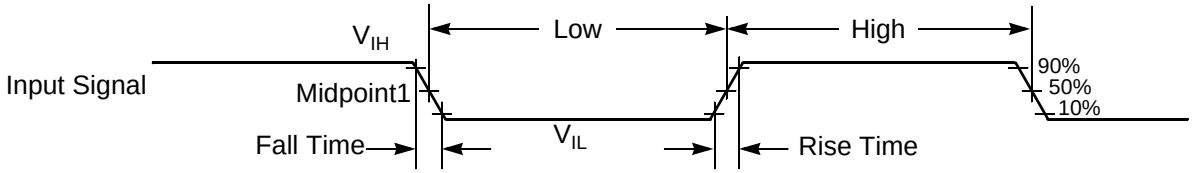


Figure 3-1 Maximum Run IDD vs. Frequency (see Note 6. in Table 3-14)

3.3 AC Electrical Characteristics

Timing waveforms in **Section 3.3** are tested using the V_{IL} and V_{IH} levels specified in the DC Characteristics table. In **Figure 3-2** the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 3-2 Input Signal Measurement References

Figure 3-3 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

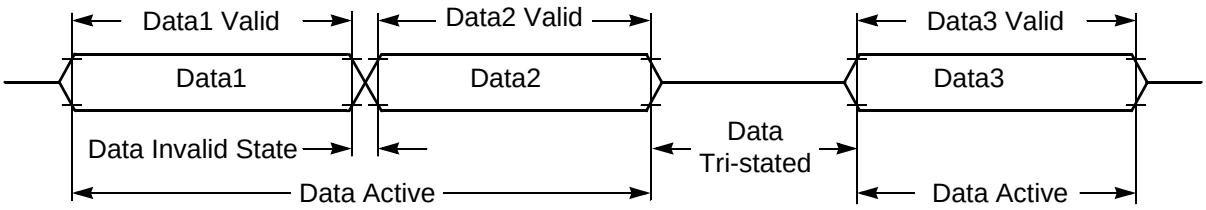


Figure 3-3 Signal States

Table 3-5 Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE=0
2. Y address enable, YMUX is disabled when YE=0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE=0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 3-6 IFREN Truth Table

Mode	IFREN=1	IFREN=0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

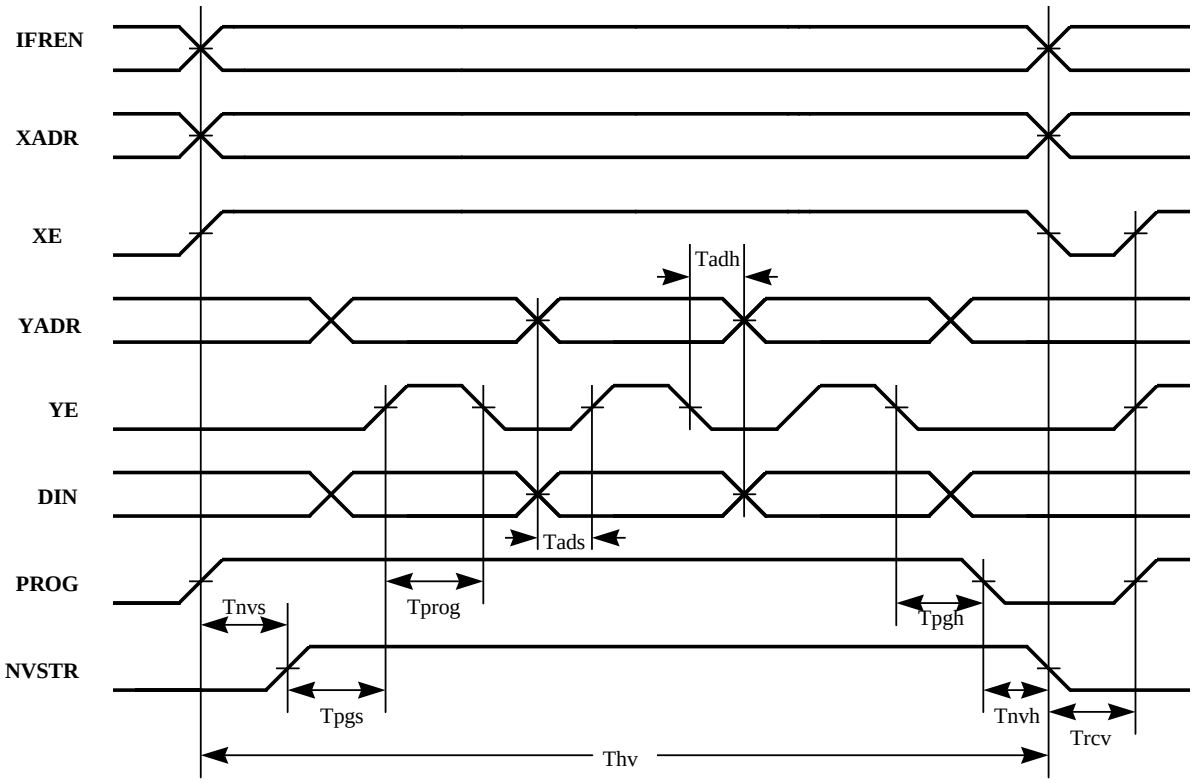


Figure 3-4 Flash Program Cycle

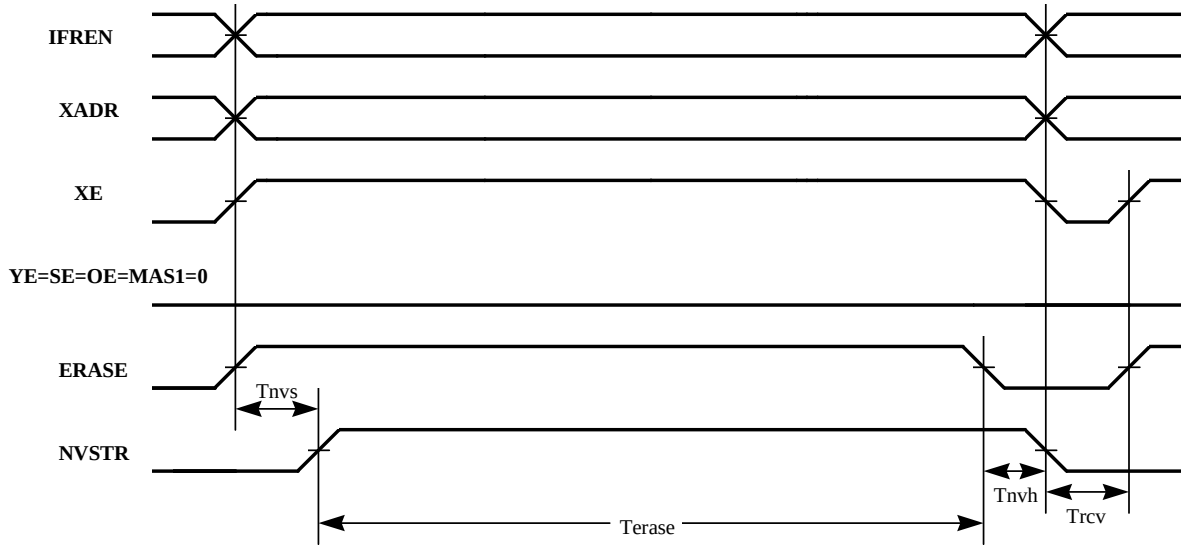


Figure 3-5 Flash Erase Cycle

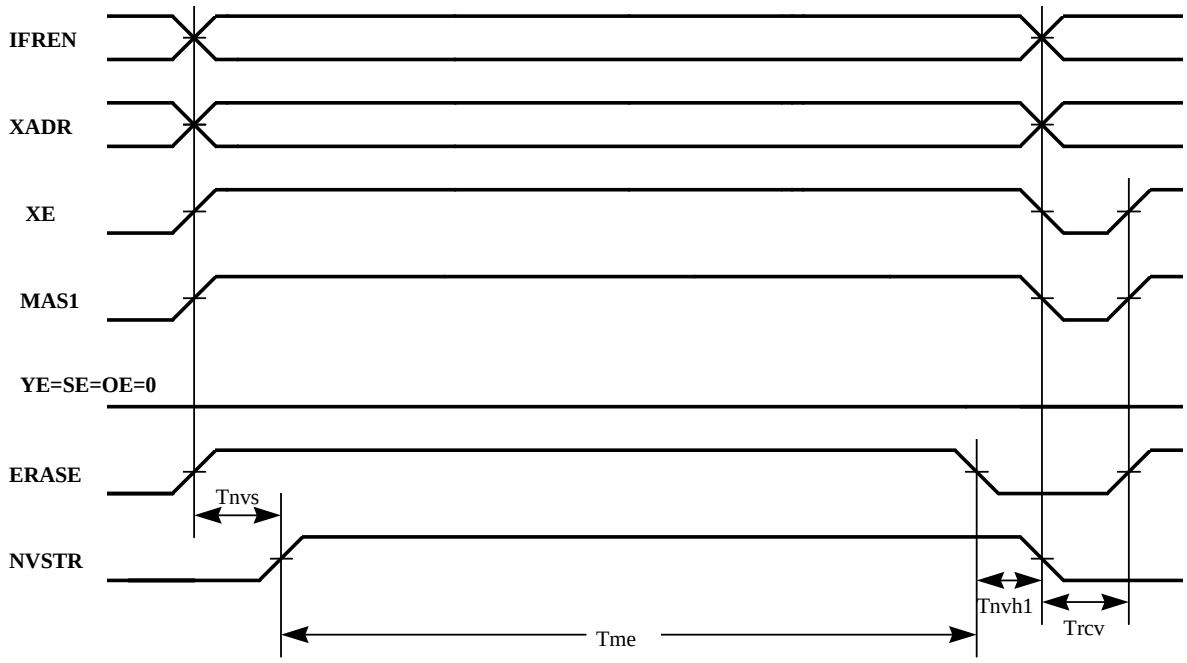


Figure 3-6 Flash Mass Erase Cycle

3.4 External Clock Operation

The 56F807 system clock can be derived from an external crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

3.4.1 Crystal Oscillator

The internal oscillator is also designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 3-9**. In **Figure 3-7** a recommended crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time. The internal 56F80x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 3-8** no external load capacitors should be used.

The 56F80x components internally are modeled as a parallel resonant oscillator circuit to provide a capacitive load on each of the oscillator pins (XTAL and EXTAL) of 10pF to 13pF over temperature and process variations. Using a typical value of internal capacitance on these pins of 12pF and a value of 3pF

3.5 External Bus Asynchronous Timing

Table 3-10 External Bus Asynchronous Timing[1,2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	6.5	—	ns
$\overline{WR}$ Width Asserted Wait states = 0 Wait states > 0	t_{WR}	 7.5 (T*WS)+7.5	 — —	 ns ns
$\overline{WR}$ Asserted to D0–D15 Out Valid	t_{WRD}	—	T + 4.2	ns
Data Out Hold Time from $\overline{WR}$ Deasserted	t_{DOH}	4.8	—	ns
Data Out Set Up Time to $\overline{WR}$ Deasserted Wait states = 0 Wait states > 0	t_{DOS}	 2.2 (T*WS)+6.4	 — —	 ns ns
$\overline{RD}$ Deasserted to Address Not Valid	t_{RDA}	0	—	ns
Address Valid to $\overline{RD}$ Deasserted Wait states = 0 Wait states > 0	t_{ARDD}	 18.7 (T*WS) + 18.7	—	 ns ns
Input Data Hold to $\overline{RD}$ Deasserted	t_{DRD}	0	—	ns
$\overline{RD}$ Assertion Width Wait states = 0 Wait states > 0	t_{RD}	 19 (T*WS)+19	 — —	 ns ns
Address Valid to Input Data Valid Wait states = 0 Wait states > 0	t_{AD}	 — —	 1 (T*WS)+1	 ns ns
Address Valid to $\overline{RD}$ Asserted	t_{ARDA}	-4.4	—	ns
$\overline{RD}$ Asserted to Input Data Valid Wait states = 0 Wait states > 0	t_{RDD}	 — —	 2.4 (T*WS) + 2.4	 ns ns
$\overline{WR}$ Deasserted to $\overline{RD}$ Asserted	t_{WRRD}	6.8	—	ns
$\overline{RD}$ Deasserted to $\overline{RD}$ Asserted	t_{RDRD}	0	—	ns
$\overline{WR}$ Deasserted to $\overline{WR}$ Asserted	t_{WRWR}	14.1	—	ns
$\overline{RD}$ Deasserted to $\overline{WR}$ Asserted	t_{RDWR}	12.8	—	ns

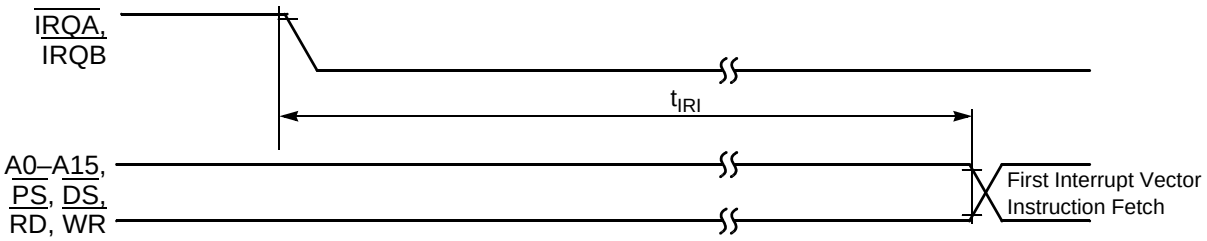


Figure 3-15 Interrupt from Wait State Timing

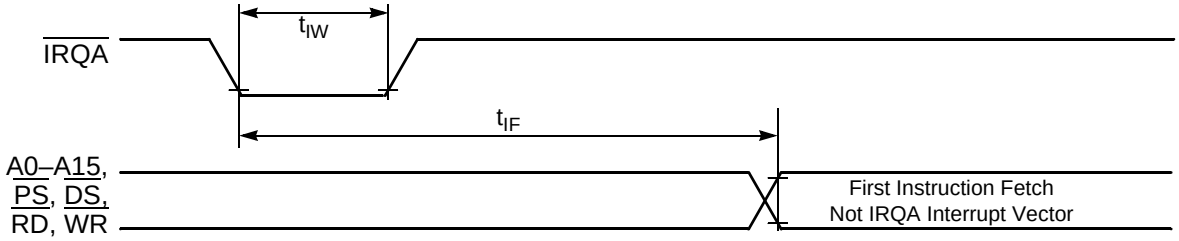


Figure 3-16 Recovery from Stop State Using Asynchronous Interrupt Timing

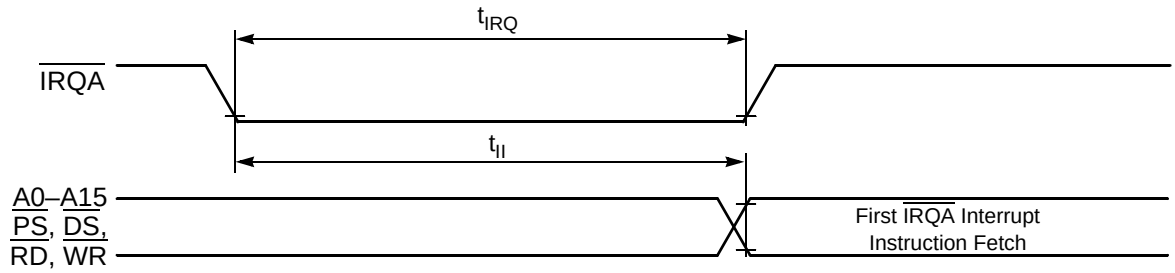


Figure 3-17 Recovery from Stop State Using IRQA Interrupt Service

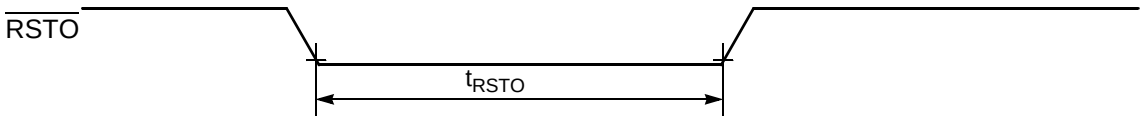


Figure 3-18 Reset Output Timing

3.13 JTAG Timing

Table 3-18 JTAG Timing[1, 3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
TCK frequency of operation[2]	f_{OP}	DC	10	MHz
TCK cycle time	t_{CY}	100	—	ns
TCK clock pulse width	t_{PW}	50	—	ns
TMS, TDI data set-up time	t_{DS}	0.4	—	ns
TMS, TDI data hold time	t_{DH}	1.2	—	ns
TCK low to TDO data valid	t_{DV}	—	26.6	ns
TCK low to TDO tri-state	t_{TS}	—	23.5	ns
$\overline{\text{TRST}}$ assertion time	t_{TRST}	50	—	ns
$\overline{\text{DE}}$ assertion time	t_{DE}	4T	—	ns

1. Timing is both wait state and frequency dependent. For the values listed, T = clock cycle. For 80MHz operation, T = 12.5ns.
2. TCK frequency of operation must be less than 1/8 the processor rate.
3. Parameters listed are guaranteed by design.

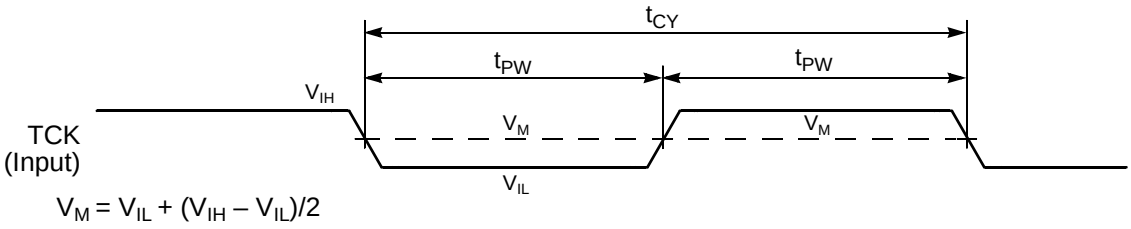


Figure 3-29 Test Clock Input Timing Diagram

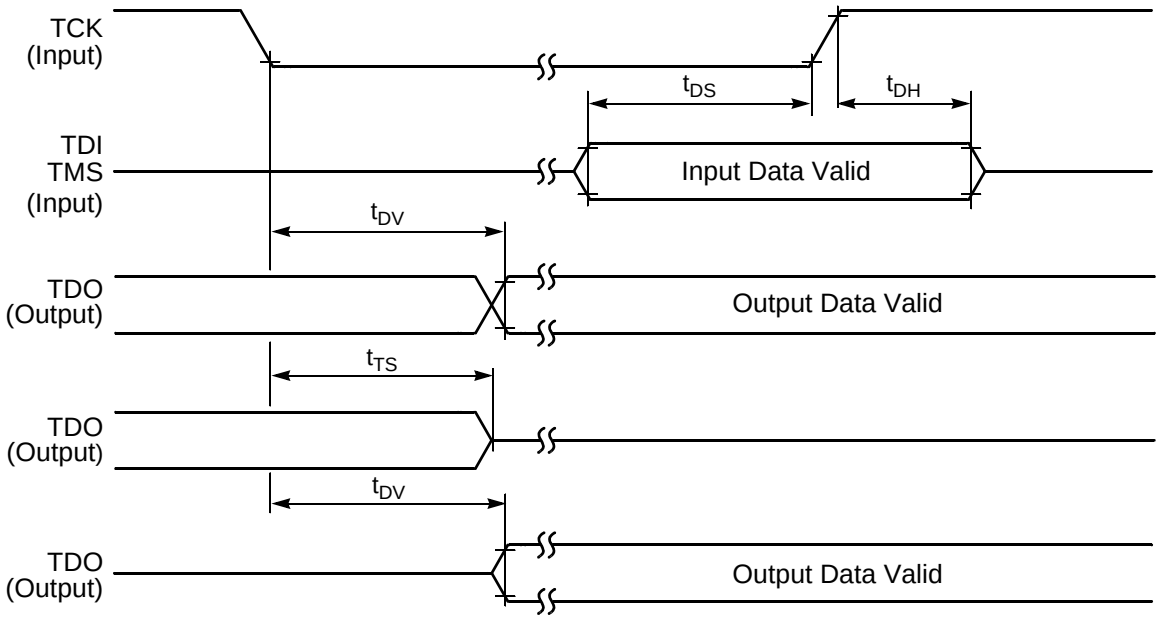
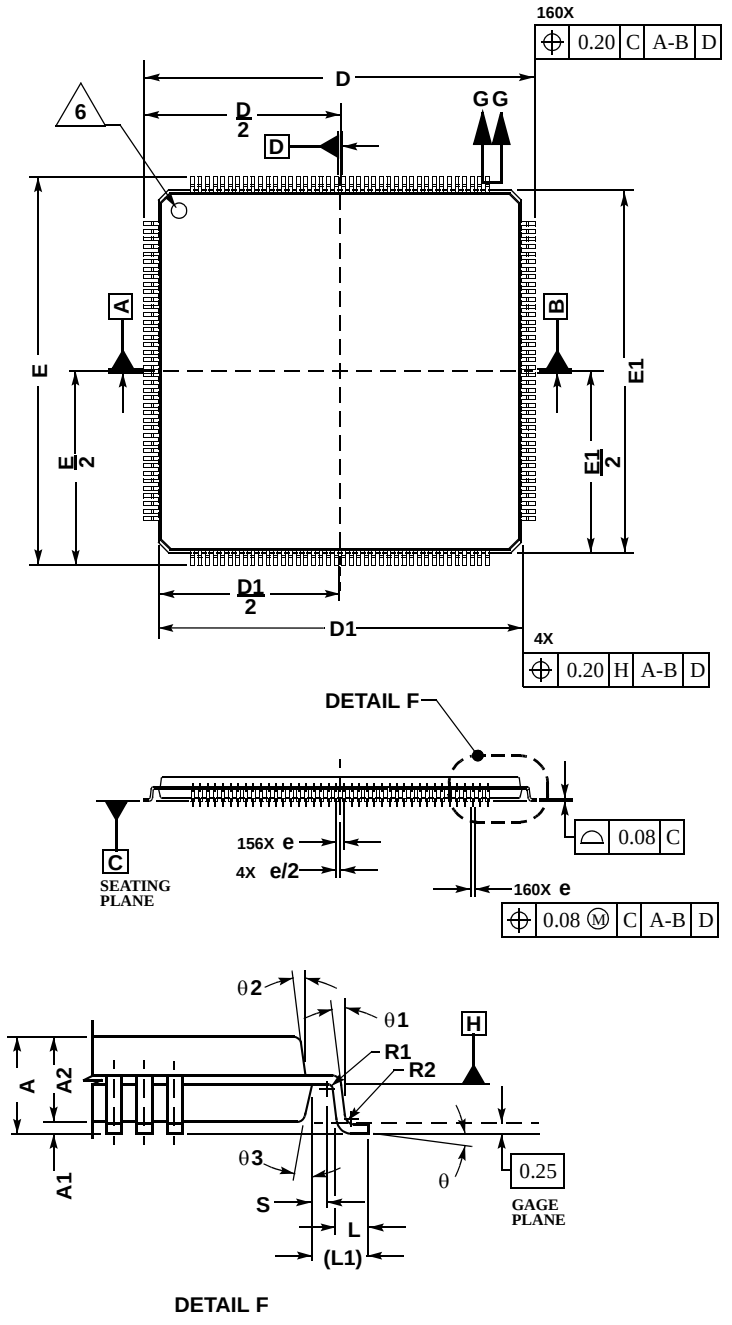
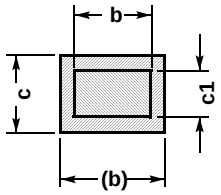


Figure 3-30 Test Access Port Timing Diagram

Figure 3-31 $\overline{\text{TRST}}$ Timing Diagram

Figure 3-32 OnCE—Debug Event





SECTION G-G

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED WHERE THE LEADS EXIT THE PLASTIC BODY AT DATUM PLANE H.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN A PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.
6. EXACT SHAPE OF CORNERS MAY VARY.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16
D	26.00 BSC	
D1	24.00 BSC	
e	0.50 BSC	
E	26.00 BSC	
E1	24.00 BSC	
L	0.45	0.75
L1	1.00 REF	
R1	0.08	---
R2	0.08	0.20
S	0.20	---
θ	0°	7°
θ1	0°	---
θ2	11°	13°
θ3	11°	13°

CASE 1259-01
ISSUE O

Figure 4-2 160-pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.

Table 4-1 56F807 LQFP Package Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	A0	41	GPIOB1	81	PWMA5	121	$\overline{DE}$
2	A1	42	GPIOB2	82	FAULTA0	122	V_{SS}
3	A2	43	GPIOB3	83	FAULTA1	123	ISA0
4	A3	44	GPIOB4	84	FAULTA2	124	ISA1
5	A4	45	GPIOB5	85	FAULTA3	125	ISA2
6	A5	46	GPIOB6	86	EXTBOOT	126	TD0
7	A6	47	GPIOB7	87	V_{SSA}	127	TD1
8	A7	48	V_{SS}	88	V_{DDA}	128	TD2
9	V_{DD}	49	GPIOD0	89	V_{DD}	129	TD3
10	A8	50	GPIOD1	90	V_{SS}	130	TC0
11	A9	51	GPIOD2	91	V_{SS}	131	TC1
12	A10	52	GPIOD3	92	XTAL	132	$\overline{TRST}$
13	A11	53	GPIOD4	93	EXTAL	133	TCS
14	A12	54	GPIOD5	94	V_{DD}	134	TCK
15	A13	55	TXD1	95	V_{SS}	135	TMS
16	A14	56	RXD1	96	V_{DD}	136	TDI
17	A15	57	PWMB0	97	$\overline{RSTO}$	137	TDO
18	V_{SS}	58	PWMB1	98	$\overline{RESET}$	138	VCAPC2
19	$\overline{PS}$	59	PWMB2	99	VREF	139	MSCAN_TX
20	$\overline{DS}$	60	PWMB3	100	V_{DDA}	140	V_{DD}
21	$\overline{WR}$	61	PWMB4	101	V_{SSA}	141	V_{SS}
22	$\overline{RD}$	62	PWMB5	102	ANA0	142	MSCAN_RX
23	D0	63	V_{DD}	103	ANA1	143	$\overline{SS}$
24	D1	64	ISB0	104	ANA2	144	SCLK
25	D2	65	VCAPC1	105	ANA3	145	MISO
26	D3	66	ISB1	106	ANA4	146	MOSI
27	D4	67	ISB2	107	ANA5	147	PHA0
28	D5	68	VPP2	108	ANA6	148	PHB0
29	D6	69	$\overline{IRQA}$	109	ANA7	149	INDEX0
30	D7	70	$\overline{IRQB}$	110	VREF2	150	HOME0

Table 4-2 160 MAPBGA Package Pin Identification by Pin Number

Solder Ball	Signal Name	Solder Ball	Signal Name	Solder Ball	Signal Name	Solder Ball	Signal Name
C3	A0	N4	GPIOB5	K12	V_{SSA}	E10	TC1
B2	A1	P4	GPIOB6	K13	V_{DDA}	D9	$\overline{TRST}$
D3	A2	M4	GPIOB7	L14	V_{DD}	B9	TCS
C2	A3	L5	V_{SS}	K11	V_{SS}	E9	TCK
B1	A4	N5	GPIOD0	K14	V_{SS}	A9	TMS
D2	A5	P5	GPIOD1	J13	XTAL	D8	TDI
C1	A6	K5	GPIOD2	J12	EXTAL	B8	TDO
D1	A7	N6	GPIOD3	J14	V_{DD}	A8	VCAPC2
E3	V_{DD}	L6	GPIOD4	J11	V_{SS}	E8	MSCAN_TX
E2	A8	K6	GPIOD5	H13	V_{DD}	D7	V_{DD}
E1	A9	P6	TXD1	H12	$\overline{RSTO}$	E7	V_{SS}
F3	A10	N7	RXD1	H14	$\overline{RESET}$	D6	MSCAN_RX
F2	A11	L7	PWMB0	H11	VREF	H1	D1
F1	A12	P7	PWMB1	G12	V_{DDA}	H2	D2
G3	A13	K7	PWMB2	G11	V_{SSA}	J3	D3
G2	A14	L8	PWMB3	G14	ANA0	J1	D4
G1	A15	K8	PWMB4	B13	$\overline{DE}$	J2	D5
F4	V_{SS}	P8	PWMB5	A14	V_{SS}	K3	D6
G4	$\overline{PS}$	L9	V_{DD}	B12	ISA0	K1	D7
H4	$\overline{DS}$	N8	ISB0	A13	ISA1	L1	D8
J4	$\overline{WR}$	P14	PWMA5	A12	ISA2	K2	D9
K4	$\overline{RD}$	M13	FAULTA0	B11	TD0	L3	D10

- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back-calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

5.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Use the following list of considerations to assure correct operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the controller, and from the board ground to each V_{SS} pin.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as close as possible to the package supply pins. The recommended bypass configuration is to place one bypass capacitor on each of the V_{DD}/V_{SS} pairs, including V_{DDA}/V_{SSA}. Ceramic and tantalum capacitors tend to provide better performance tolerances.

How to Reach Us:

Home Page:
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E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
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Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
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