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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	120KB (60K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BGA
Supplier Device Package	160-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f807vf80e

Document Revision History

Version History	Description of Change
Rev. 16	Added revision history. Added this text to footnote 2 in **Table 3-8**: “However, the high pulse width does not have to be any particular percent of the low pulse width.”

1.4 Product Documentation

The four documents listed in **Table 1-1** are required for a complete description and proper design with the 56F807. Documentation is available from local Freescale distributors, Freescale Semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com**.

Table 1-1 56F807 Chip Documentation

Topic	Description	Order Number
56800E Family Manual	Detailed description of the 56800 family architecture, and 16-bit core processor and the instruction set	56800EFM
DSP56F801/803/805/807 User's Manual	Detailed description of memory, peripherals, and interfaces of the 56F801, 56F803, 56F805, and 56F807	DSP56F801-7UM
56F807 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions (this document)	DSP56F807
56F807 Errata	Details any chip issues that might be present	56F807E

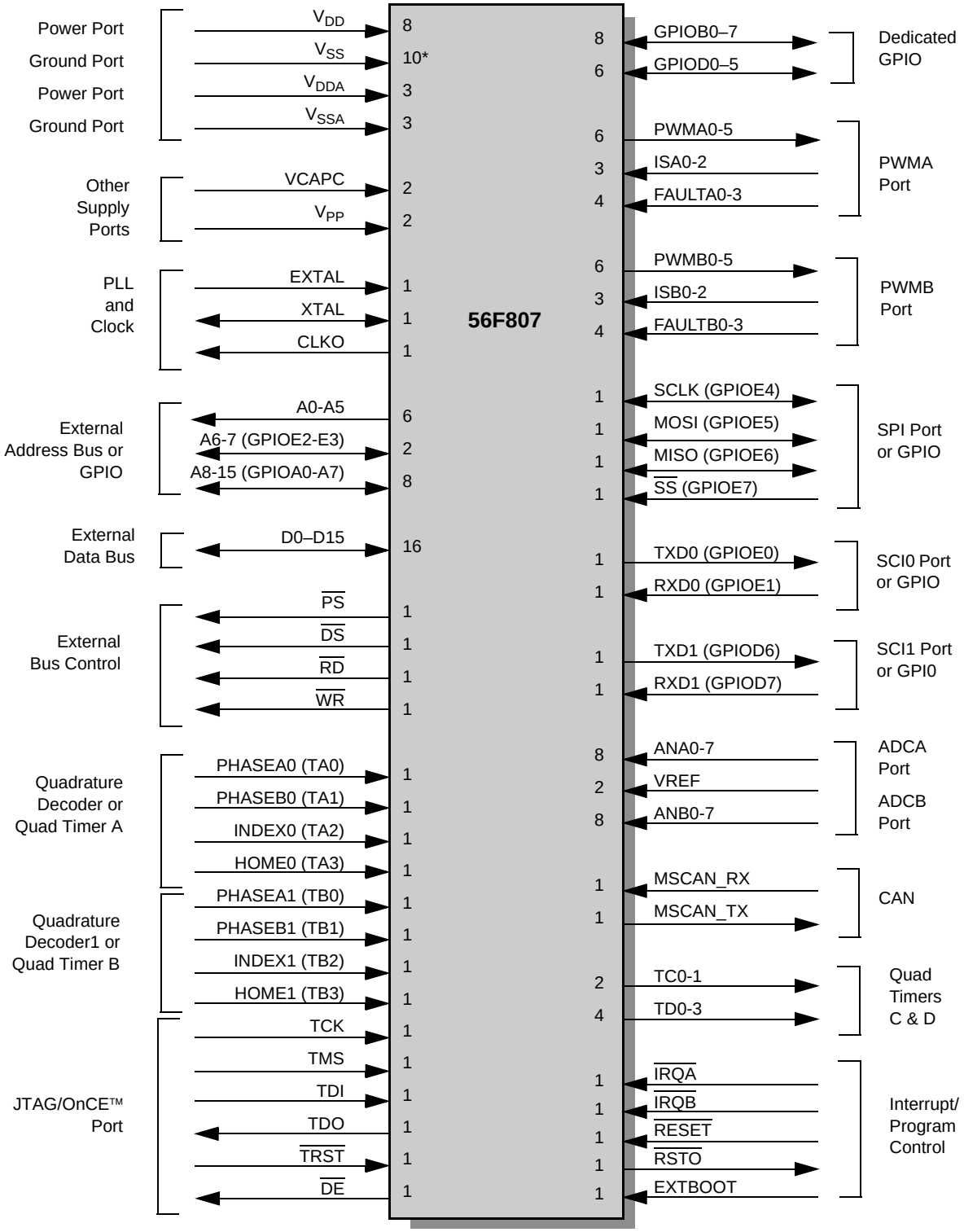
1.5 Data Sheet Conventions

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:	Signal/Symbol	Logic State	Signal State	Voltage[1]
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.



*includes TCS pin which is reserved for factory use and is tied to VSS

Figure 2-1 56F807 Signals Identified by Functional Group[1]

1. Alternate pin functionality is shown in parenthesis.

2.10 Serial Communications Interface (SCI) Signals

Table 2-14 Serial Peripheral Interface (SPI) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MISO**	Input/ Output	Input	**SPI Master In/Slave Out (MISO)**—This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected.
	GPIOE6	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MISO.
1	**MOSI**	Input/ Output	Input	**SPI Master Out/Slave In (MOSI)**—This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge that the slave device uses to latch the data.
	GPIOE5	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is MOSI.
1	**SCLK**	Input/Output	Input	**SPI Serial Clock**—In master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input.
	GPIOE4	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCLK.
1	**$\overline{\text{SS}}$**	Input	Input	**SPI Slave Select**—In master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave.
	GPIOE7	Input/Output	Input	**Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is $\overline{\text{SS}}$.

Table 2-15 Serial Communications Interface (SCI0 and SCI1) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0** **GPIOE0**	Output Input/Output	Input Input	**Transmit Data (TXD0)**—transmit data output **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI output.
1	**RXD0** **GPIOE1**	Input Input/Output	Input Input	**Receive Data (RXD0)**— receive data input **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI input.
1	**TXD1** **GPIOD6**	Output Input/Output	Input Input	**Transmit Data (TXD1)**—transmit data output **Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI output.
1	**RXD1** **GPIOD7**	Input Input/Output	Input Input	**Receive Data (RXD1)**— receive data input **Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI input.

2.11 CAN Signals

Table 2-16 CAN Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MSCAN_ RX**	Input (Schmitt)	Input	**MSCAN Receive Data**—MSCAN input. This pin has an internal pull-up resistor.
1	**MSCAN_ TX**	Output	Output	**MSCAN Transmit Data**—MSCAN output. CAN output is open-drain output and pull-up resistor is needed.

2.12 Analog-to-Digital Converter (ADC) Signals

Table 2-17 Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANA0-3**	Input	Input	**ANA0-3**—Analog inputs to ADCA channel 1
4	**ANA4-7**	Input	Input	**ANA4-7**—Analog inputs to ADCA channel 2
2	**VREF**	Input	Input	**VREF**—Analog reference voltage for ADC. Must be set to V_{DDA}-0.3V for optimal performance.
4	**ANB0-3**	Input	Input	**ANB0-3**—Analog inputs to ADCB, channel 1
4	**ANB4-7**	Input	Input	**ANB4-7**—Analog inputs to ADCB, channel 2

2.13 Quad Timer Module Signals

Table 2-18 Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**TC0-1**	Input/Output	Input	**TC0-1**—Timer C Channels 0 and 1
4	**TD0-3**	Input/Output	Input	**TD0-3**—Timer D Channels 0, 1, 2, and 3

damage to the device.

The 56F807 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Analog inputs, ANA0-7 and VREF	V_{IN}	V_{SSA}– 0.3	V_{DDA}+ 0.3	V
Analog inputs EXTAL and XTAL	V_{IN}	V_{SSA}– 0.3	V_{SSA}+ 3.0	V
Current drain per pin excluding V_{DD}, V_{SS}, PWM outputs, TCS, VPP, V_{DDA}, V_{SSA}	I	—	10	mA

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, digital	V_{DD}	3.0	3.3	3.6	V
Supply Voltage, analog	V_{DDA}	3.0	3.3	3.6	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V

4. Thermal Characterization Parameter, Psi-JT (Ψ_{JT}), is the “resistance” from junction to reference point thermocouple on top center of case as defined in JESD51-2. Ψ_{JT} is a useful value to use to estimate junction temperature in steady state customer environments.
5. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
6. See Section 5.1 from more details on thermal design considerations.
7. TJ = Junction Temperature
   TA = Ambient Temperature

3.2 DC Electrical Characteristics

Table 3-4 DC Electrical Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Input high voltage (XTAL/EXTAL)	V_{IHC}	2.25	—	2.75	V
Input low voltage (XTAL/EXTAL)	V_{ILC}	0	—	0.5	V
Input high voltage (Schmitt trigger inputs)[1]	V_{IHS}	2.2	—	5.5	V
Input low voltage (Schmitt trigger inputs)[1]	V_{ILS}	-0.3	—	0.8	V
Input high voltage (all other digital inputs)	V_{IH}	2.0	—	5.5	V
Input low voltage (all other digital inputs)	V_{IL}	-0.3	—	0.8	V
Input current high (pullup/pulldown resistors disabled, $V_{IN}=V_{DD}$)	I_{IH}	-1	—	1	µA
Input current low (pullup/pulldown resistors disabled, $V_{IN}=V_{SS}$)	I_{IL}	-1	—	1	µA
Input current high (with pullup resistor, $V_{IN}=V_{DD}$)	I_{IHPU}	-1	—	1	µA
Input current low (with pullup resistor, $V_{IN}=V_{SS}$)	I_{ILPU}	-210	—	-50	µA
Input current high (with pulldown resistor, $V_{IN}=V_{DD}$)	I_{IHPD}	20	—	180	µA
Input current low (with pulldown resistor, $V_{IN}=V_{SS}$)	I_{ILPD}	-1	—	1	µA
Nominal pullup or pulldown resistor value	R_{PU}, R_{PD}		30		KΩ
Output tri-state current low	I_{OZL}	-10	—	10	µA
Output tri-state current high	I_{OZH}	-10	—	10	µA
Input current high (analog inputs, $V_{IN}=V_{DDA}$)[2]	I_{IHA}	-15	—	15	µA
Input current low (analog inputs, $V_{IN}=V_{SSA}$)[3]	I_{ILA}	-15	—	15	µA
Output High Voltage (at IOH)	V_{OH}	V_{DD} – 0.7	—	—	V

Table 3-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Output Low Voltage (at IOL)	V_{OL}	—	—	0.4	V
Output source current	I_{OH}	4	—	—	mA
Output source current	I_{OL}	4	—	—	mA
PWM pin output source current[3]	I_{OHP}	10	—	—	mA
PWM pin output sink current[4]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current	I_{DDT}[5]				
Run [6]		—	195	220	mA
Wait[7]		—	170	200	mA
Stop		—	115	145	mA
Low Voltage Interrupt, external power supply[8]	V_{EIO}	2.4	2.7	3.0	V
Low Voltage Interrupt, internal power supply[9]	V_{EIC}	2.0	2.2	2.4	V
Power on Reset[10]	V_{POR}	—	1.7	2.0	V

1. Schmitt Trigger inputs are: EXTBOOT, IRQA, IRQB, RESET, TCS, ISA0-2, FAULTA0-3, ISB0-2, FAULTB0-3, TCK, TRST, TMS, TDI, and MSCAN_RX

2. Analog inputs are: ANA[0:7], XTAL and EXTAL. Specification assumes ADC is not sampling.

3. PWM pin output source current measured with 50% duty cycle.

4. PWM pin output sink current measured with 50% duty cycle.

5. $I_{DDT} = I_{DD} + I_{DDA}$ (Total supply current for $V_{DD} + V_{DDA}$)

6. Run (operating) I_{DD} measured using 8MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.

7. Wait I_{DD} measured using external square wave clock source (f_{osc} = 8MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50pF on all outputs. C_L = 20pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.

8. This low voltage interrupt monitors the V_{DDA} external power supply. V_{DDA} is generally connected to the same potential as V_{DD} via separate traces. If V_{DDA} drops below V_{EIO}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DDA} \geq V_{EIO}$ (between the minimum specified V_{DD} and the point when the V_{EIO} interrupt is generated).

9. This low voltage interrupt monitors the internally regulated core power supply. If the output from the internal voltage is regulator drops below V_{EIC}, an interrupt is generated. Since the core logic supply is internally regulated, this interrupt will not be generated unless the external power supply drops below the minimum specified value (3.0V).

10. Power–on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active as long as the internal 2.5V is below 1.5V typical, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

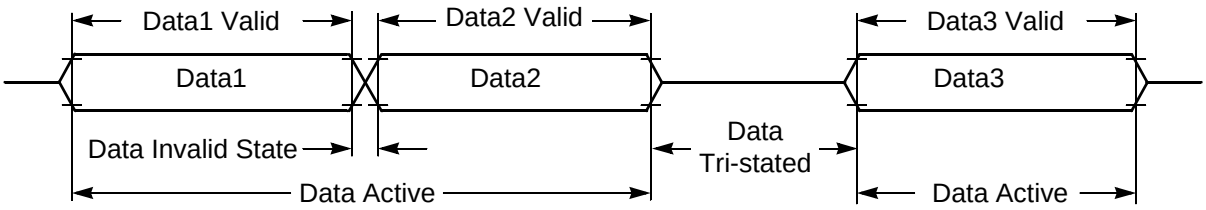


Figure 3-3 Signal States

Table 3-5 Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE=0
2. Y address enable, YMUX is disabled when YE=0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE=0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 3-6 IFREN Truth Table

Mode	IFREN=1	IFREN=0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

Table 3-7 Flash Timing Parameters

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF

Characteristic	Symbol	Min	Typ	Max	Unit	Figure
Program time	T_{prog}*	20	–	–	us	Figure 3-4
Erase time	T_{erase}*	20	–	–	ms	Figure 3-5
Mass erase time	T_{me}*	100	–	–	ms	Figure 3-6
Endurance[1]	E_{CYC}	10,000	20,000	–	cycles	
Data Retention[1]	D_{RET}	10	30	–	years	
The following parameters should only be used in the Manual Word Programming Mode						
PROG/ERASE to NVSTR set up time	T_{nvs}*	–	5	–	us	Figure 3-4, Figure 3-5, Figure 3-6
NVSTR hold time	T_{nvh}*	–	5	–	us	Figure 3-4, Figure 3-5
NVSTR hold time (mass erase)	T_{nvh1}*	–	100	–	us	Figure 3-6
NVSTR to program set up time	T_{pgs}*	–	10	–	us	Figure 3-4
Recovery time	T_{rcv}*	–	1	–	us	Figure 3-4, Figure 3-5, Figure 3-6
Cumulative program HV period[2]	T_{hv}	–	3	–	ms	Figure 3-4
Program hold time[3]	T_{pgh}	–	–	–		Figure 3-4
Address/data set up time[3]	T_{ads}	–	–	–		Figure 3-4
Address/data hold time[3]	T_{adh}	–	–	–		Figure 3-4

1. One cycle is equal to an erase program and read.
2. Thv is the cumulative high voltage programming time to the same row before next erase. The same address cannot be programmed twice before next erase.
3. Parameters are guaranteed by design in smart programming mode and must be one cycle or greater.

*The Flash interface unit provides registers for the control of these parameters.

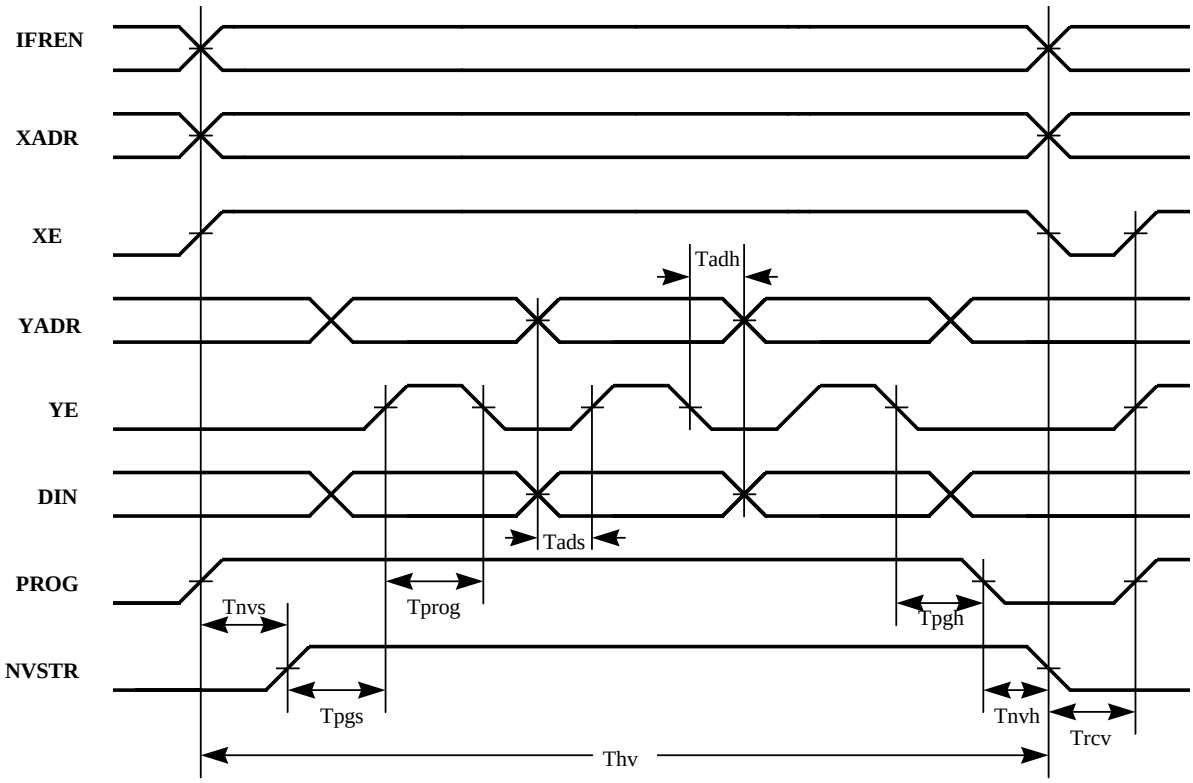


Figure 3-4 Flash Program Cycle

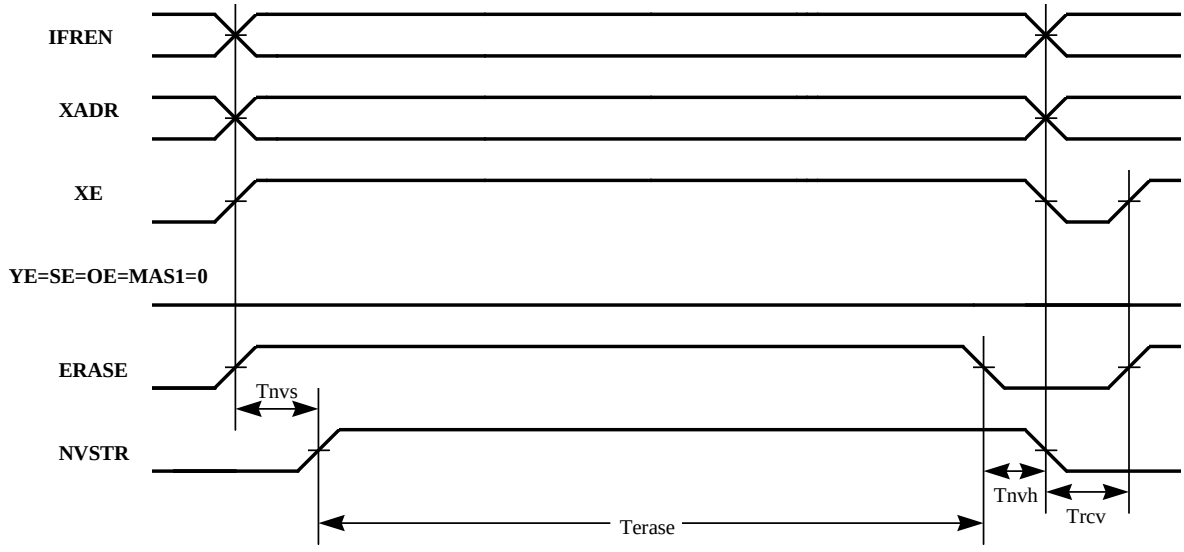


Figure 3-5 Flash Erase Cycle

1. Timing is both wait state and frequency dependent. In the formulas listed, WS = the number of wait states and T = Clock Period. For 80MHz operation, T = 12.5ns.

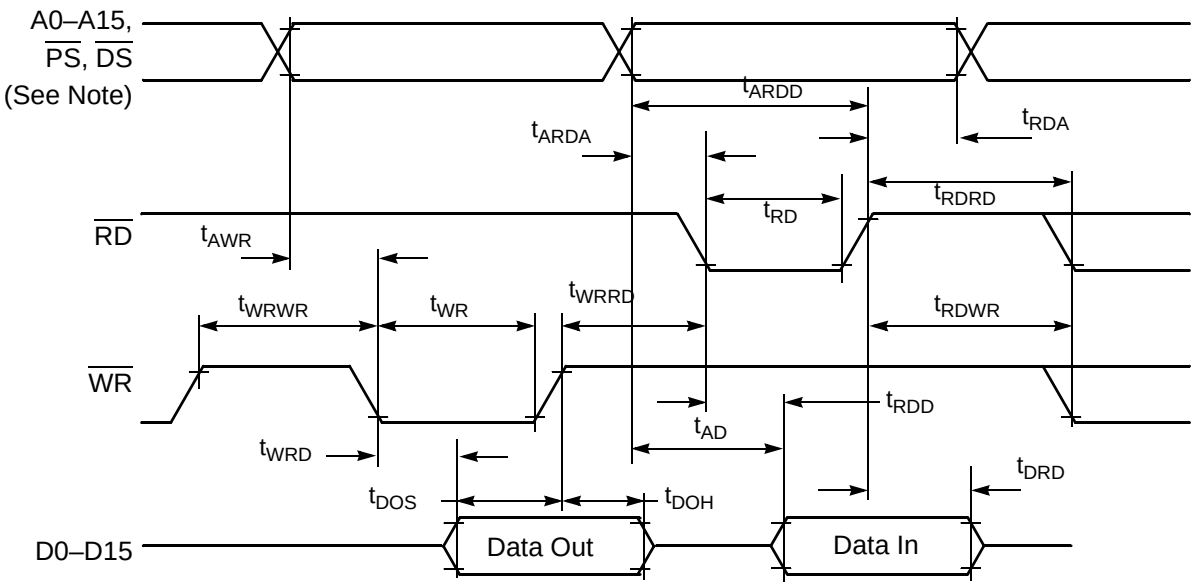
2. Parameters listed are guaranteed by design.

To calculate the required access time for an external memory for any frequency < 80MHz, use this formula:

Top = Clock period @ desired operating frequency

WS = Number of wait states

Memory Access Time = (Top*WS) + (Top- 11.5)



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 3-11 External Bus Asynchronous Timing

3.6 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 3-11 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1,5]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	3-12
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	3-12
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	33T	34T	ns	3-12
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	3-13
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	15T	—	ns	3-14
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	16T	—	ns	3-14
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[3]	t_{IRI}	13T	—	ns	3-15
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[4]	t_{IW}	2T	—	ns	3-16
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IF}	 — —	 275,000T 12T	 ns ns	3-16
Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IRQ}	 — —	 275,000T 12T	 ns ns	3-17
Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{II}	 — —	 275,000T 12T	 ns ns	3-17

1. In the formulas, T = clock cycle. For an operating frequency of 80MHz, T = 12.5ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   - After power-on reset
   - When recovering from Stop state
3. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
4. The interrupt instruction fetch is visible on the pins only in Mode 3.
5. Parameters listed are guaranteed by design.

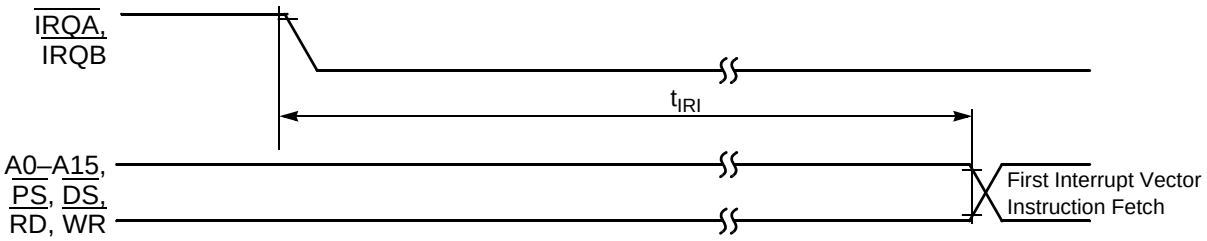


Figure 3-15 Interrupt from Wait State Timing

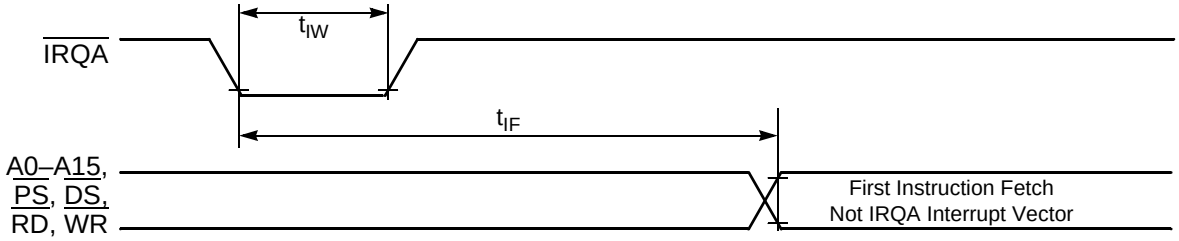


Figure 3-16 Recovery from Stop State Using Asynchronous Interrupt Timing

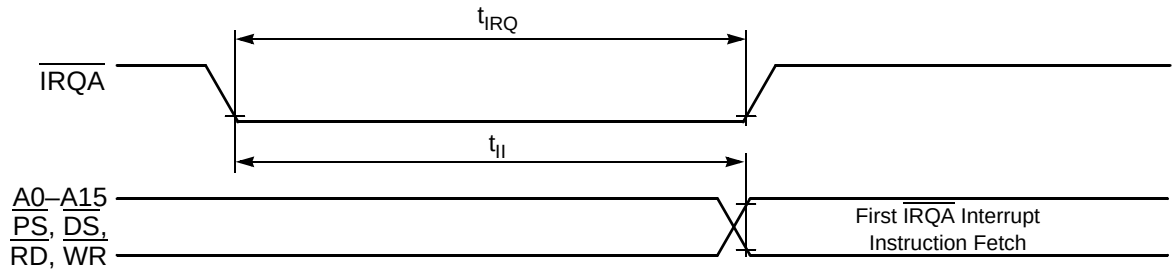


Figure 3-17 Recovery from Stop State Using IRQA Interrupt Service

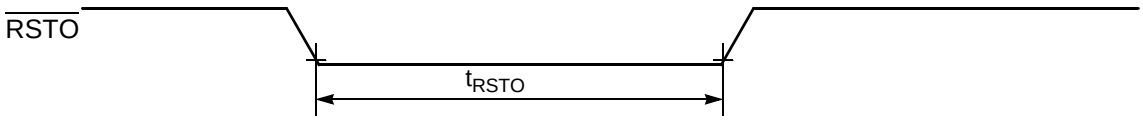


Figure 3-18 Reset Output Timing

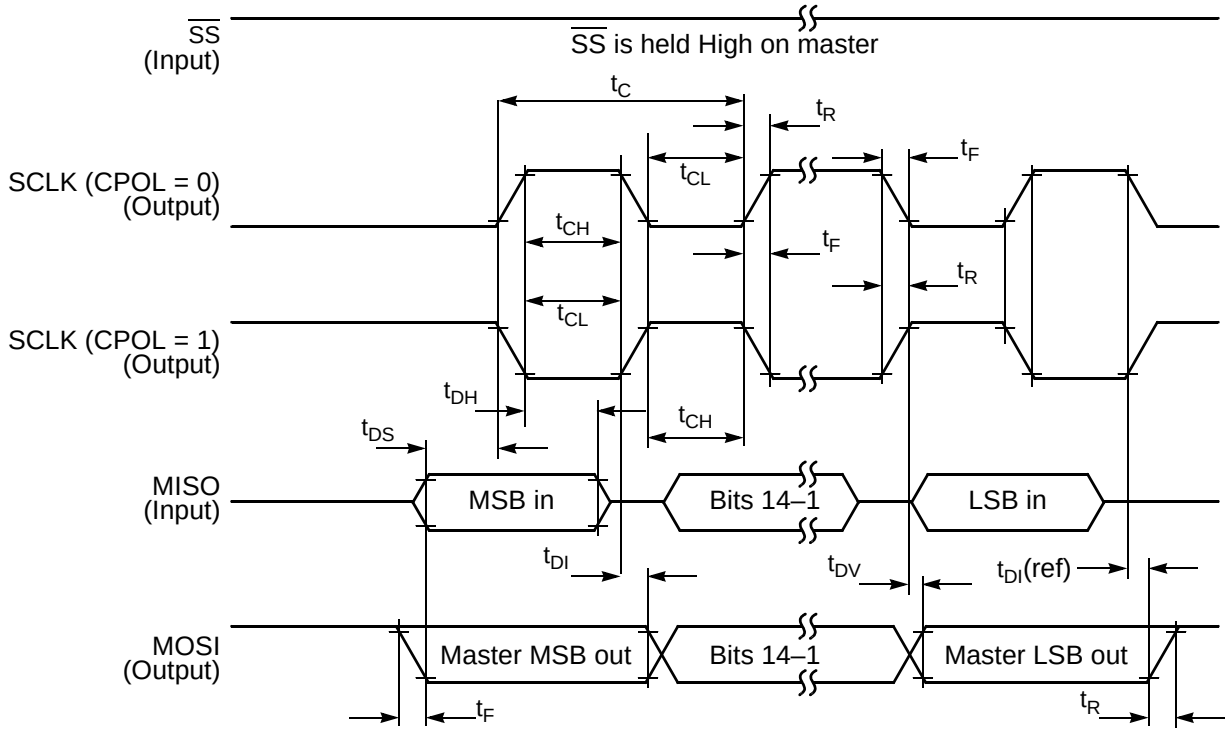


Figure 3-19 SPI Master Timing (CPHA = 0)

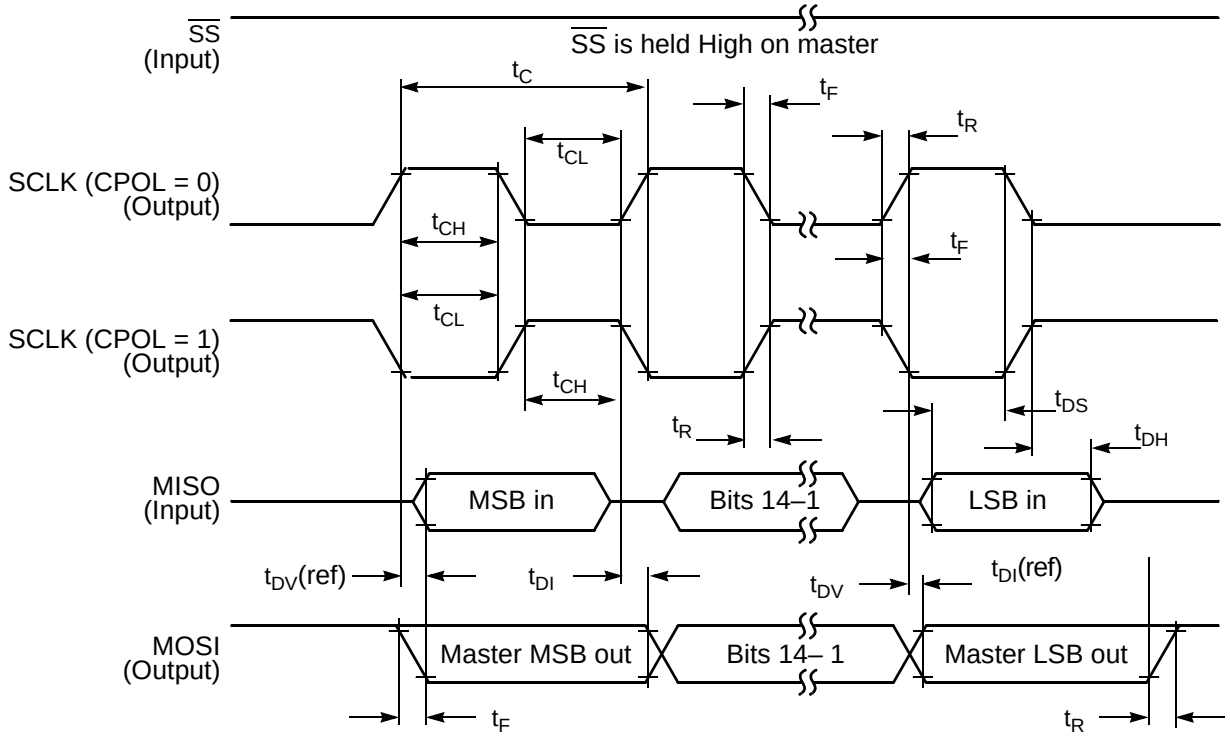


Figure 3-20 SPI Master Timing (CPHA = 1)

3.11 Analog-to-Digital Converter (ADC) Characteristics

Table 3-16 ADC Characteristics

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $V_{REF} = V_{DD}$-0.3V, ADCDIV = 4, 9, or 14, (for optimal performance), ADC clock = 4MHz, 3.0–3.6 V, $T_A = –40°$ to +85°C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
ADC input voltages	V_{ADCIN}	0[1]	—	V_{REF}[2]	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[3]	INL	—	+/- 2.5	+/- 4	LSB[4]
Differential Non-Linearity	DNL	—	+/- 0.9	+/- 1	LSB[4]
Monotonicity	GUARANTEED				
ADC internal clock[5]	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{SSA}	—	V_{DDA}	V
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[6]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[6]
Input capacitance	C_{ADI}	—	5	—	pF[6]
Gain Error (transfer gain)[5]	E_{GAIN}	0.93	1.00	1.08	—
Total Harmonic Distortion[5]	THD	60	64	—	
Offset Voltage[5]	V_{OFFSET}	-90	-25	+10	mV
Signal-to-Noise plus Distortion[5]	SINAD	55	60	—	—
Effective Number of Bits[5]	ENOB	9	10	—	bit
Spurious Free Dynamic Range[5]	SFDR	65	70	—	dB
Bandwidth	BW	—	100	—	KHz
ADC Quiescent Current (each dual ADC)	I_{ADC}	—	50	—	mA
V_{REF} Quiescent Current (each dual ADC)	I_{VREF}	—	12	16.5	mA

1. For optimum ADC performance, keep the minimum V_{ADCIN} value ≥ 25mV. Inputs less than 25mV may convert to a digital output code of 0.
2. V_{REF} must be equal to or less than V_{DDA} and must be greater than 2.7V. For optimal ADC performance, set V_{REF} to V_{DDA}-0.3V.
3. Measured in 10-90% range.
4. LSB = Least Significant Bit.
5. Guaranteed by characterization.
6. $t_{AIC} = 1/f_{ADIC}$

- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} pins are less than 0.5 inch per capacitor lead.
- Bypass the V_{DD} and V_{SS} layers of the PCB with approximately 100 µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the controller's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the VREF, V_{DDA} and V_{SSA} pins.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. $\overline{\text{TRST}}$ must be asserted at power up for proper operation. Designs that do not require debugging functionality, such as consumer products, $\overline{\text{TRST}}$ should be tied low.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

Part 6 Ordering Information

Table 6-1 lists the pertinent information needed to place an order. Consult a Freescale Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 6-1 56F807 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Ambient Frequency (MHz)	Order Number
56F807	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	80	DSP56F807PY80
56F807	3.0–3.6 V	Mold Array Process Ball Grid Array (MAPBGA)	160	80	DSP56F807VF80
56F807	3.0–3.6 V	Low-Profile Quad Flat Pack (LQFP)	160	80	DSP56F807PY80E*
56F807	3.0–3.6 V	Mold Array Process Ball Grid Array (MAPBGA)	160	80	DSP56F807VF80E*

*This package is RoHS compliant.