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Details	
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Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 1x5b, 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	14-SOIC
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REGISTER 7-4: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PWM6IE(1)	PWM5IE	COG1IE	ZCDIE	COG2IE(1)	CLC3IE	CLC2IE	CLC1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **PWM6IE:** PWM6 Interrupt Enable bit(1)
- 1 = PWM6 interrupt is enabled
- 0 = PWM6 interrupt is disabled

bit 6 **PWM5IE:** PWM5 Interrupt Enable bit
- 1 = PWM5 interrupt is enabled
- 0 = PWM5 interrupt is disabled

bit 5 **COG1IE:** COG1 Auto-Shutdown Interrupt Enable bit
- 1 = COG1 interrupt is enabled
- 0 = COG1 interrupt is disabled

bit 4 **ZCDIE:** Zero-Cross Detection Interrupt Enable bit
- 1 = ZCD interrupt is enabled
- 0 = ZCD interrupt is disabled

bit 3 **COG2IE:** COG2 Auto-Shutdown Interrupt Enable bit(1)
- 1 = COG2 interrupt is enabled
- 0 = COG2 interrupt is disabled

bit 2 **CLC3IE:** CLC3 Interrupt Enable bit
- 1 = CLC3 interrupt is enabled
- 0 = CLC3 interrupt is disabled

bit 1 **CLC2IE:** CLC2 Interrupt Enable bit
- 1 = CLC2 interrupt is enabled
- 0 = CLC2 interrupt is disabled

bit 0 **CLC1IE:** CLC1 Interrupt Enable bit
- 1 = CLC1 interrupt is enabled
- 0 = CLC1 interrupt is disabled

Note 1: PIC16(L)F1768/9 only.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 7-7: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PWM6IF(1)	PWM5IF	COG1IF	ZCDIF	COG2IF(1)	CLC3IF	CLC2IF	CLC1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **PWM6IF:** PWM6 Interrupt Flag bit(1)
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 6 **PWM5IF:** PWM5 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 5 **COG1IF:** COG1 Auto-Shutdown Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 4 **ZCDIF:** Zero-Cross Detection Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 3 **COG2IF:** COG2 Auto-Shutdown Interrupt Flag bit(1)
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 2 **CLC3IF:** CLC3 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 1 **CLC2IF:** CLC2 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 0 **CLC1IF:** CLC1 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

Note 1: PIC16(L)F1768/9 only.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 10-3: PMADRL: PROGRAM MEMORY ADDRESS LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PMADR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **PMADR<7:0>**: Specifies the Least Significant bits for Program Memory Address bits

REGISTER 10-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH BYTE REGISTER

U-1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—(1)	PMADR<14:8>						
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **Unimplemented:** Read as '1'

bit 6-0 **PMADR<14:8>**: Specifies the Most Significant bits for Program Memory Address bits

Note 1: Unimplemented, read as '1'.

12.8 Register Definitions: PPS Input and Output Selections

REGISTER 12-1: xxxPPS: PERIPHERAL xxx INPUT SELECTION

U-0	U-0	U-0	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u	R/W-q/u
—	—	—	xxxPPS<4:3>		xxxPPS<2:0>(1)		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on peripheral

bit 7-5 **Unimplemented:** Read as '0'

bit 4-3 **xxxPPS<4:3>:** Peripheral xxx Input PORT Selection bits

11 = Reserved; do not use
10 = Peripheral input is PORTC
01 = Peripheral input is PORTB(2)
00 = Peripheral input is PORTA

bit 2-0 **xxxPPS<2:0>:** Peripheral xxx Input Bit Selection bits(1)

111 = Peripheral input is from PORTx, bit 7 (Rx7)
110 = Peripheral input is from PORTx, bit 6 (Rx6)
101 = Peripheral input is from PORTx, bit 5 (Rx5)
100 = Peripheral input is from PORTx, bit 4 (Rx4)
011 = Peripheral input is from PORTx, bit 3 (Rx3)
010 = Peripheral input is from PORTx, bit 2 (Rx2)
001 = Peripheral input is from PORTx, bit 1 (Rx1)
000 = Peripheral input is from PORTx, bit 0 (Rx0)

Note 1: See Table 12-1 for xxxPPS register list and Reset values.
2: PIC16(L)F1768/9 only.

REGISTER 12-2: RxyPPS: PIN Rxy OUTPUT SOURCE SELECTION REGISTER

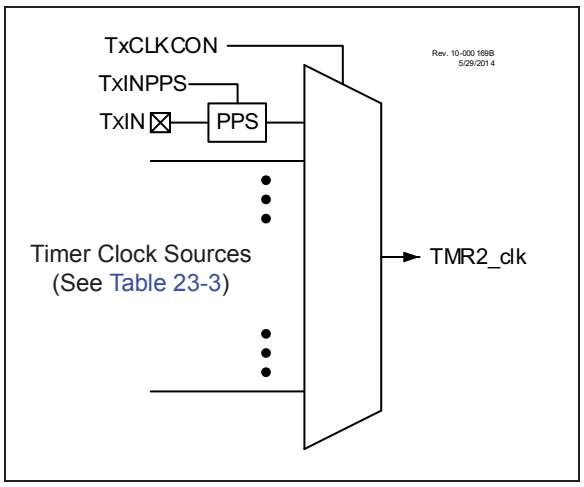
U-0	U-0	U-0	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u
—	—	—	RxyPPS<4:0>				
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **RxyPPS<4:0>:** Pin Rxy Output Source Selection bits
Selection code determines the output signal on the port pin. See Table 12-2 for the selection codes.

FIGURE 23-2: TIMER2 CLOCK SOURCE BLOCK DIAGRAM



23.1 Timer2 Operation

Timer2 operates in three major modes:

- Free-Running Period
- One-Shot
- Monostable

Within each mode, there are several options for starting, stopping and resetting. Table 23-1 lists the options.

In all modes, the TMR2 Count register is incremented on the rising edge of the clock signal from the programmable prescaler. When TMR2 equals T2PR, a high level is output to the postscaler counter. TMR2 is cleared on the next clock input.

An external signal from hardware can also be configured to gate the timer operation or force a TMR2 count Reset. In Gate modes the counter stops when the gate is disabled and resumes when the gate is enabled. In Reset modes the TMR2 count is reset on either the level or edge from the external source.

The T2PR period register is double buffered. Software reads and writes the T2PR register. However, the timer uses a buffered PRx register for operation. Software does not have direct access to the buffered PRx register. The content of the PRx register is transferred to the buffer by any of the following events:

- A write to the TMR2 register
- A write to the T2CON register
- When TMR2 = PRx buffer and the prescaler rolls over
- An external Reset event

The TMR2 register is directly readable and writable. The TMR2 register is cleared and the T2PR register initializes to FFh on any device Reset. Both the prescaler and postscaler counters are cleared on the following events:

- A write to the TMR2 register
- A write to the T2CON register
- Any device Reset
- External Reset source event that resets the timer.

Note: TMR2 is not cleared when T2CON is written.

23.1.1 FREE-RUNNING PERIOD MODE

The value of TMR2 is compared to that of the Period register, T2PR, on each clock cycle. When the two values match, the comparator resets the value of TMR2 to 00h on the next cycle and increments the output postscaler counter. When the postscaler count equals the value in the OUTPS<4:0> bits of the TMRxCON1 register then a one clock period wide pulse occurs on the TMR2_postscaled output, and the postscaler count is cleared.

23.1.2 ONE-SHOT MODE

The One-Shot mode is identical to the Free-Running Period mode except that the ON bit is cleared and the timer is stopped when TMR2 matches T2PR, and will not restart until the T2ON bit is cycled off and on. Postscaler OUTPS<4:0> values other than 0 are meaningless in this mode because the timer is stopped at the first period event and the postscaler is reset when the timer is restarted.

23.1.3 MONOSTABLE MODE

Monostable modes are similar to One-Shot modes except that the ON bit is not cleared and the timer can be restarted by an external Reset event.

23.2 Timer2 Output

The Timer2 module's primary output is TMR2_postscaled, which pulses for a single TMR2_clk period when the postscaler counter matches the value in the OUTPS bits of the TMR2xCON register. The T2PR postscaler is incremented each time the TMR2 value matches the T2PR value. This signal can be selected as an input to several other input modules:

- The ADC module as an auto-conversion trigger
- COG as an auto-shutdown source

In addition, the Timer2 is also used by the CCP module for pulse generation in PWM mode. Both the actual TMR2 value as well as other internal signals are sent to the CCP module to properly clock both the period and pulse width of the PWM signal. See **Section 24.6 "CCP/PWM Clock Selection"** for more details on setting up Timer2 for use with the CCP, as well as the timing diagrams in **Section 23.6 "Operation Examples"** for examples of how the varying Timer2 modes affect CCP PWM output.

23.6 Operation Examples

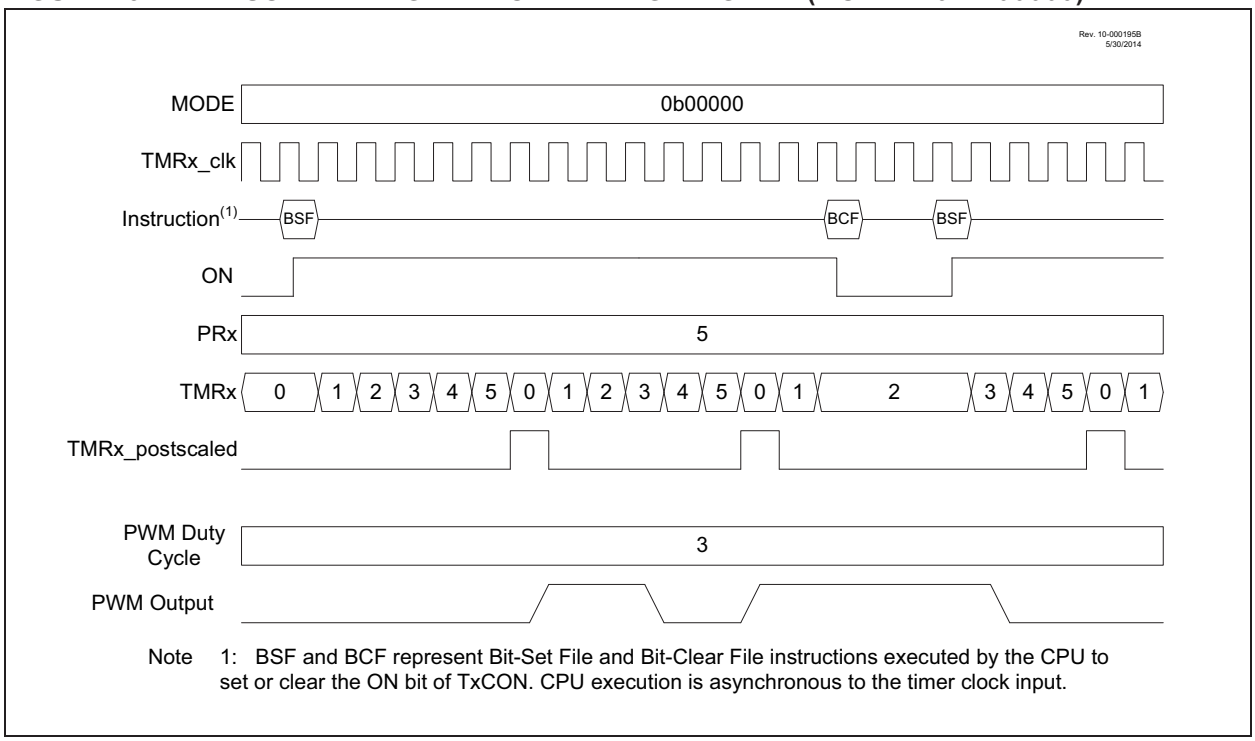
Unless otherwise specified, the following notes apply to the following timing diagrams:

- Both the prescaler and postscaler are set to 1:1 (both the CKPSx and OUTPSx bits in the TxCON register are cleared).
- The diagrams illustrate any clock except FOSC/4 and show clock-sync delays of at least two full cycles for both ON and Timer2_ers. When using FOSC/4, the clock-sync delay is at least one instruction period for Timer2_ers; ON applies in the next instruction period.
- The PWM duty cycle and PWM output are illustrated assuming that the timer is used for the PWM function of the CCP module, as described in **Section 24.6 "CCP/PWM Clock Selection"**. The signals are not a part of the Timer2 module.

23.6.1 SOFTWARE GATE MODE

This mode corresponds to legacy Timer2 operation. The timer increments with each clock input when ON = 1 and does not increment when ON = 0. When the TMRx count equals the PRx period count, the timer resets on the next clock and continues counting from 0. Operation with the ON bit software controlled is illustrated in Figure 23-4. With PRx = 5, the counter advances until TMRx = 5, and goes to zero with the next clock.

FIGURE 23-4: SOFTWARE GATE MODE TIMING DIAGRAM (MODE<4:0> = 00000)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

24.3 PWM Overview

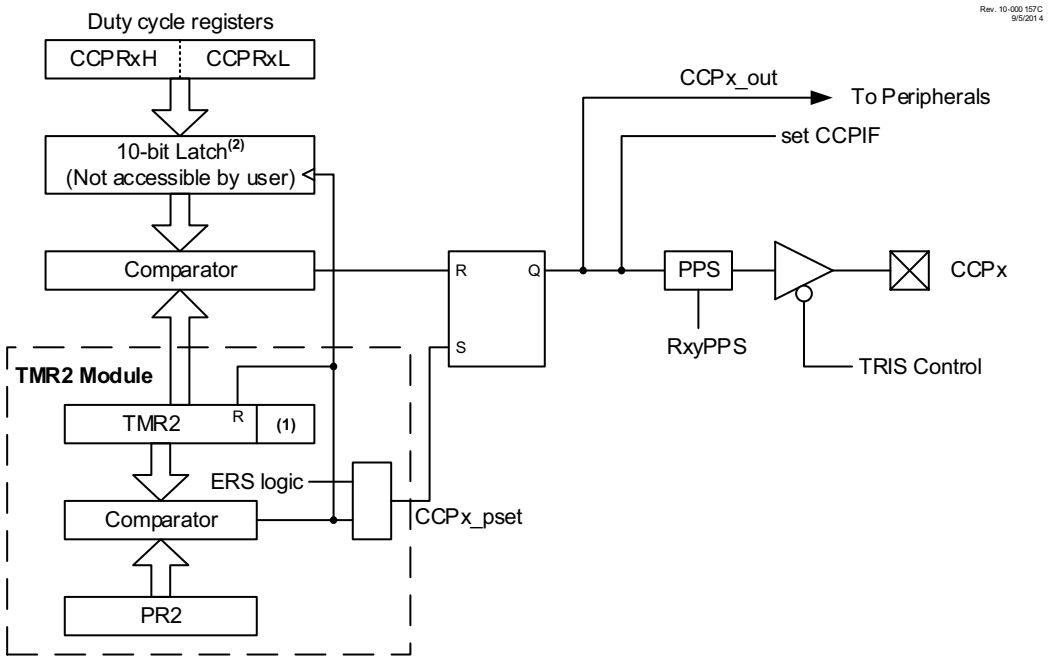
Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse-width time, and in turn, the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 24-3 shows a typical waveform of the PWM signal.

FIGURE 24-3: SIMPLIFIED PWM BLOCK DIAGRAM



Notes: 1. 8-bit timer is concatenated with two bits generated by Fosc or two bits of the internal prescaler to create 10-bit time-base.
2. The alignment of the 10 bits from the CCPR register is determined by the FMT bit.

The maximum PWM resolution is ten bits when T2PR is 255. The resolution is a function of the T2PR register value as shown by Equation 25-4.

Note: If the pulse-width value is greater than the period the assigned PWM pin(s) will remain unchanged.

EQUATION 25-4: PWM RESOLUTION

$$Resolution = \frac{log[4(T2PR + 1)]}{log(2)} \ bits$$

TABLE 25-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	0.31 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	64	4	1	1	1	1
T2PR Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 25-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	0.31 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	64	4	1	1	1	1
T2PR Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

25.7 Operation in Sleep Mode

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

25.8 Changes in System Clock Frequency

The PWM frequency is derived from the system clock frequency (FOSC). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 5.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for additional details.

25.9 Effects of Reset

Any Reset will force all ports to Input mode and the PWM registers to their Reset states.

29.6 Register Definitions: Op Amp Control

Long bit name prefixes for the op amp peripherals are shown in Table 29-1. Refer to **Section 1.1 "Register and Bit Naming Conventions"** for more information.

TABLE 29-1: BIT NAME PREFIXES

Peripheral	Bit Name Prefix
OPA1	OPA1
OPA2(1)	OPA2

Note 1: PIC16(L)F1768/9 devices only.

REGISTER 29-1: OPAxCON: OPERATIONAL AMPLIFIER x (OPAx) CONTROL REGISTER

R/W-0/0	U-0	U-0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	—	UG	—	ORPOL	ORM<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **EN:** Op Amp Enable bit
1 = Op amp is enabled
0 = Op amp is disabled and consumes no active power

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **UG:** Op Amp Unity Gain Select bit
1 = OPA output is connected to inverting input; OPAxIN- pin is available for general purpose I/O
0 = Inverting input is connected to the OPAxIN- pin

bit 3 **Unimplemented:** Read as '0'

bit 2 **ORPOL:** Op Amp Override Source Polarity bit
1 = Override source polarity is inverted; override occurs when source is high
0 = Override source polarity is not inverted; override occurs when source is low

bit 1-0 **ORM<1:0>:** Op Amp Override Mode Selection bits
11 = Reserved; do not use
10 = Op amp is forced to unity gain when override source is true
01 = Op amp output is tri-stated when override source is true
00 = Output override function is disabled

30.1.2.2 Rising Ramp

The Rising Ramp mode is identical to the Slope Compensation mode, except that the ramps have a rising slope instead of a falling slope. One side of the internal capacitor is connected to the voltage input source and the other side is connected to the internal current source. The internal current source charges this capacitor at a programmable rate. As the capacitor charges, the capacitor voltage is added to the voltage source, producing a linear voltage rise at the required rate (see Figure 30-5). The ramp terminates and the capacitor is discharged when the set_falling timing input goes true. The next ramp starts when the set_rising timing input goes true.

Enabling the optional one-shot by setting the OS bit of the PRGxCON0 register ensures that the capacitor is fully discharged by overriding the set_rising timing input and holding the shorting switch closed for at least the one-shot period, typically 50 ns. Edge-sensitive timing inputs that occur during the one-shot period will be ignored. Level-sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

30.2 Enable, Ready, Go

The EN bit of the PRGxCON0 register enables the analog circuitry including the current sources. This permits preparing the PRG module for use and allowing it to become stable before putting it into operation. When the EN bit is set, then the timing inputs are enabled so that initial ramp action can be determined before the GO bit is set. The capacitor shorting switch is closed when the EN bit is set and remains closed while the GO bit is zero.

The RDY bit of the PRGxCON1 register indicates that the analog circuits and current sources are stable.

The GO bit of the PRGxCON0 register enables the switch control circuits, thereby putting the PRG into operation. The GO transition, from cleared to set, triggers the one-shot, thereby extending the capacitor shorting switch closure for the one-shot period.

To ensure predictable operation, set the EN bit first, then wait for the RDY bit to go high before setting the GO bit.

30.3 Independent Set_rising and Set_falling Timing Inputs

The timing inputs determine when the ramp starts and stops. In the Alternating Rising/Falling mode, the ramp rises when the set_rising input goes true and falls when the set_falling input goes true. In the Slope Compensation and Rising Ramp modes, the capacitor is discharged when the set_falling timing input goes true and the ramp starts when the set_rising timing input goes true. The set_falling input dominates the set_rising input.

30.4 Level and Edge Timing Sensitivity

The set_rising and set_falling timing inputs can be independently configured as either level or edge-sensitive.

Level-sensitive operation is useful when it is necessary to detect a timing input true state after an overriding condition ceases. For example, level sensitivity is useful for capacitor generated timing inputs that may be suppressed by the overriding action of the one-shot. With level sensitivity, a capacitor output that changes during the one-shot period will be detected at the end of the one-shot time. With edge sensitivity, the change would be ignored.

Edge-sensitive operation is useful for periodic timing inputs, such as those generated by PWMs and clocks. The duty cycle of a level-sensitive periodic signal may interfere with the other timing input. Consider an Alternating Ramp mode with a level-sensitive 50% PWM as the set_rising timing source and a level-sensitive comparator as the set_falling timing source. If the comparator output reverses the ramp while the PWM signal is still high, then the ramp will improperly reverse again when the comparator signal goes low. That same scenario with the set_rising timing input set for edge sensitivity would properly change the ramp output to rising only on the rising edge of the PWM signal.

set_rising and set_falling timing input edge sensitivity is selected with the respective REDG and FEDG bits of the PRGxCON1 register.

30.5 One-Shot Minimum Timing

The one-shot timer ensures a minimum capacitor discharge time in the Slope Compensation and Rising Ramp modes, and a minimum rising or falling ramp duration in the Alternating Ramp mode. Setting the OS bit of the PRGxCON0 register enables the one-shot timer.

30.6 DAC Voltage Sources

When using any of the DACs as the voltage source, expect a voltage offset equal to the current setting times the DAC equivalent resistance. This will be a constant offset in the Slope Compensation and Ramp modes, and a positive/negative step offset in the Alternating mode. To avoid this limitation, feed the DAC output to the PRG input through one of the op amps set for unity gain.

30.7 Operation During Sleep

The PRG module is unaffected by Sleep.

30.8 Effects of a Reset

The PRG module resets to a disabled condition.

32.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

TABLE 32-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELC	ANSC<7:6>(2)		—	—	ANSC<3:0>				148
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	102
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	105
RxyPPS	—	—	—	RxyPPS<4:0>					154
SSPCLKPPS	—	—	—	SSPCLKPPS<4:0>					154, 156
SSPDATPPS	—	—	—	SSPDATPPS<4:0>					154, 156
SSPSSPPS	—	—	—	SSPSSPPS<4:0>					154, 156
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								380*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				426
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	424
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	424
TRISA	—	—	TRISA<5:4>		—(1)	TRISA<2:0>			136
TRISB(2)	TRISB<7:4>				—	—	—	—	142
TRISC	TRISC<7:6>(2)		TRISC<5:0>						147

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

* Page provides register information.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1768/9 only.

32.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN, of the SSPxCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 32-30).

32.6.8.1 WCOL Status Flag

If the user writes the SSPxBUF when an Acknowledge sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

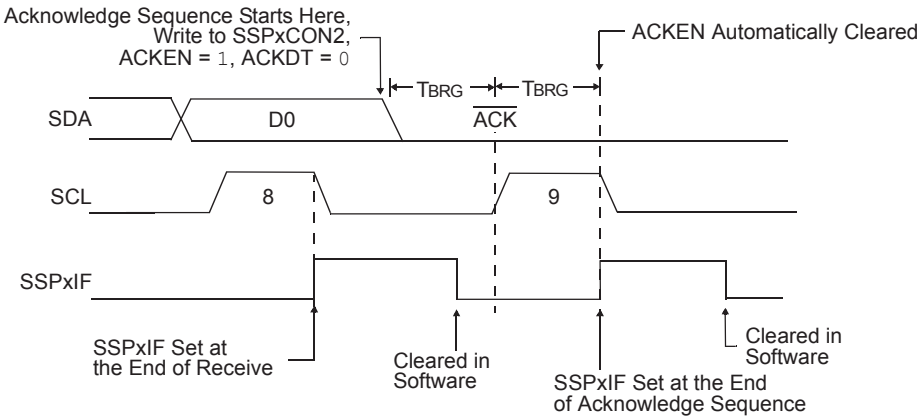
32.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN, of the SSPxCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPxSTAT register is set. A TBRG later, the PEN bit is cleared and the SSPxIF bit is set (Figure 32-31).

32.6.9.1 WCOL Status Flag

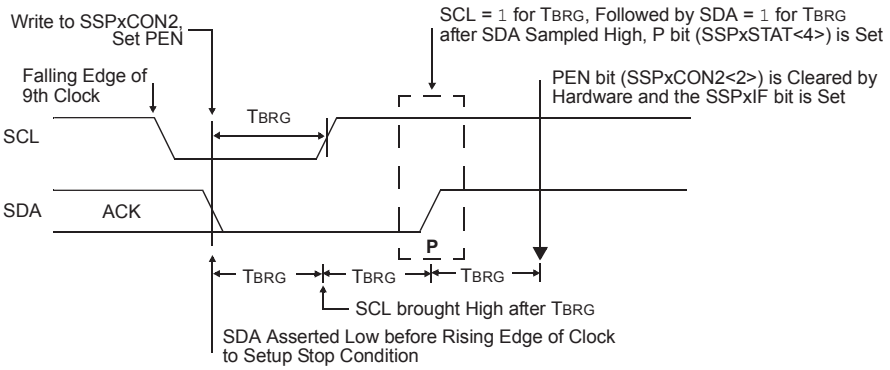
If the user writes the SSPxBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 32-30: ACKNOWLEDGE SEQUENCE WAVEFORM



Note: TBRG = one Baud Rate Generator period.

FIGURE 32-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



Note: TBRG = one Baud Rate Generator period.

REGISTER 33-2: RC1STA: RECEIVE STATUS AND CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-0/0
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **SPEN:** Serial Port Enable bit
1 = Serial port is enabled
0 = Serial port is disabled (held in Reset)

bit 6 **RX9:** 9-Bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5 **SREN:** Single Receive Enable bit
Asynchronous mode:
Don’t care.
Synchronous mode – Master:
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.
Synchronous mode – Slave:
Don’t care.

bit 4 **CREN:** Continuous Receive Enable bit
Asynchronous mode:
1 = Enables receiver
0 = Disables receiver
Synchronous mode:
1 = Enables continuous receive until enable bit, CREN, is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3 **ADDEN:** Address Detect Enable bit
Asynchronous mode, 9-bit (RX9 = 1):
1 = Enables address detection, enables interrupt and loads the receive buffer when RSR<8> is set
0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
Asynchronous mode, 8-bit (RX9 = 0):
Don’t care.

bit 2 **FERR:** Framing Error bit
1 = Framing error (can be updated by reading RCxREG register and receiving next valid byte)
0 = No framing error

bit 1 **OERR:** Overrun Error bit
1 = Overrun error (can be cleared by clearing bit, CREN)
0 = No overrun error

bit 0 **RX9D:** Ninth bit of Received Data
This can be address/data bit or a parity bit and must be calculated by user firmware.

34.0 IN-CIRCUIT SERIAL PROGRAMMING™ (ICSP™)

ICSP™ programming allows customers to manufacture circuit boards with unprogrammed devices. Programming can be done after the assembly process, allowing the device to be programmed with the most recent firmware or a custom firmware. Five pins are needed for ICSP™ programming:

- ICSPCLK
- ICSPDAT
- $\overline{MCLR}/V_{PP}$
- V_{DD}
- V_{SS}

In Program/Verify mode, the program memory, User IDs and the Configuration Words are programmed through serial communications. The ICSPDAT pin is a bidirectional I/O used for transferring the serial data and the ICSPCLK pin is the clock input. For more information on ICSP™ refer to the *"PIC16(L)F170X Memory Programming Specification"* (DS40001683).

34.1 High-Voltage Programming Entry Mode

The device is placed into High-Voltage Programming Entry mode by holding the ICSPCLK and ICSPDAT pins low, then raising the voltage on $\overline{MCLR}/V_{PP}$ to V_{IHH}.

34.2 Low-Voltage Programming Entry Mode

The Low-Voltage Programming Entry mode allows the PIC® Flash MCUs to be programmed using V_{DD} only, without high voltage. When the LVP bit of Configuration Words is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'.

Entry into the Low-Voltage Programming Entry mode requires the following steps:

1. $\overline{MCLR}$ is brought to V_{IL}.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

Once the key sequence is complete, $\overline{MCLR}$ must be held at V_{IL} for as long as Program/Verify mode is to be maintained.

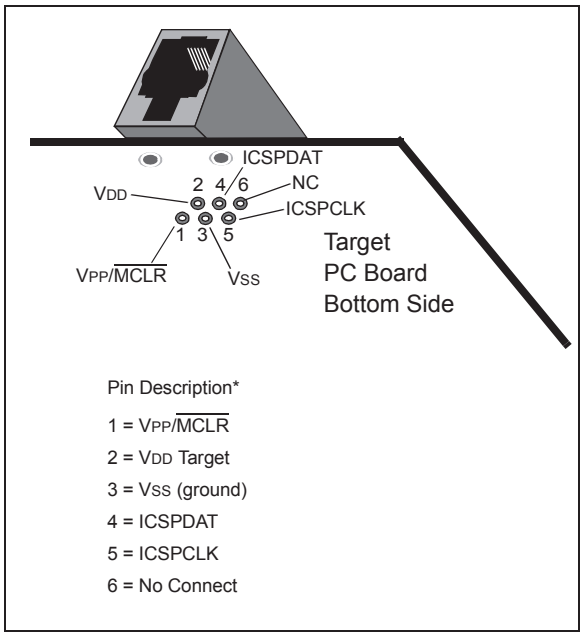
If Low-Voltage Programming mode is enabled (LVP = 1), the $\overline{MCLR}$ Reset function is automatically enabled and cannot be disabled. See **Section 6.5 "MCLR"** for more information.

The LVP bit can only be reprogrammed to '0' by using the High-Voltage Programming mode.

34.3 Common Programming Interfaces

Connection to a target device is typically done through an ICSP header. A commonly found connector on development tools is the RJ-11 in the 6P6C (6-pin, 6-connector) configuration. See Figure 34-1.

FIGURE 34-1: ICD RJ-11 STYLE CONNECTOR INTERFACE



Another connector often found in use with the PICkit™ programmers is a standard 6-pin header with 0.1 inch spacing. Refer to Figure 34-2.

For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices, such as resistors, diodes or even jumpers. See Figure 34-3 for more information.

RRF **Rotate Right f through Carry**

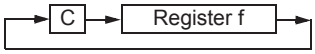
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP **Enter Sleep mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The Power-Down Status bit, $\overline{PD}$, is cleared. Time-out Status bit, $\overline{TO}$, is set. Watchdog Timer and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.

SUBLW **Subtract W from literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) - (W) → (destination)

Status Affected: C, DC, Z

Description: Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.

C = 0	W > f
C = 1	W ≤ f
DC = 0	W<3:0> > f<3:0>
DC = 1	W<3:0> ≤ f<3:0>

SUBWFB **Subtract W from f with Borrow**

Syntax: SUBWFB f {,d}

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) – (W) – ($\overline{B}$) → dest

Status Affected: C, DC, Z

Description: Subtract W and the Borrow flag (Carry) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

36.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} – Operating Supply Voltage(1)

PIC16LF1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +1.8V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +3.6V

PIC16F1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +2.3V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +5.5V

T_A – Operating Ambient Temperature Range

Industrial Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +85°C

Extended Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

TABLE 36-25: SPI MODE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
SP70*	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ Input	Tcy	—	—	ns	
SP71*	TscH	SCK Input High Time (Slave mode)	Tcy + 20	—	—	ns	
SP72*	TscL	SCK Input Low Time (Slave mode)	Tcy + 20	—	—	ns	
SP73*	TdiV2scH, TdiV2scL	Setup Time of SDI Data Input to SCK Edge	100	—	—	ns	
SP74*	TscH2diL, TscL2diL	Hold Time of SDI Data Input to SCK Edge	100	—	—	ns	
SP75*	TdoR	SDO Data Output Rise Time	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP76*	TdoF	SDO Data Output Fall Time	—	10	25	ns	
SP77*	TssH2doZ	$\overline{SS}$↑ to SDO Output High-Impedance	10	—	50	ns	
SP78*	TscR	SCK Output Rise Time (Master mode)	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP79*	TscF	SCK Output Fall Time (Master mode)	—	10	25	ns	
SP80*	TscH2doV, TscL2doV	SDO Data Output Valid after SCK Edge	—	—	50	ns	3.0V ≤ VDD ≤ 5.5V
			—	—	145	ns	1.8V ≤ VDD ≤ 5.5V
SP81*	TdoV2scH, TdoV2scL	SDO Data Output Setup to SCK Edge	1 Tcy	—	—	ns	
SP82*	TssL2doV	SDO Data Output Valid after $\overline{SS}$↓ Edge	—	—	50	ns	
SP83*	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK Edge	1.5 Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

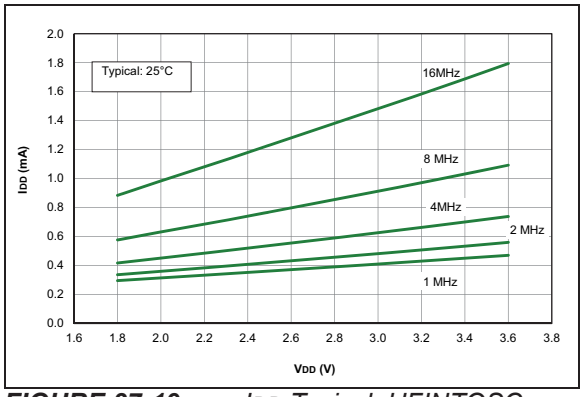


FIGURE 37-19: *IDD Typical, HFINTOSC Mode, PIC16LF1764/5/8/9 Only.*

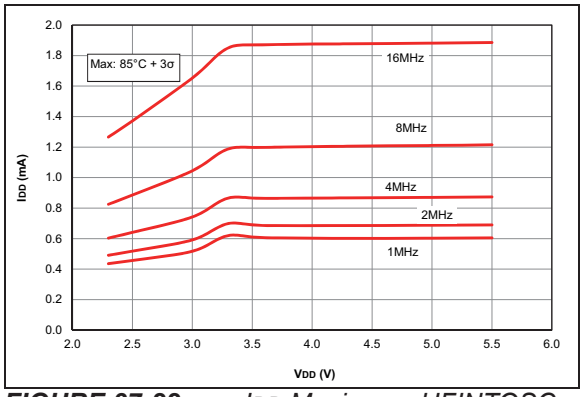


FIGURE 37-22: *IDD Maximum, HFINTOSC Mode, PIC16F1764/5/8/9 Only.*

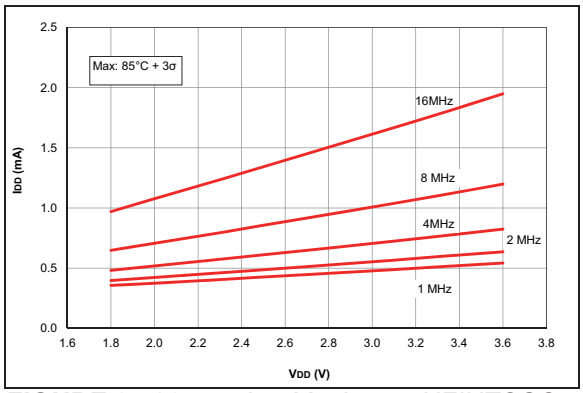


FIGURE 37-20: *IDD Maximum, HFINTOSC Mode, PIC16LF1764/5/8/9 Only.*

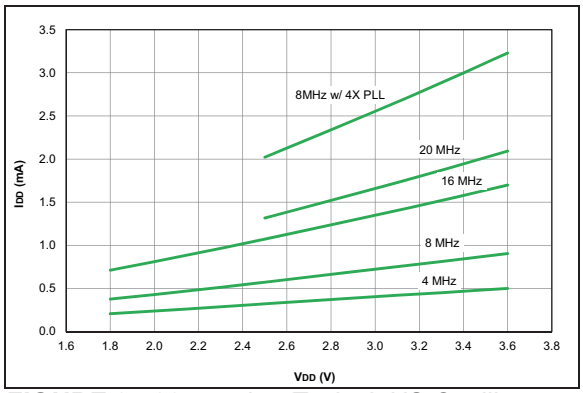


FIGURE 37-23: *IDD Typical, HS Oscillator, 25°C, PIC16LF1764/5/8/9 Only.*

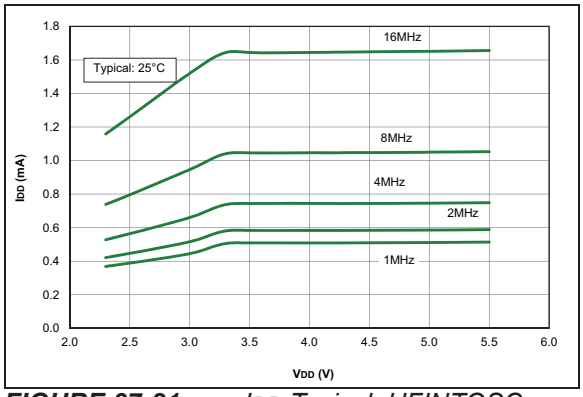


FIGURE 37-21: *IDD Typical, HFINTOSC Mode, PIC16F1764/5/8/9 Only.*

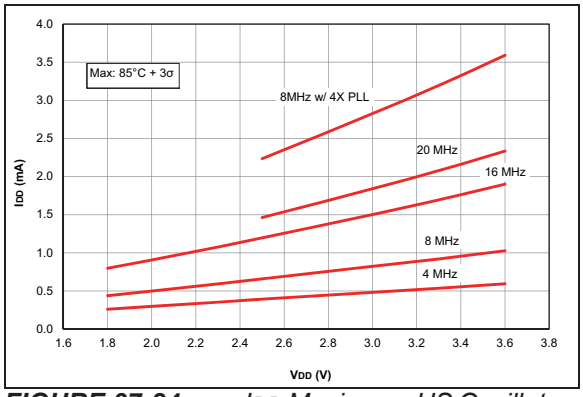
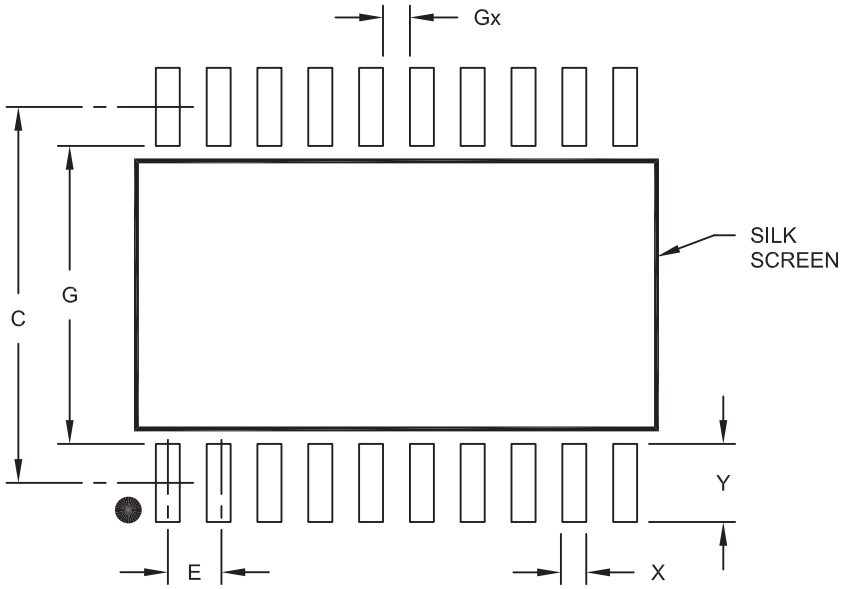


FIGURE 37-24: *IDD Maximum, HS Oscillator, PIC16LF1764/5/8/9 Only.*

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width (X20)	X			0.60
Contact Pad Length (X20)	Y			1.95
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2094A