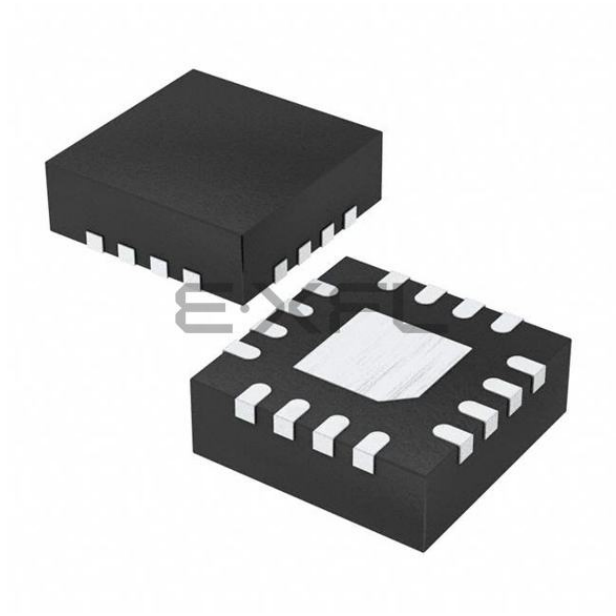

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 1x5b, 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1764-i-ml

TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 2											
10Ch	LATA	—	—	LATA<5:4>		—	LATA<2:0>			--xx -xxx	--uu -uuu
10Dh	LATB(2)	LATB<7:4>				—	—	—	—	xxxx ----	uuuu ----
10Eh	LATC	LATC<7:6>(2)		LATC<5:0>						xxxx xxxx	uuuu uuuu
10Fh	CMOUT	—	—	—	—	MC4OUT(2)	MC3OUT(2)	MC2OUT	MC1OUT	---- 0000	---- 0000
110h	CM1CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	00-0 0100	00-0 0100
111h	CM1CON1	—	—	—	—	—	—	INTP	INTN	---- --00	---- --00
112h	CM1NSEL	—	—	—	—	—	NCH<2:0>			---- -000	---- -000
113h	CM1PSEL	—	—	—	—	—	PCH<2:0>			---- -000	---- -000
114h	CM2CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	00-0 0100	00-0 0100
115h	CM2CON1	—	—	—	—	—	—	INTP	INTN	---- --00	---- --00
116h	CM2NSEL	—	—	—	—	—	NCH<2:0>			---- -000	---- -000
117h	CM2PSEL	—	—	—	—	—	PCH<2:0>			---- -000	---- -000
118h	CM3CON0(2)	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	00-0 0100	00-0 0100
119h	CM3CON1(2)	—	—	—	—	—	—	INTP	INTN	---- --00	---- --00
11Ah	CM3NSEL(2)	—	—	—	—	—	NCH<2:0>			---- -000	---- -000
11Bh	CM3PSEL(2)	—	—	—	—	—	PCH<2:0>			---- -000	---- -000
11Ch	CM4CON0(2)	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	00-0 0100	00-0 0100
11Dh	CM4CON1(2)	—	—	—	—	—	—	INTP	INTN	---- --00	---- --00
11Eh	CM4NSEL(2)	—	—	—	—	—	NCH<2:0>			---- -000	---- -000
11Fh	CM4PSEL(2)	—	—	—	—	—	PCH<2:0>			---- -000	---- -000
Bank 3											
18Ch	ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			---1 -111	---1 -111
18Dh	ANSELB(2)	ANSB<7:4>				—	—	—	—	1111 ----	1111 ----
18Eh	ANSELC	ANSC<7:6>(2)		—	—	ANSC<3:0>				11-- 1111	11-- 1111
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	PMADRL	Program Memory Address Register Low Byte								0000 0000	0000 0000
192h	PMADRH	—(1)	Program Memory Address Register High Byte							1000 0000	1000 0000
193h	PMDATL	Program Memory Read Data Register Low Byte								xxxx xxxx	uuuu uuuu
194h	PMDATH	—	—	Program Memory Read Data Register High Byte						--xx xxxx	--uu uuuu
195h	PMCON1	—(1)	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	1000 x000	1000 q000
196h	PMCON2	Program Memory Control Register 2								0000 0000	0000 0000
197h	VREGCON(4)	—	—	—	—	—	—	VREGPM	Reserved	---- --01	---- --01
198h	—	Unimplemented								—	—
199h	RC1REG	EUSART Receive Data Register								0000 0000	0000 0000
19Ah	TX1REG	EUSART Transmit Data Register								0000 0000	0000 0000
19Bh	SP1BRGL	SP1BRG<7:0>								0000 0000	0000 0000
19Ch	SP1BRGH	SP1BRG<15:8>								0000 0000	0000 0000
19Dh	RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0000	0000 0000
19Eh	TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
19Fh	BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1768/9 only.

3: PIC16(L)F1764/5 only.

4: Unimplemented on PIC16LF1764/5/8/9.

REGISTER 4-2: CONFIG2: CONFIGURATION WORD 2 (CONTINUED)

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits

4 kW Flash Memory (PIC16(L)F1764/8):

11 = Off Write protection is off
10 = Boot 0000h to 01FFh are write-protected, 0200h to 0FFFh may be modified by PMCON control
01 = Half 0000h to 07FFh are write-protected, 0800h to 0FFFh may be modified by PMCON control
00 = All 0000h to 0FFFh are write-protected, no addresses may be modified by PMCON control

8 kW Flash Memory (PIC16(L)F1765/9):

11 = Off Write protection is off
10 = Boot 0000h to 01FFh are write-protected, 0200h to 1FFFh may be modified by PMCON control
01 = Half 0000h to 0FFFh are write-protected, 1000h to 1FFFh may be modified by PMCON control
00 = All 0000h to 1FFFh are write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

2: The $\overline{\text{DEBUG}}$ bit in the Configuration Words is managed automatically by device development tools, including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.

3: See V_{BOR} parameter for specific trip point voltages.

7.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate interrupt enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to **Section 8.0 "Power-Down Mode (Sleep)"** for more details.

7.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

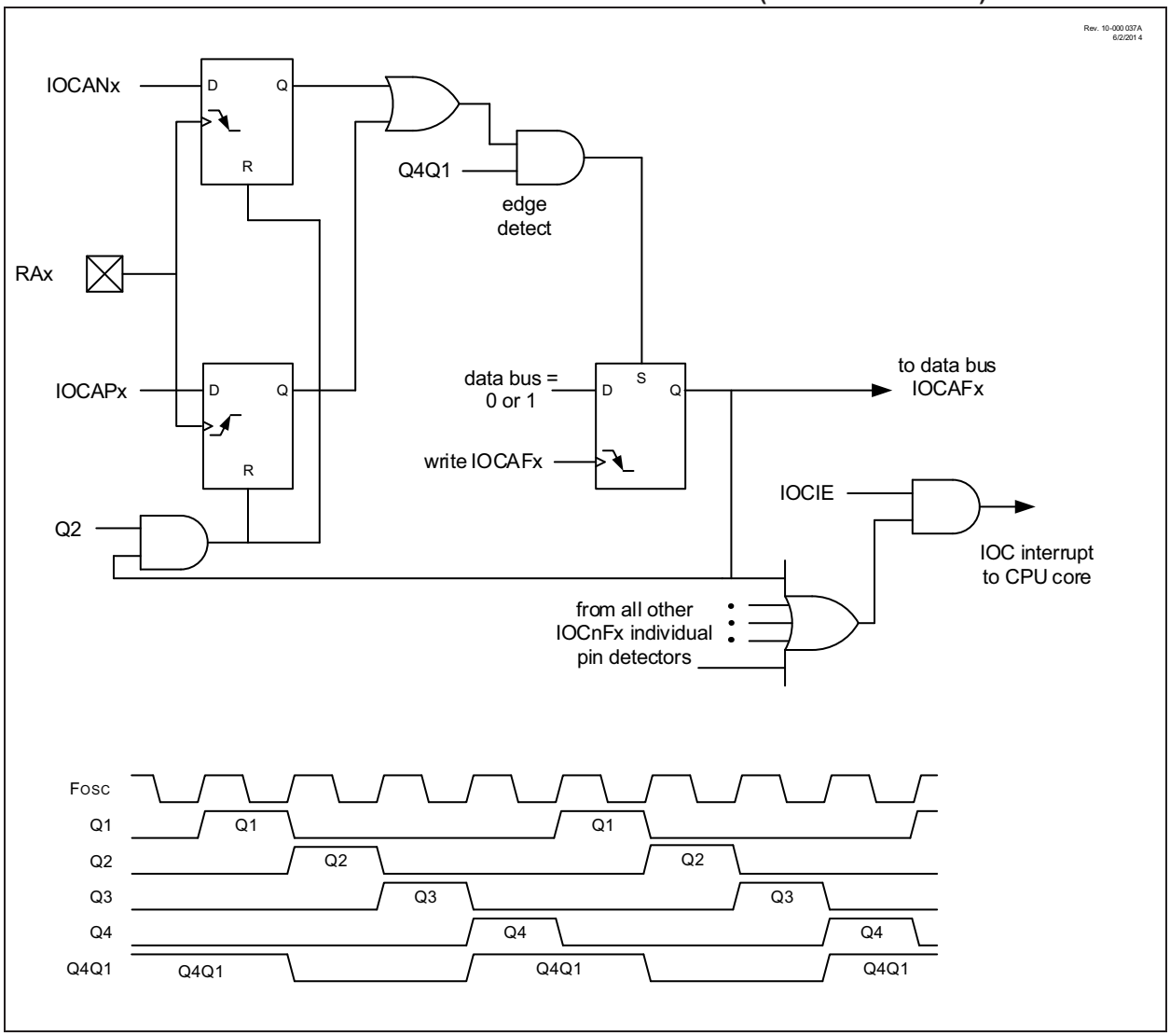
7.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for $\overline{TO}$ and $\overline{PD}$)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

FIGURE 13-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM (PORTA EXAMPLE)



16.2.6 ADC CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure the PORT:
   - Disable the pin output driver (refer to the TRISx register)
   - Configure pin as an analog (refer to the ANSELx register)
   - Disable weak pull-ups either globally (Refer to the OPTION_REG register) or individually (Refer to the appropriate WPUx register)
2. Configure the ADC module:
   - Select ADC conversion clock
   - Configure voltage reference
   - Select ADC input channel
   - Turn on ADC module
3. Configure ADC interrupt (optional):
   - Clear ADC interrupt flag
   - Enable ADC interrupt
   - Enable peripheral interrupt
   - Enable global interrupt(1)
4. Wait the required acquisition time.(2)
5. Start conversion by setting the GO/$\overline{\text{DONE}}$ bit.
6. Wait for ADC conversion to complete by one of the following:
   - Polling the GO/$\overline{\text{DONE}}$ bit
   - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to **Section 16.4 "ADC Acquisition Requirements"**.

EXAMPLE 16-1: ADC CONVERSION

```
;This code block configures the ADC
;for polling, Vdd and Vss references, FRC
;oscillator and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL   ADCON1       ;
MOVLW     B'11110000'  ;Right justify, FRC
                       ;oscillator
MOVWF     ADCON1       ;Vdd and Vss Vref
BANKSEL   TRISA        ;
BSF       TRISA,0      ;Set RA0 to input
BANKSEL   ANSEL        ;
BSF       ANSEL,0      ;Set RA0 to analog
BANKSEL   WPUA
BCF       WPUA,0       ;Disable weak
                       ;pull-up on RA0
BANKSEL   ADCON0       ;
MOVLW     B'00000001'  ;Select channel AN0
MOVWF     ADCON0       ;Turn ADC On
CALL      SampleTime   ;Acquisiton delay
BSF       ADCON0,ADGO  ;Start conversion
BTFSC     ADCON0,ADGO  ;Is conversion done?
GOTO      $-1          ;No, test again
BANKSEL   ADRESH       ;
MOVF      ADRESH,W     ;Read upper 2 bits
MOVWF     RESULTHI     ;store in GPR space
BANKSEL   ADRESL       ;
MOVF      ADRESL,W     ;Read lower 8 bits
MOVWF     RESULTLO     ;Store in GPR space
```

16.4 ADC Acquisition Requirements

For the ADC to meet its specified accuracy, the Charge Holding Capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 16-4. The Source Impedance (RS) and the internal Sampling Switch (RSS) impedance directly affect the time required to charge the capacitor, CHOLD. The Sampling Switch (RSS) impedance varies over the device voltage (VDD), refer to Figure 16-4. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an ADC acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 16-1 may be used. This equation assumes that 1/2 LSb error is used (1,024 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

EQUATION 16-1: ACQUISITION TIME EXAMPLE

Assumptions: *Temperature = 50°C and external impedance of 10kΩ 5.0V VDD*

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \\ &= 2\mu s + T_C + [(\text{Temperature} - 25°C)(0.05\mu s/°C)] \end{aligned}$$

The value for TC can be approximated with the following equations:

$$V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) = V_{CHOLD} \quad ;[1]\ V_{CHOLD}\ \text{charged to within 1/2 lsb}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{CHOLD} \quad ;[2]\ V_{CHOLD}\ \text{charge response to}\ V_{APPLIED}$$

$$V_{APPLIED}\left(1 - e^{\frac{-T_C}{RC}}\right) = V_{APPLIED}\left(1 - \frac{1}{(2^{n+1}) - 1}\right) \quad ;\text{combining [1] and [2]}$$

Note: Where n = number of bits of the ADC.

Solving for TC:

$$\begin{aligned} T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S)\ ln(1/2047) \\ &= -10pF(1k\Omega + 7k\Omega + 10k\Omega)\ ln(0.0004885) \\ &= 1.37\mu s \end{aligned}$$

Therefore:

$$\begin{aligned} T_{ACQ} &= 2\mu s + 892ns + [(50°C - 25°C)(0.05\mu s/°C)] \\ &= 4.62\mu s \end{aligned}$$

Note 1: The Reference Voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The Charge Holding Capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

19.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the HYS bit of the CMxCON0 register.

See Comparator Specifications in Table 36-19: Comparator Specifications for more information.

19.4 Timer1 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1. See **Section 22.6 "Timer1 Gate"** for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

19.4.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the SYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 19-2) and the Timer1 Block Diagram (Figure 22-1) for more information.

19.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator, a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (INTP and/or INTN bits of the CMxCON1 register), the corresponding interrupt flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, you must set the following bits:

- ON and POL bits of the CMxCON0 register
- CxIE bit of the PIE2 register
- INTP bit of the CMxCON1 register (for a rising edge detection)
- INTN bit of the CMxCON1 register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

Note:	Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the POL bit of the CMxCON0 register, or by switching the comparator on or off with the ON bit of the CMxCON0 register.

19.6 Comparator Positive Input Selection

Configuring the PCH<3:0> bits of the CMxPSEL register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN+ analog pin
- Programmable Ramp Generator (PRG) output
- DAC output
- FVR (Fixed Voltage Reference)
- VSS (Ground)

See **Section 14.0 "Fixed Voltage Reference (FVR)"** for more information on the Fixed Voltage Reference module.

See **Section 17.0 "5-Bit Digital-to-Analog Converter (DAC) Module"** for more information on the DAC input signal.

Any time the comparator is disabled (CxON = 0), all comparator inputs are disabled.

19.7 Comparator Negative Input Selection

The NCH<2:0> bits of the CMxNSEL register direct an analog input pin and internal reference voltage or analog ground to the inverting input of the comparator:

- CxIN- pin
- FVR (Fixed Voltage Reference)
- Analog ground

Some inverting input selections share a pin with the operational amplifier output function. Enabling both functions at the same time will direct the operational amplifier output to the comparator inverting input.

Note:	To use CxINy+ and CxINy- pins as analog inputs, the appropriate bits must be set in the ANSELx register and the corresponding TRISx bits must also be set to disable the output drivers.

REGISTER 19-2: CMxCON1: COMPARATOR Cx CONTROL REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	—	—	—	—	INTP	INTN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-2 **Unimplemented:** Read as ‘0’

bit 1 **INTP:** Comparator Interrupt on Positive Going Edge Enable bit
1 = The CxIF interrupt flag will be set upon a positive going edge of the CxOUT bit
0 = No interrupt flag will be set on a positive going edge of the CxOUT bit

bit 0 **INTN:** Comparator Interrupt on Negative Going Edge Enable bit
1 = The CxIF interrupt flag will be set upon a negative going edge of the CxOUT bit
0 = No interrupt flag will be set on a negative going edge of the CxOUT bit

REGISTER 19-3: CMxNSEL: COMPARATOR Cx NEGATIVE CHANNEL SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	NCH<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-3 **Unimplemented:** Read as ‘0’

bit 2-0 **NCH<2:0>:** Comparator Negative Input Channel Select bits
111 = CxVN connects to AGND
110 = CxVN connects to FVR Buffer2
101 = CxVN connects to PRG2_output(1)
100 = CxVN connects to PRG1_output
011 = CxVN connects to CxIN3- pin
010 = CxVN connects to CxIN2- pin
001 = CxVN connects to CxIN1- pin
000 = CxVN connects to CxIN0- pin

Note 1: PIC16(L)F1768/9 only.

23.5 Timer2 Interrupt

Timer2 can also generate a device interrupt. The interrupt is generated when the postscaler counter matches one of 16 postscale options (from 1:1 through 1:16), which are selected with the postscaler control bits, OUTPS<3:0> of the T2CON register. The interrupt is enabled by setting the TMR2IE interrupt enable bit of the PIE1 register. Interrupt timing is illustrated in Figure 23-3.

FIGURE 23-3: TIMER2 PRESCALER, POSTSCALER AND INTERRUPT TIMING DIAGRAM

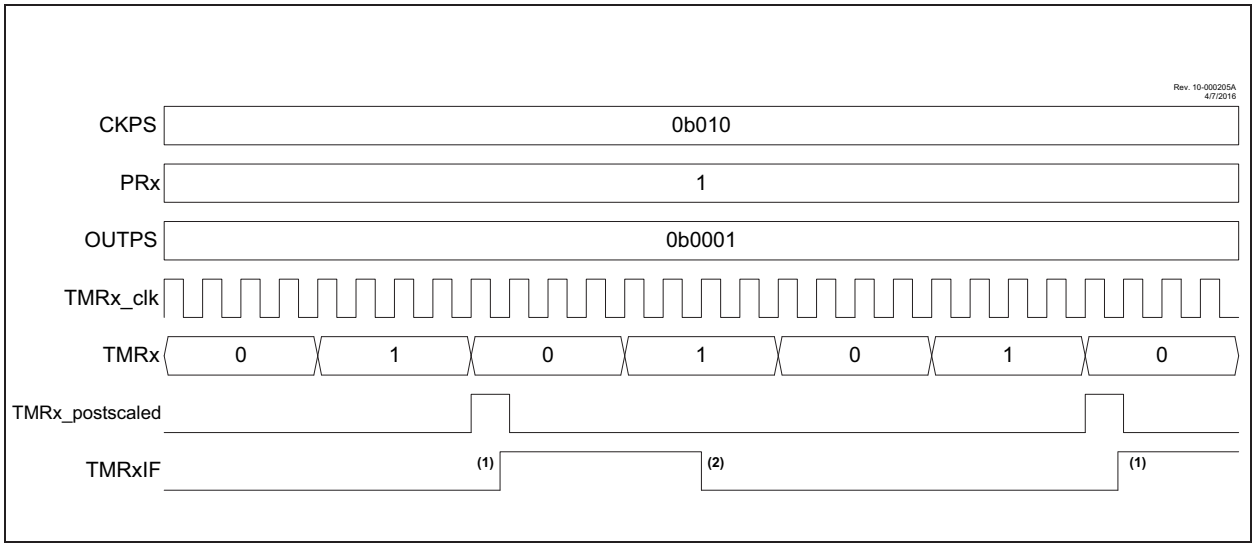


FIGURE 26-9: SLAVE RUN MODE WITH SYNC START TIMING DIAGRAM

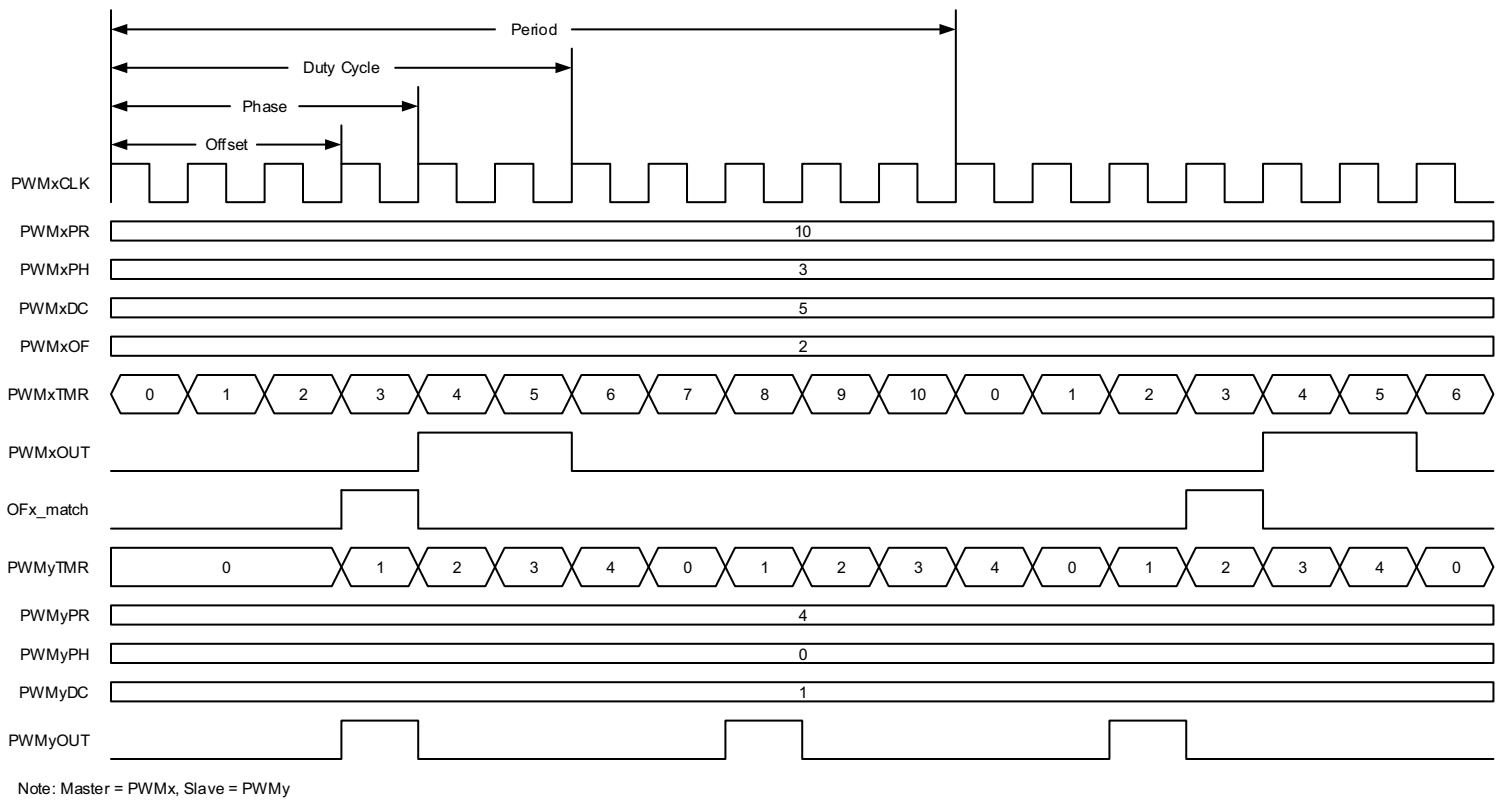
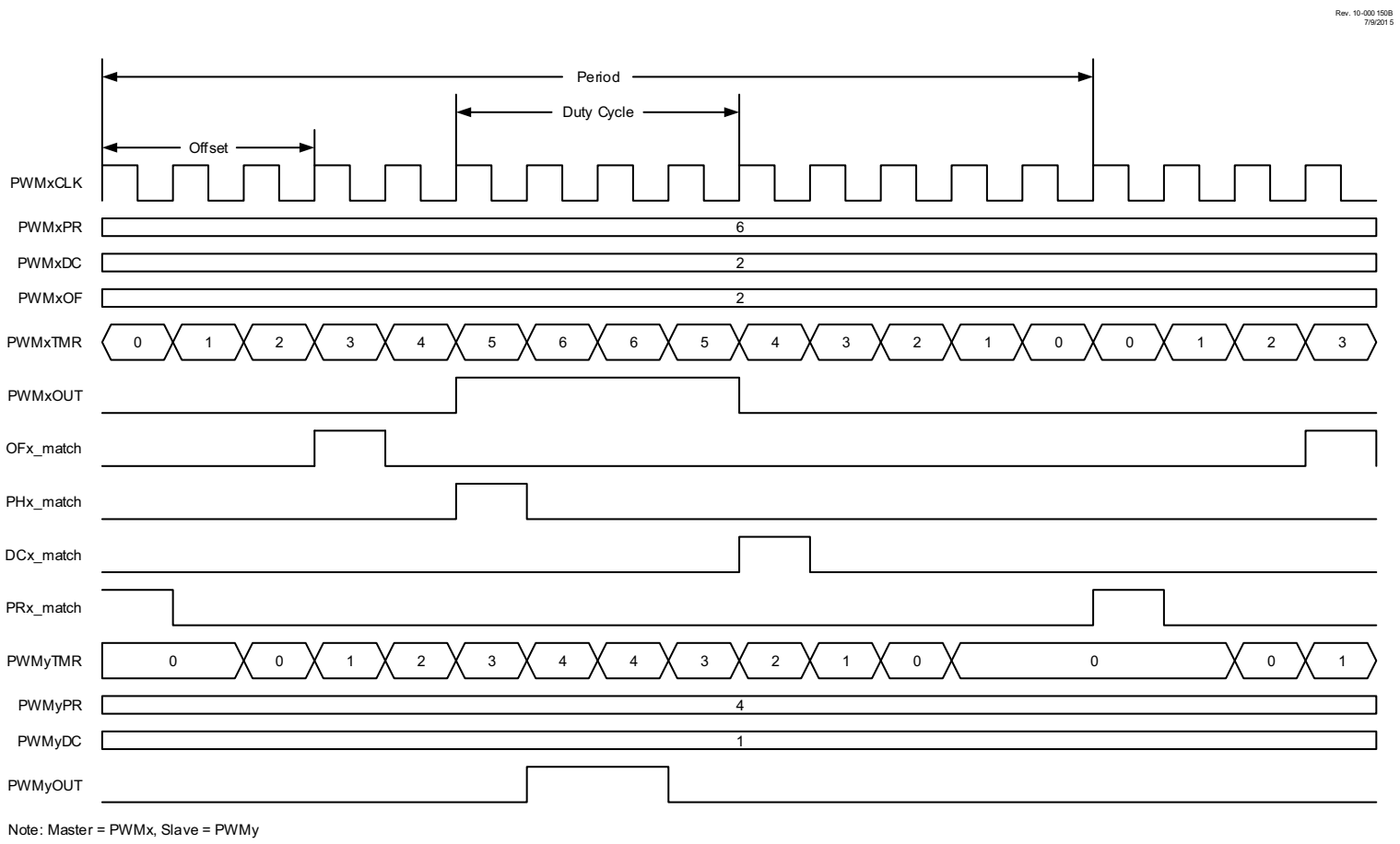


FIGURE 26-12: OFFSET MATCH ON INCREMENTING TIMER TIMING DIAGRAM



REGISTER 26-2: PWMxINTE: PWMx INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	OFIE	PHIE	DCIE	PRIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OFIE**: Offset Interrupt Enable bit
1 = Interrupts CPU on offset match
0 = Does not interrupt CPU on offset match

bit 2 **PHIE:** Phase Interrupt Enable bit
1 = Interrupts CPU on phase match
0 = Does not interrupt CPU on phase match

bit 1 **DCIE:** Duty Cycle Interrupt Enable bit
1 = Interrupts CPU on duty cycle match
0 = Does not interrupt CPU on duty cycle match

bit 0 **PRIE:** Period Interrupt Enable bit
1 = Interrupts CPU on period match
0 = Does not interrupt CPU on period match

REGISTER 28-3: CLCxSEL0: GENERIC CLCx DATA 1 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	D1S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **D1S<5:0>:** CLCx Data1 Input Selection bits
See Table 28-1.

REGISTER 28-4: CLCxSEL1: GENERIC CLCx DATA 2 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	D2S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **D2S<5:0>:** CLCx Data 2 Input Selection bits
See Table 28-1.

REGISTER 28-5: CLCxSEL2: GENERIC CLCx DATA 3 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	D3S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **D3S<5:0>:** CLCx Data 3 Input Selection bits
See Table 28-1.

29.1 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common-Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open-Loop Gain
- Gain Bandwidth Product

Common-mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between VSS and VDD. Behavior for Common-mode voltages greater than VDD, or below VSS, are not guaranteed.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the Common-mode voltage. The OPA is factory calibrated to minimize the input offset voltage of the module.

Open-loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) – (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open-loop gain falls off to 0 dB.

29.2 OPA Module Control

The OPA module is enabled by setting the OPAxEN bit of the OPAxCON register (Register 29-1). When enabled, the OPA forces the output driver of OPAxOUT pin into tri-state to prevent contention between the driver and the OPA output.

Note:	When the OPA module is enabled, the OPAxOUT pin is driven by the op amp output, not by the PORT digital driver. Refer to Table 36-17: Operational Amplifier (OPA) for the op amp output drive capability.

29.2.1 UNITY GAIN MODE

The OPAxUG bit of the OPAxCON register (Register 29-1) selects the Unity Gain mode. When unity gain is selected, the OPA output is connected to the inverting input and the OPAxIN pin is relinquished, releasing the pin for general purpose input and output.

29.2.2 PROGRAMMABLE SOURCE SELECTIONS

The inverting and non-inverting sources are selected with the OPAxNCHS (Register 29-3) and OPAxPCHS (Register 29-4) registers, respectively. Sources include:

- Internal DACs
- Device pins
- Internal slope compensation ramp generator
- Other op amps in the device

29.3 Override Control

29.3.1 OVERRIDE MODE

The op amp operation can be overridden in two ways:

- Forced tri-state output
- Force unity gain

The Override mode is selected with the ORM<1:0> bits of the OPxCON register (Register 29-1). The override is in effect when the mode is selected and the override source is true.

29.3.2 OVERRIDE SOURCES

The override source is selected with the OPAxORS register (Register 29-2). Sources are from internal peripherals including:

- CCP outputs
- PWM outputs
- Comparator outputs
- Zero-Cross Detect (ZCD) output
- Configurable Logic Cell outputs
- COG outputs

29.3.3 OVERRIDE SOURCE POLARITY

The override source polarity can be inverted so that the override will occur on either the high or low level of the selected source. Override polarity is controlled by the ORPOL bit of the OPAxCON register (Register 29-1).

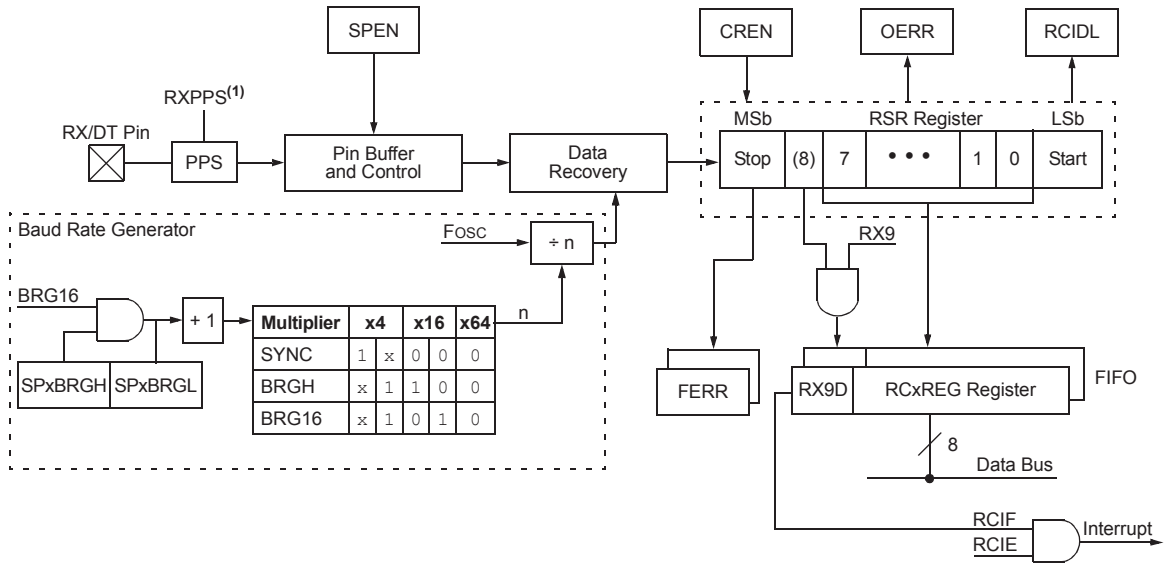
29.4 Effects of Reset

A device Reset forces all registers to their Reset state. This disables the OPA module.

29.5 Effects of Sleep

The operational amplifier continues to operate when the device is put in Sleep mode.

FIGURE 33-2: EUSART RECEIVE BLOCK DIAGRAM



Note 1: In Synchronous mode, the DT output and RX input PPS selections should enable the same pin.

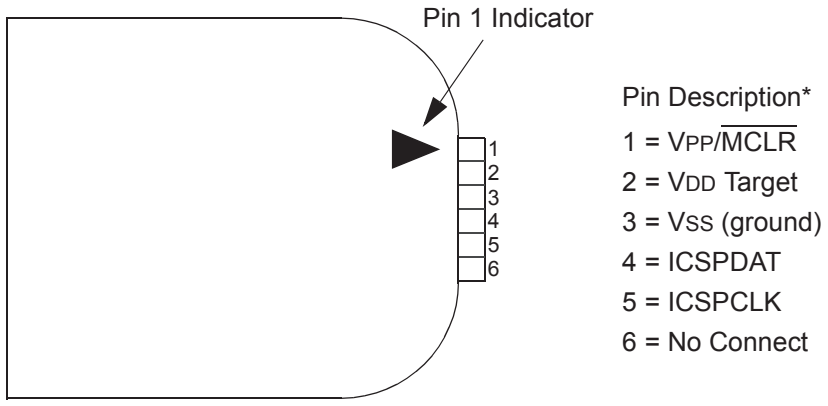
The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXxSTA)
- Receive Status and Control (RCxSTA)
- Baud Rate Control (BAUDxCON)

These registers are detailed in Register 33-1, Register 33-2 and Register 33-3, respectively.

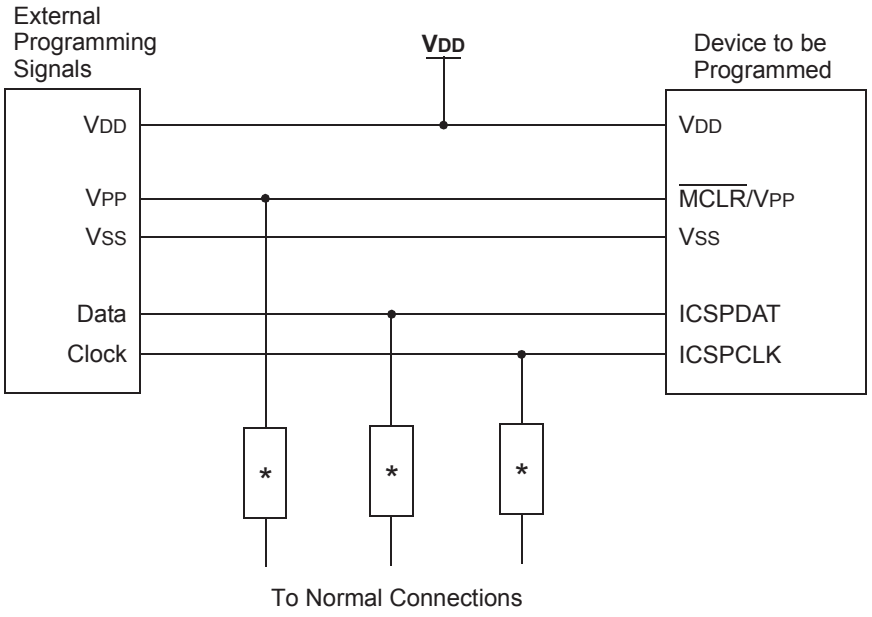
The RX and CK input pins are selected with the RXPPS and CKPPS registers, respectively. TX, CK and DT output pins are selected with each pin's RxyPPS register. Since the RX input is coupled with the DT output in Synchronous mode, it is the user's responsibility to select the same pin for both of these functions when operating in Synchronous mode. The EUSART control logic will control the data direction drivers automatically.

FIGURE 34-2: PICkit™ PROGRAMMER STYLE CONNECTOR INTERFACE



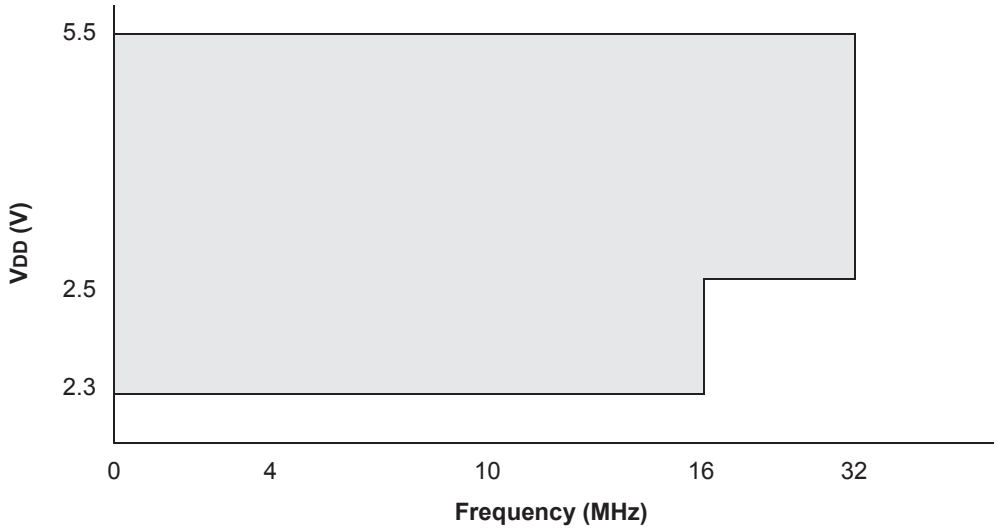
* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

FIGURE 34-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING



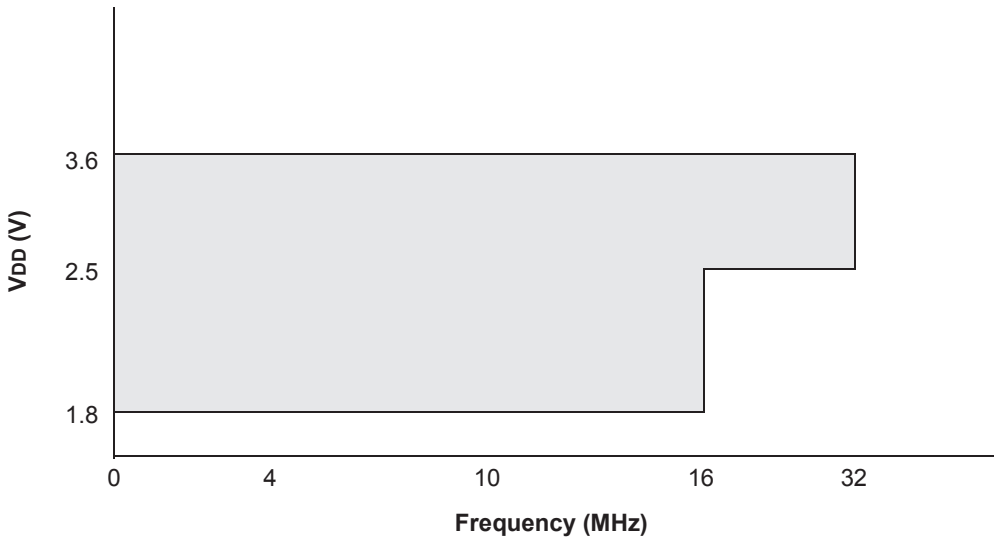
* Isolation devices (as required).

FIGURE 36-1: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16F1764/5/8/9 ONLY



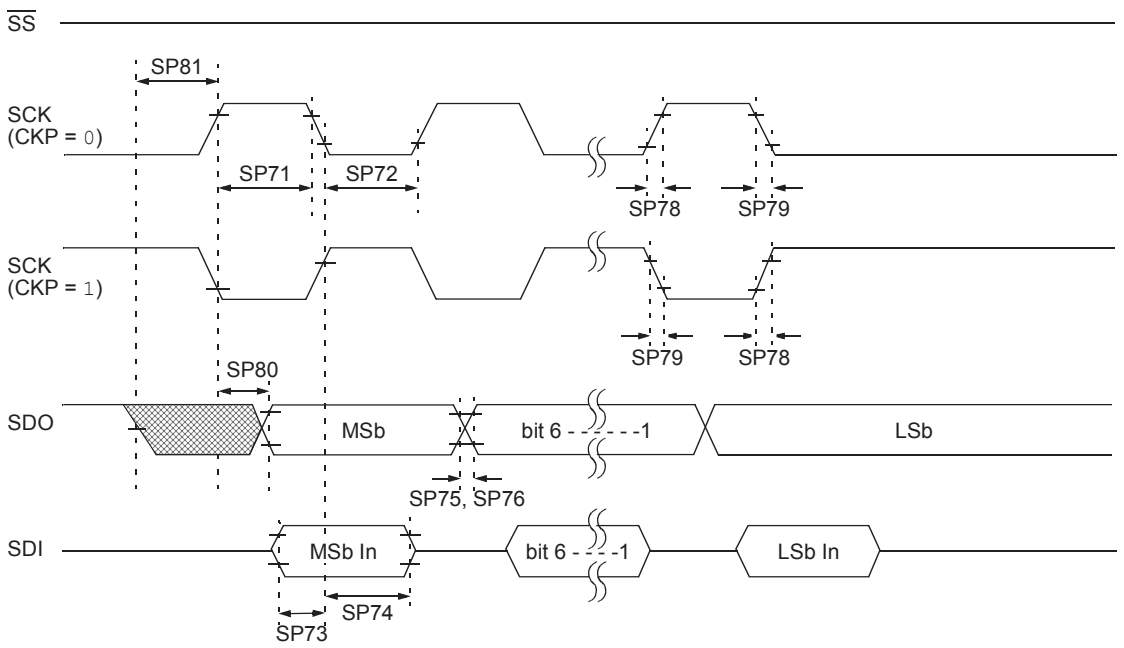
Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 36-7 for each Oscillator mode's supported frequencies.

FIGURE 36-2: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16LF1764/5/8/9 ONLY



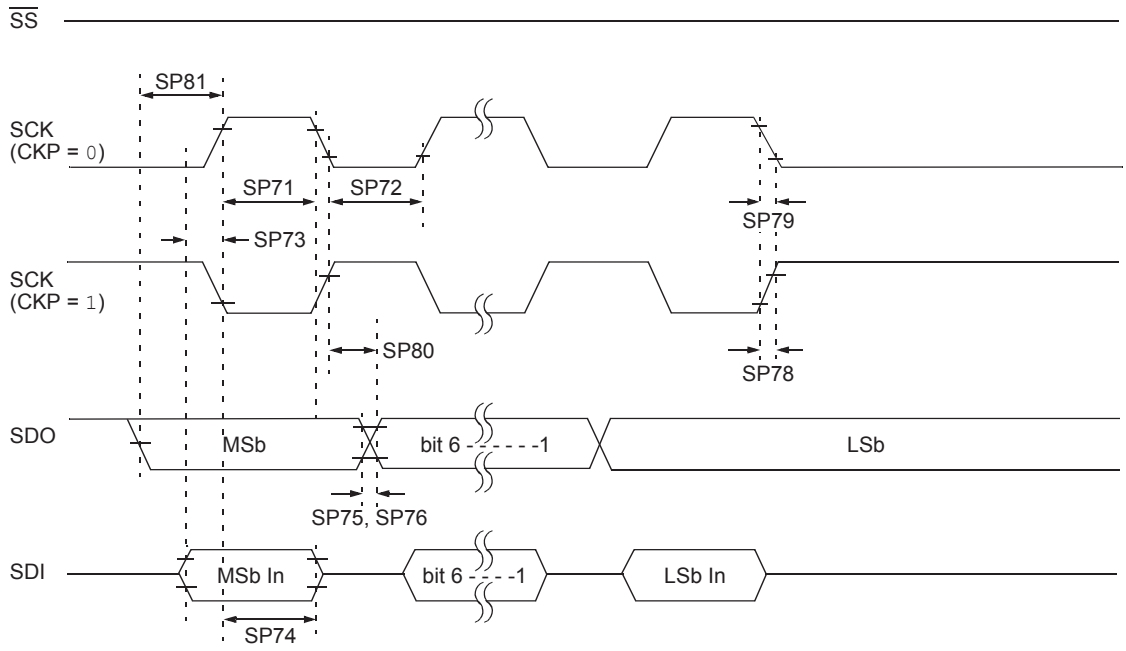
Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 36-7 for each Oscillator mode's supported frequencies.

FIGURE 36-17: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)



Note: Refer to Figure 36-4 for load conditions.

FIGURE 36-18: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 36-4 for load conditions.

37.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Unless otherwise noted, all graphs apply to both the L and LF devices.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum", "Max.", "Minimum" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

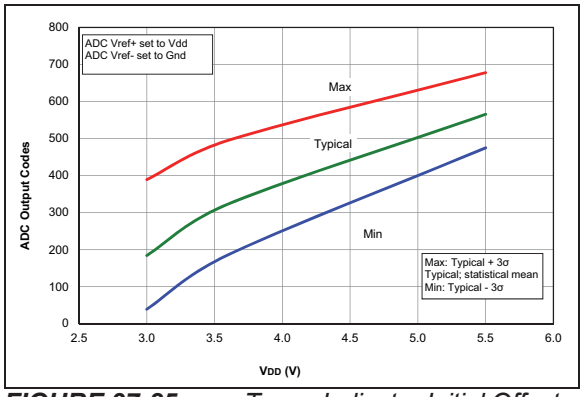


FIGURE 37-85: *Temp. Indicator Initial Offset, High Range, Temp. = 20°C, PIC16F1764/5/8/9 Only..*

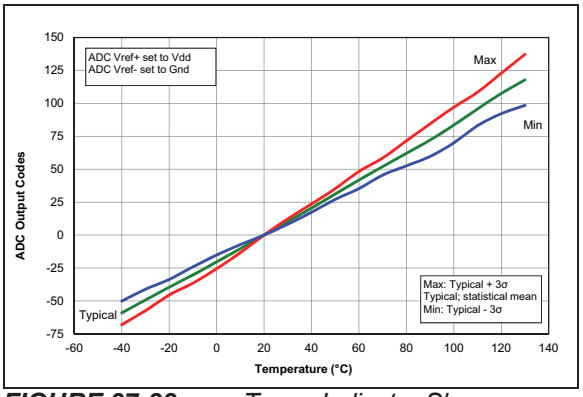


FIGURE 37-88: *Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 5.5V, PIC16F1764/5/8/9 Only.*

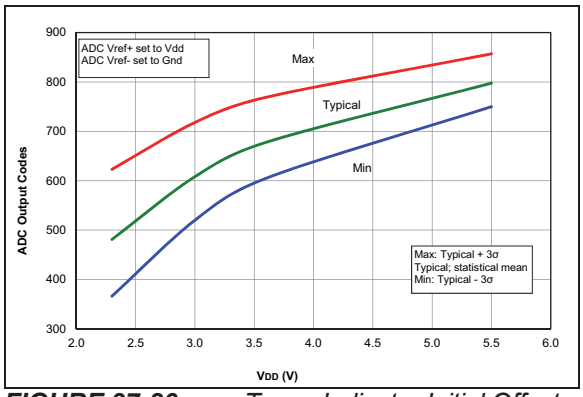


FIGURE 37-86: *Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16F1764/5/8/9 Only.*

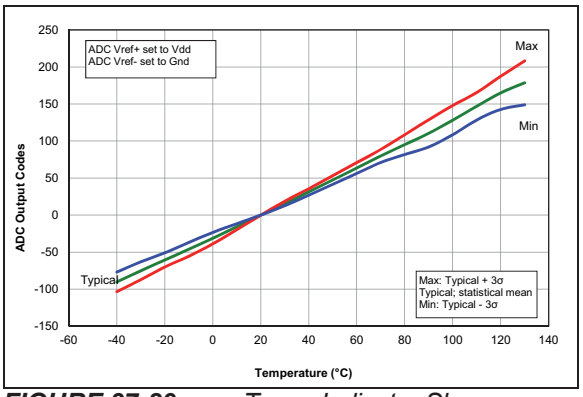


FIGURE 37-89: *Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 3.6V, PIC16F1764/5/8/9 Only.*

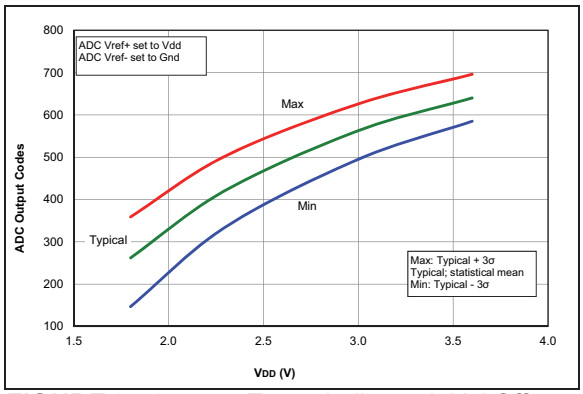


FIGURE 37-87: *Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16LF1764/5/8/9 Only.*

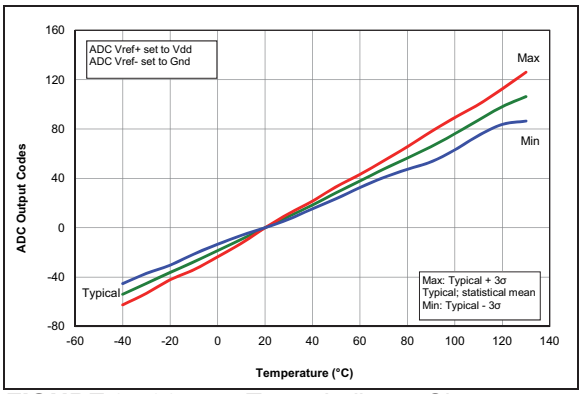


FIGURE 37-90: *Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 3.0V, PIC16F1764/5/8/9 Only.*