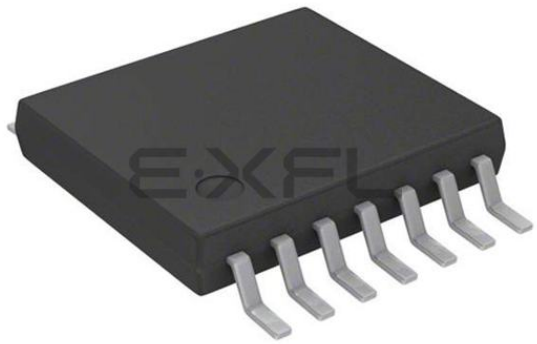


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 1x5b, 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1764t-i-st

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1768/9)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Programmable Ramp Generator	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RA0	19	16	AN0	VREF- DAC1REF- DAC2REF- DAC3REF- DAC4REF-	DAC1OUT1 DAC2OUT1 DAC3OUT1 DAC4OUT1	—	C1IN0+ C3IN0+	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPDAT
RA1	18	15	AN1	VREF+ DAC1REF+ DAC2REF+ DAC3REF+ DAC4REF+	—	—	C1IN0- C2IN0- C3IN0- C4IN0-	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	ICSPCLK
RA2	17	14	AN2	—	—	—	—	ZCD	—	T0CKI(1)	—	—	COG1IN(1) COG2IN(1)	—	—	—	—	INT(1) IOC	Y	—	—
RA3(4)	4	1	—	—	—	—	—	—	—	T6IN(1)	—	—	—	—	MD1CH(1) MD2CH(1)	—	—	IOC	Y	—	VPP MCLR ICD
RA4	3	20	AN3	—	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	MD1CL(1) MD2CL(1)	—	—	IOC	Y	—	OSC2 CLKOUT
RA5	2	19	—	—	—	—	—	—	—	T1CKI(1) T2IN(1) SOSCI	—	—	—	CLCIN3(1)	MD1MOD(1) MD2MOD(1)	—	—	IOC	Y	—	OSC1 CLKIN
RB4	13	10	AN10	—	—	OPA1IN0-	—	—	—	—	—	—	—	—	—	—	SDI(1) SDA(1,3)	IOC	Y	—	—
RB5	12	9	AN11	—	—	OPA1IN0+	—	—	—	—	—	—	—	—	—	RX(1,3)	—	IOC	Y	—	—
RB6	11	8	—	—	—	—	C1IN1+ C3IN1+	—	—	—	—	—	—	—	—	—	SCL(1) SCK(1,3)	IOC	Y	—	—
RB7	10	7	—	—	—	—	C2IN1+ C4IN1+	—	—	—	—	—	—	—	—	CK(1)	—	IOC	Y	—	—
RC0	16	13	AN4	—	—	—	C2IN0+ C4IN0+	—	—	T5CKI(1)	—	—	—	—	—	—	—	IOC	Y	—	—
RC1	15	12	AN5	—	—	—	C1IN1- C2IN1- C3IN1- C4IN1-	—	—	T4IN(1)	—	—	—	CLCIN2(1)	—	—	—	IOC	Y	—	—
RC2	14	11	AN6	—	—	OPA1OUT OPA2IN1- OPA2IN1+	C1IN2- C2IN2-	—	PRG1IN0 PRG2IN1	—	—	—	—	—	—	—	—	IOC	Y	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection register. See Table 12-1.
2: All pin outputs default to PORT latch data. Any input capable pin can be selected as a digital peripheral output with the PPS Output Selection registers. See Table 12-2.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: Input only.

TABLE 3-11: PIC16(L)F1764/5/8/9 MEMORY MAP (BANKS 24-31)

BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31	
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)	F80h	Core Registers (Table 3-2)
C0Bh		C8Bh		D0Bh		D8Bh		E0Bh		E8Bh		F0Bh		F8Bh	
C0Ch	—	C8Ch	—	D0Ch	—										
C0Dh	—	C8Dh	—	D0Dh	—										
C0Eh	—	C8Eh	—	D0Eh	—										
C0Fh	—	C8Fh	—	D0Fh	—										
C10h	—	C90h	—	D10h	—										
C11h	—	C91h	—	D11h	—										
C12h	—	C92h	—	D12h	—										
C13h	—	C93h	—	D13h	—										
C14h	—	C94h	—	D14h	—										
C15h	—	C95h	—	D15h	—										
C16h	—	C96h	—	D16h	—										
C17h	—	C97h	—	D17h	—										
C18h	—	C98h	—	D18h	—		See Table 3-12 and Table 3-13 for Register Mapping Details		See Table 3-12 and Table 3-13 for Register Mapping Details		See Table 3-12 and Table 3-13 for Register Mapping Details		See Table 3-12 and Table 3-13 for Register Mapping Details		See Table 3-14 for Register Mapping Details
C19h	—	C99h	—	D19h	—										
C1Ah	—	C9Ah	—	D1Ah	—										
C1Bh	—	C9Bh	—	D1Bh	—										
C1Ch	—	C9Ch	—	D1Ch	—										
C1Dh	—	C9Dh	—	D1Dh	—										
C1Eh	—	C9Eh	—	D1Eh	—										
C1Fh	—	C9Fh	—	D1Fh	—										
C20h	Unimplemented Read as '0'	CA0h	Unimplemented Read as '0'	D20h	Unimplemented Read as '0'										
C6Fh		CEFh		D6Fh		DEFh		E6Fh		EEFh		F6Fh		FEFh	
C70h	Accesses 70h-7Fh	CF0h	Accesses 70h-7Fh	D70h	Accesses 70h-7Fh	DF0h	Accesses 70h-7Fh	E70h	Accesses 70h-7Fh	EF0h	Accesses 70h-7Fh	F70h	Accesses 70h-7Fh	FF0h	Accesses 70h-7Fh
CFFh		CFFh		D7Fh		DFFh		E7Fh		EFFh		F7Fh		FFFh	

Legend: ☐ = Unimplemented data memory locations, read as '0'.

TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 8											
40Ch — 40Dh	—	Unimplemented								—	—
40Eh	HIDRVC	—	—	HIDC<5:4>		—	—	—	—	--00 ----	--00 ----
40Fh — 412h	—	Unimplemented								—	—
413h	T4TMR	Holding Register for the 8-Bit TMR4 Register								0000 0000	0000 0000
413h	T4PR	TMR4 Period Register								1111 1111	1111 1111
415h	T4CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
416h	T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
417h	T4CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
418h	T4RST	—	—	—	—	RSEL<3:0>				---- 0000	---- 0000
419h	—	Unimplemented								—	—
41Ah	T6TMR	Holding Register for the 8-Bit TMR4 Register								0000 0000	0000 0000
41Bh	T6PR	TMR4 Period Register								1111 1111	1111 1111
41Ch	T6CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
41Dh	T6HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
41Eh	T6CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
41Fh	T6RST	—	—	—	—	RSEL<3:0>				---- 0000	---- 0000
Bank 9											
48Ch to 492h	—	Unimplemented								—	—
493h	TMR3L	Holding Register for the Least Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
494h	TMR3H	Holding Register for the Most Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
495h	T3CON	CS<1:0>		CKPS<1:0>		OSCEN	$\overline{\text{SYNC}}$	—	ON	0000 00-0	uuuu uu-u
496h	T3GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	GSS<1:0>		0000 0x00	uuuu uxuu
497h to 499h	—	Unimplemented								—	—
49Ah	TMR5L	Holding Register for the Least Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
49Bh	TMR5H	Holding Register for the Most Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
49Ch	T5CON	CS<1:0>		CKPS<1:0>		OSCEN	$\overline{\text{SYNC}}$	—	ON	0000 00-0	uuuu uu-u
49Dh	T5GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	GSS<1:0>		0000 0x00	uuuu uxuu
49Eh to 49Fh	—	Unimplemented								—	—

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: PIC16(L)F1768/9 only.
3: PIC16(L)F1764/5 only.
4: Unimplemented on PIC16LF1764/5/8/9.

5.4 Two-Speed Clock Start-up Mode

Two-Speed Clock Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the Internal Oscillator Block, INTOSC, as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

Note:	Executing a `SLEEP` instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCSTAT register to remain clear.

5.4.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Words) = `1`; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS<1:0> (of the OSCCON register) = `00`.
- FOSC<2:0> bits in the Configuration Words configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

TABLE 5-1: OSCILLATOR SWITCHING DELAYS

Switch From	Switch To	Frequency	Oscillator Delay
Sleep	LFINTOSC MFINTOSC HFINTOSC(1)	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-up Delay (TWARM)(2)
Sleep	EC, RC(1)	DC- 32 MHz	2 cycles
LFINTOSC	EC, RC(1)	DC-32 MHz	1 Cycle of Each
Sleep	Secondary Oscillator LP, XT, HS(1)	32 kHz-20 MHz	1024 Clock Cycles (OST)
Any Clock Source	MFINTOSC HFINTOSC(1)	31.25 kHz-500 kHz 31.25 kHz-16 MHz	2 μs (approx.)
Any Clock Source	LFINTOSC	31 kHz	1 Cycle of Each
Any Clock Source	Secondary Oscillator	32 kHz	1024 Clock Cycles (OST)
PLL Inactive	PLL Active	16-32 MHz	2 ms (approx.)

Note 1: PLL is inactive.

2: See Table 36-8.

15.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 16.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

15.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μs between sequential conversions of the temperature indicator output.

TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVR<1:0>		ADFVR<1:0>		169

Legend: Shaded cells are unused by the temperature indicator module.

20.9 Register Definitions: ZCD Control

Long bit name prefixes for the Zero-Cross Detect peripheral are shown in Table 20-1. Refer to **Section 1.1.2.2 "Long Bit Names"** for more information

TABLE 20-1: BIT NAME PREFIXES

Peripheral	Bit Name Prefix
ZCD1	ZCD1

REGISTER 20-1: ZCDxCON: ZERO-CROSS DETECTION x CONTROL REGISTER

R/W-0/0	U-0	R-x/x	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
EN(1)	—	OUT	POL	—	—	INTP	INTN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7 **EN:** Zero-Cross Detection Enable bit(1)
1 = Zero-Cross Detect is enabled; ZCD pin is forced to output to source and sink current
0 = Zero-Cross Detect is disabled; ZCD pin operates according to PPS and TRISx controls

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Zero-Cross Detection Logic Level bit
POL bit = 0:
1 = ZCD pin is sinking current
0 = ZCD pin is sourcing current
POL bit = 1:
1 = ZCD pin is sourcing current
0 = ZCD pin is sinking current

bit 4 **POL:** Zero-Cross Detection Logic Output Polarity bit
1 = ZCD logic output is inverted
0 = ZCD logic output is not inverted

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **INTP:** Zero-Cross Positive Edge Interrupt Enable bit
1 = ZCDIF bit is set on low-to-high OUT transition
0 = ZCDIF bit is unaffected by low-to-high OUT transition

bit 0 **INTN:** Zero-Cross Negative Edge Interrupt Enable bit
1 = ZCDIF bit is set on high-to-low OUT transition
0 = ZCDIF bit is unaffected by high-to-low OUT transition

Note 1: The EN bit has no effect when the $\overline{\text{ZCD}}$ Configuration bit is cleared.

22.3 Timer1 Prescaler

Timer1 has four prescaler options, allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS<1:0> bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

22.4 Timer1 (Secondary) Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built in between pins, SOSCI (input) and SOSCO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the OSCEN bit of the T1CON register. The oscillator will continue to run during Sleep.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, OSCEN should be set and a suitable delay observed prior to using Timer1. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

22.5 Timer1 Operation in Asynchronous Counter Mode

If the control bit, $\overline{\text{SYNC}}$ of the T1CON register, is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt-on-overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 22.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

22.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

22.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 Gate Enable.

Timer1 gate can also be driven by multiple selectable sources.

22.6.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 22-3 for timing details.

TABLE 22-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

REGISTER 26-2: PWMxINTE: PWMx INTERRUPT ENABLE REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	OFIE	PHIE	DCIE	PRIE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OFIE**: Offset Interrupt Enable bit
1 = Interrupts CPU on offset match
0 = Does not interrupt CPU on offset match

bit 2 **PHIE:** Phase Interrupt Enable bit
1 = Interrupts CPU on phase match
0 = Does not interrupt CPU on phase match

bit 1 **DCIE:** Duty Cycle Interrupt Enable bit
1 = Interrupts CPU on duty cycle match
0 = Does not interrupt CPU on duty cycle match

bit 0 **PRIE:** Period Interrupt Enable bit
1 = Interrupts CPU on period match
0 = Does not interrupt CPU on period match

FIGURE 27-9: TYPICAL HALF-BRIDGE MODE COG OPERATION WITH CCP1

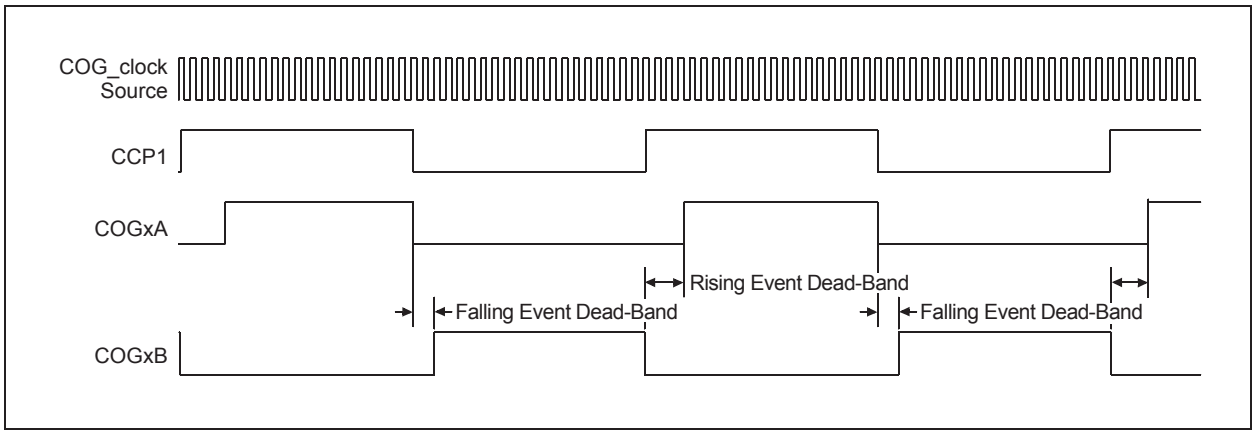


FIGURE 27-10: HALF-BRIDGE MODE COG OPERATION WITH CCP1 AND PHASE DELAY

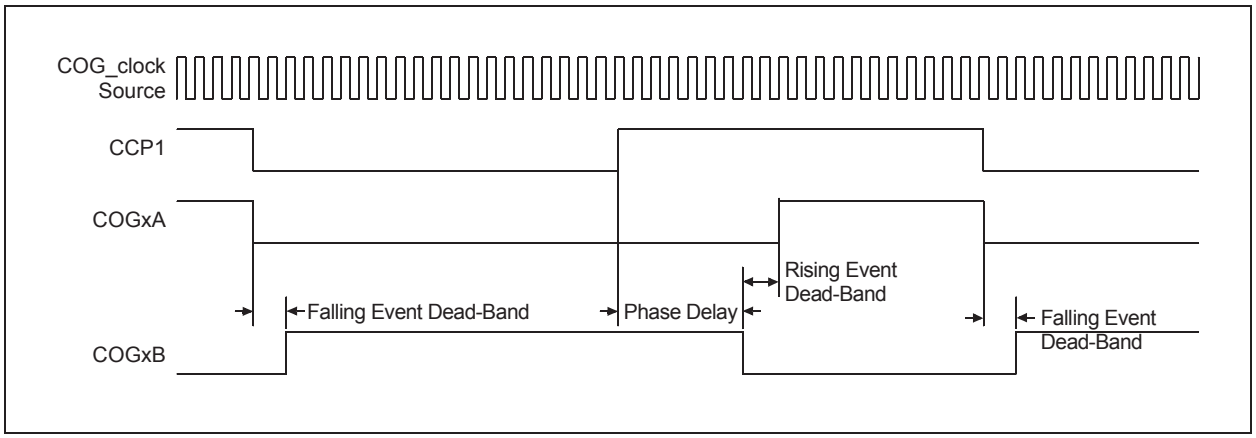
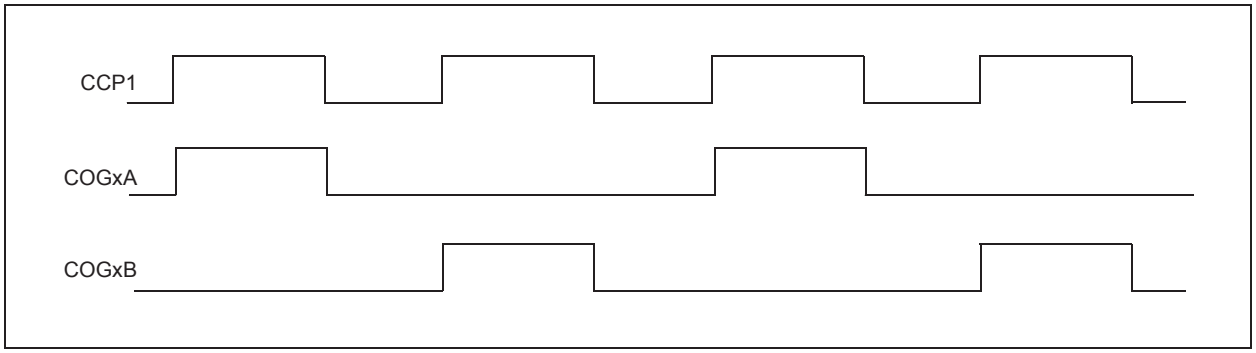


FIGURE 27-11: PUSH-PULL MODE COG OPERATION WITH CCP1



REGISTER 27-10: COGxFSIM1: COGx FALLING EVENT SOURCE INPUT MODE REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FSIM15(1)	FSIM14	FSIM13	FSIM12	FSIM11	FSIM10	FSIM9	FSIM8
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **FSIM15:** COGx Falling Event Input Source 15 Mode bit(1)

FIS15 = 1:
1 = DSM2 MD2_out output high-to-low transition will cause a falling event after falling event phase delay
0 = DSM2 MD2_out low level will cause an immediate falling event

FIS15 = 0:
DSM2 MD2_out output has no effect on falling event.

bit 6 **FSIM14:** COGx Falling Event Input Source 14 Mode bit

FIS14 = 1:
1 = DSM1 MD1_out output high-to-low transition will cause a falling event after falling event phase delay
0 = DSM1 MD1_out output low level will cause an immediate falling event

FIS14 = 0:
DSM1 MD1_out output has no effect on falling event.

bit 5 **FSIM13:** COGx Falling Event Input Source 13 Mode bit

FIS13 = 1:
1 = CLC3 output high-to-low transition will cause a falling event after falling event phase delay
0 = CLC3 output low level will cause an immediate falling event

FIS13 = 0:
CLC3 output has no effect on falling event.

bit 4 **FSIM12:** COGx Falling Event Input Source 12 Mode bit

FIS12 = 1:
1 = CLC2 output high-to-low transition will cause a falling event after falling event phase delay
0 = CLC2 output low level will cause an immediate falling event

FIS12 = 0:
CLC2 output has no effect on falling event.

bit 3 **FSIM11:** COGx Falling Event Input Source 11 Mode bit

FIS11 = 1:
1 = CLC1 output high-to-low transition will cause a falling event after falling event phase delay
0 = CLC1 output low level will cause an immediate falling event

FIS11 = 0:
CLC1 output has no effect on falling event.

bit 2 **FSIM10:** COGx Falling Event Input Source 10 Mode bit

FIS10 = 1:
1 = PWM6 output high-to-low transition will cause a falling event after falling event phase delay
0 = PWM6 output low level will cause an immediate falling event

FIS10 = 0:
Comparator 2 has no effect on falling event.

Note 1: PIC16(L)F1768/9 only. Otherwise unimplemented, read as '0'.

28.1.5 CLCx SETUP STEPS

The following steps should be followed when setting up the CLCx:

- Disable CLCx by clearing the EN bit.
- Select desired inputs using CLCxSEL0 through CLCxSEL3 registers (see Table 28-1).
- Clear any associated ANSELx bits.
- Set all TRISx bits associated with inputs.
- Clear all TRISx bits associated with outputs.
- Enable the chosen inputs through the four gates using CLCxGLS0, CLCxGLS1, CLCxGLS2, and CLCxGLS3 registers.
- Select the gate output polarities with the POLy bits of the CLCxPOL register.
- Select the desired logic function with the MODE<2:0> bits of the CLCxCON register.
- Select the desired polarity of the logic output with the POL bit of the CLCxPOL register. (This step may be combined with the previous gate output polarity step).
- If driving a device pin, set the desired Pin PPS Control register and also clear the TRISx bit corresponding to that output.
- If interrupts are desired, configure the following bits:
  - Set the INTP bit in the CLCxCON register for a rising event.
  - Set the INTN bit in the CLCxCON register for a falling event.
  - Set the CLCxIE bit of the associated PIE registers.
  - Set the GIE and PEIE bits of the INTCON register.
- Enable the CLCx by setting the EN bit of the CLCxCON register.

28.2 CLCx Interrupts

An interrupt will be generated upon a change in the output value of the CLCx when the appropriate interrupt enables are set. A rising edge detector and a falling edge detector are present in each CLC for this purpose.

The CLCxIF bit of the associated PIR registers will be set when either edge detector is triggered and its associated enable bit is set. The INTP enables rising edge interrupts and the INTN bit enables falling edge interrupts. Both are located in the CLCxCON register.

To fully enable the interrupt, set the following bits:

- EN bit of the CLCxCON register
- CLCxIE bit of the associated PIE registers
- INTP bit of the CLCxCON register (for a rising edge detection)
- INTN bit of the CLCxCON register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The CLCxIF bit of the associated PIR registers must be cleared in software as part of the interrupt service. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

28.3 Output Mirror Copies

Mirror copies of all CLCxCON output bits are contained in the CLCxDATA register. Reading this register reads the outputs of all CLCs simultaneously. This prevents any reading skew introduced by testing or reading the CLCxOUT bits in the individual CLCxCON registers.

28.4 Effects of a Reset

The CLCxCON register is cleared to zero as the result of a Reset. All other selection and gating values remain unchanged.

28.5 Operation During Sleep

The CLCx module operates independently from the system clock and will continue to run during Sleep, provided that the input sources selected remain active.

The HFINTOSC remains active during Sleep when the CLCx module is enabled and the HFINTOSC is selected as an input source, regardless of the system clock source selected.

In other words, if the HFINTOSC is simultaneously selected as the system clock and as a CLCx input source when the CLCx is enabled, the CPU will go Idle during Sleep, but the CLCx will continue to operate and the HFINTOSC will remain active.

This will have a direct effect on the Sleep mode current.

REGISTER 28-11: CLCxDATA: CLCx DATA OUTPUT

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	MLC3OUT	MLC2OUT	MLC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **MLC3OUT:** Mirror copy of LC3OUT bit

bit 1 **MLC2OUT:** Mirror copy of LC2OUT bit

bit 0 **MLC1OUT:** Mirror copy of LC1OUT bit

TABLE 28-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx

Name	Bit7	Bit6	Bit5	Bit4	BIt3	Bit2	Bit1	Bit0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELB(1)	ANSB<7:4>				—	—	—	—	143
ANSELC	ANSC<7:6>(1)		—	—	ANSC<3:0>				148
CLCxCON	EN	—	OUT	INTP	INTN	MODE<2:0>			338
CLCDATA	—	—	—	—	—	MLC3OUT	MLC2OUT	MLC1OUT	345
CLCxGLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	341
CLCxGLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	342
CLCxGLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	343
CLCxGLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	344
CLCxPOL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	339
CLCxSEL0	—	—	D1S<5:0>						340
CLCxSEL1	—	—	D2S<5:0>						340
CLCxSEL2	—	—	D3S<5:0>						340
CLCxSEL3	—	—	D4S<5:0>						341
CLCxPPS	—	—	—	CLCxPPS<4:0>					154, 156
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
PIE3	PWM6IE(1)	PWM5IE	COG1IE	ZCDIE	COG2IE(1)	CLC3IE	CLC2IE	CLC1IE	104
PIR3	PWM6IF(1)	PWM5IF	COG1IF	ZCDIF	COG2IF(1)	CLC3IF	CLC2IF	CLC1IF	107
RxyPPS	—	—	—	RxyPPS<4:0>					154
TRISA	—	—	TRISA<5:4>		—(3)	TRISA<2:0>			136
TRISB(1)	TRISB<7:4>				—	—	—	—	142
TRISC	TRISC<7:6>(1)		TRISC<5:0>						147

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for CLCx module.

Note 1: PIC16(L)F1768/9 only.

2: Unimplemented, read as '1'.

32.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

TABLE 32-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELC	ANSC<7:6>(2)		—	—	ANSC<3:0>				148
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	102
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	105
RxyPPS	—	—	—	RxyPPS<4:0>					154
SSPCLKPPS	—	—	—	SSPCLKPPS<4:0>					154, 156
SSPDATPPS	—	—	—	SSPDATPPS<4:0>					154, 156
SSPSSPPS	—	—	—	SSPSSPPS<4:0>					154, 156
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								380*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				426
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	424
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	424
TRISA	—	—	TRISA<5:4>		—(1)	TRISA<2:0>			136
TRISB(2)	TRISB<7:4>				—	—	—	—	142
TRISC	TRISC<7:6>(2)		TRISC<5:0>						147

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

* Page provides register information.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1768/9 only.

FIGURE 32-20: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)

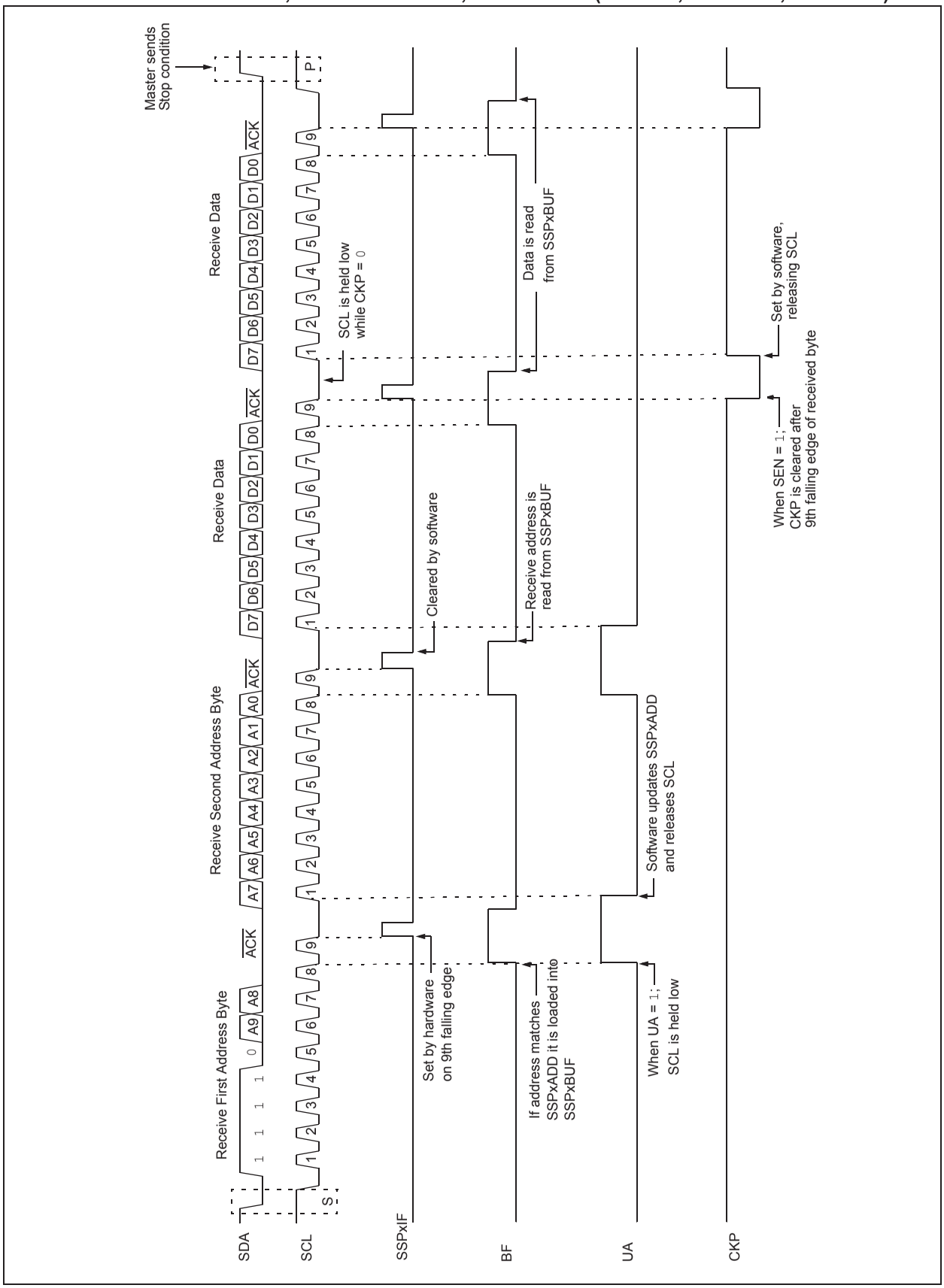


FIGURE 32-29: I²C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)

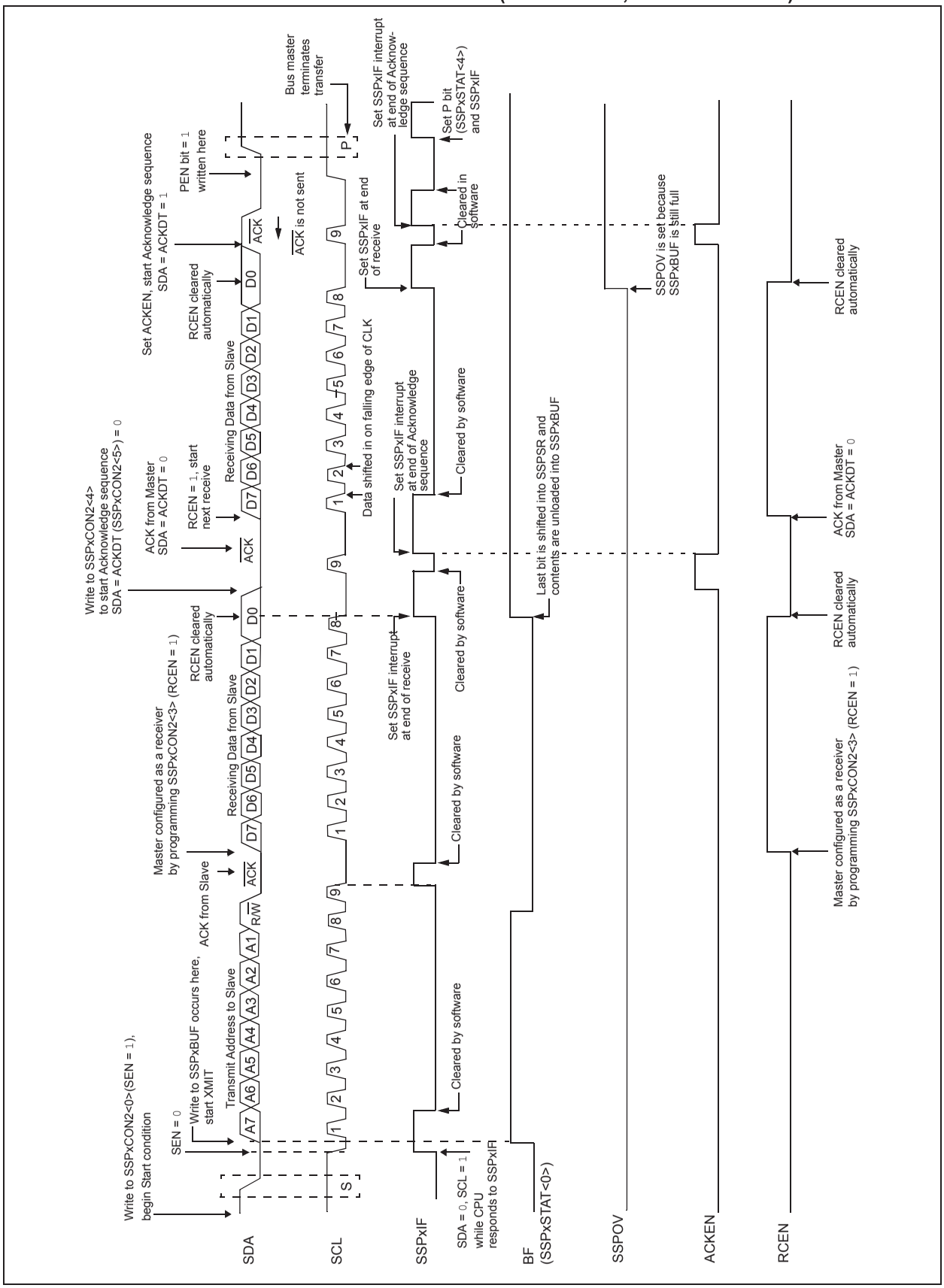
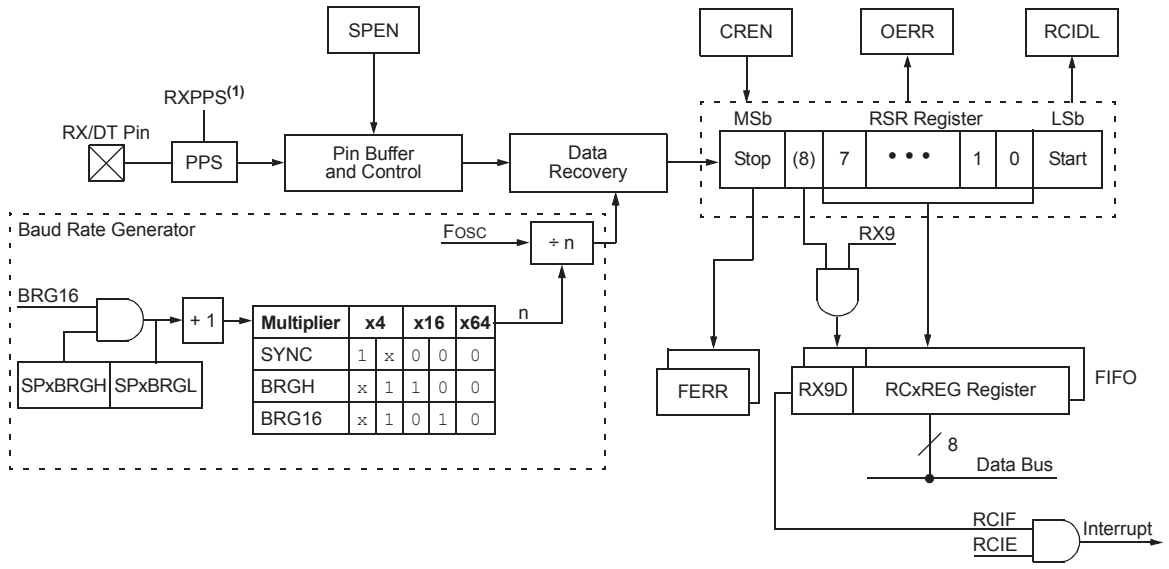


FIGURE 33-2: EUSART RECEIVE BLOCK DIAGRAM



Note 1: In Synchronous mode, the DT output and RX input PPS selections should enable the same pin.

The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXxSTA)
- Receive Status and Control (RCxSTA)
- Baud Rate Control (BAUDxCON)

These registers are detailed in Register 33-1, Register 33-2 and Register 33-3, respectively.

The RX and CK input pins are selected with the RXPPS and CKPPS registers, respectively. TX, CK and DT output pins are selected with each pin's RxyPPS register. Since the RX input is coupled with the DT output in Synchronous mode, it is the user's responsibility to select the same pin for both of these functions when operating in Synchronous mode. The EUSART control logic will control the data direction drivers automatically.

TABLE 35-3: PIC16(L)F1764/5/8/9 INSTRUCTION SET (CONTINUED)

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb	LSb	Status Affected	Notes
CONTROL OPERATIONS							
BRA	k	Relative Branch	2	11 001k kkkk kkkk			
BRW	–	Relative Branch with W	2	00 0000 0000 1011			
CALL	k	Call Subroutine	2	10 0kkk kkkk kkkk			
CALLW	–	Call Subroutine with W	2	00 0000 0000 1010			
GOTO	k	Go to address	2	10 1kkk kkkk kkkk			
RETFIE	k	Return from interrupt	2	00 0000 0000 1001			
RETLW	k	Return with literal in W	2	11 0100 kkkk kkkk			
RETURN	–	Return from Subroutine	2	00 0000 0000 1000			
INHERENT OPERATIONS							
CLRWDT	–	Clear Watchdog Timer	1	00 0000 0110 0100		$\overline{TO}$, $\overline{PD}$	
NOP	–	No Operation	1	00 0000 0000 0000			
OPTION	–	Load OPTION_REG register with W	1	00 0000 0110 0010			
RESET	–	Software device Reset	1	00 0000 0000 0001			
SLEEP	–	Go into Standby mode	1	00 0000 0110 0011		$\overline{TO}$, $\overline{PD}$	
TRIS	f	Load TRIS register with W	1	00 0000 0110 0fff			
C-COMPILER OPTIMIZED							
ADDFSR	n, k	Add Literal k to FSRn	1	11 0001 0nkk kkkk			
MOVIW	n mm	Move Indirect FSRn to W with pre/post inc/dec modifier, mm	1	00 0000 0001 0nmm		Z	**2, 3**
	k[n]	Move INDFn to W, Indexed Indirect.	1	11 1111 0nkk kkkk		Z	**2**
MOVWI	n mm	Move W to Indirect FSRn with pre/post inc/dec modifier, mm	1	00 0000 0001 1nmm			**2, 3**
	k[n]	Move W to INDFn, Indexed Indirect.	1	11 1111 1nkk kkkk			**2**

Note 1: If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

2: If this instruction addresses an INDFn register and the MSb of the corresponding FSRn is set, this instruction will require one additional instruction cycle.

3: See Table 35-3 for the `MOVIW` and `MOVWI` instruction descriptions.

LSLF **Logical Left Shift**

Syntax: [*label*] LSLF f {,d}

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f<7>) → C
(f<6:0>) → dest<7:1>
0 → dest<0>

Status Affected: C, Z

Description: The contents of register 'f' are shifted one bit to the left through the Carry flag. A '0' is shifted into the LSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.

LSRF **Logical Right Shift**

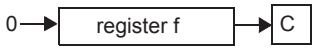
Syntax: [*label*] LSRF f {,d}

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: 0 → dest<7>
(f<7:1>) → dest<6:0>,
(f<0>) → C,

Status Affected: C, Z

Description: The contents of register 'f' are shifted one bit to the right through the Carry flag. A '0' is shifted into the MSb. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Description: The contents of register f are moved to a destination dependent upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:

```
MOVF    FSR, 0
```

After Instruction
W = value in FSRn register
Z = 1

36.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} – Operating Supply Voltage(1)

PIC16LF1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +1.8V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +3.6V

PIC16F1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +2.3V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +5.5V

T_A – Operating Ambient Temperature Range

Industrial Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +85°C

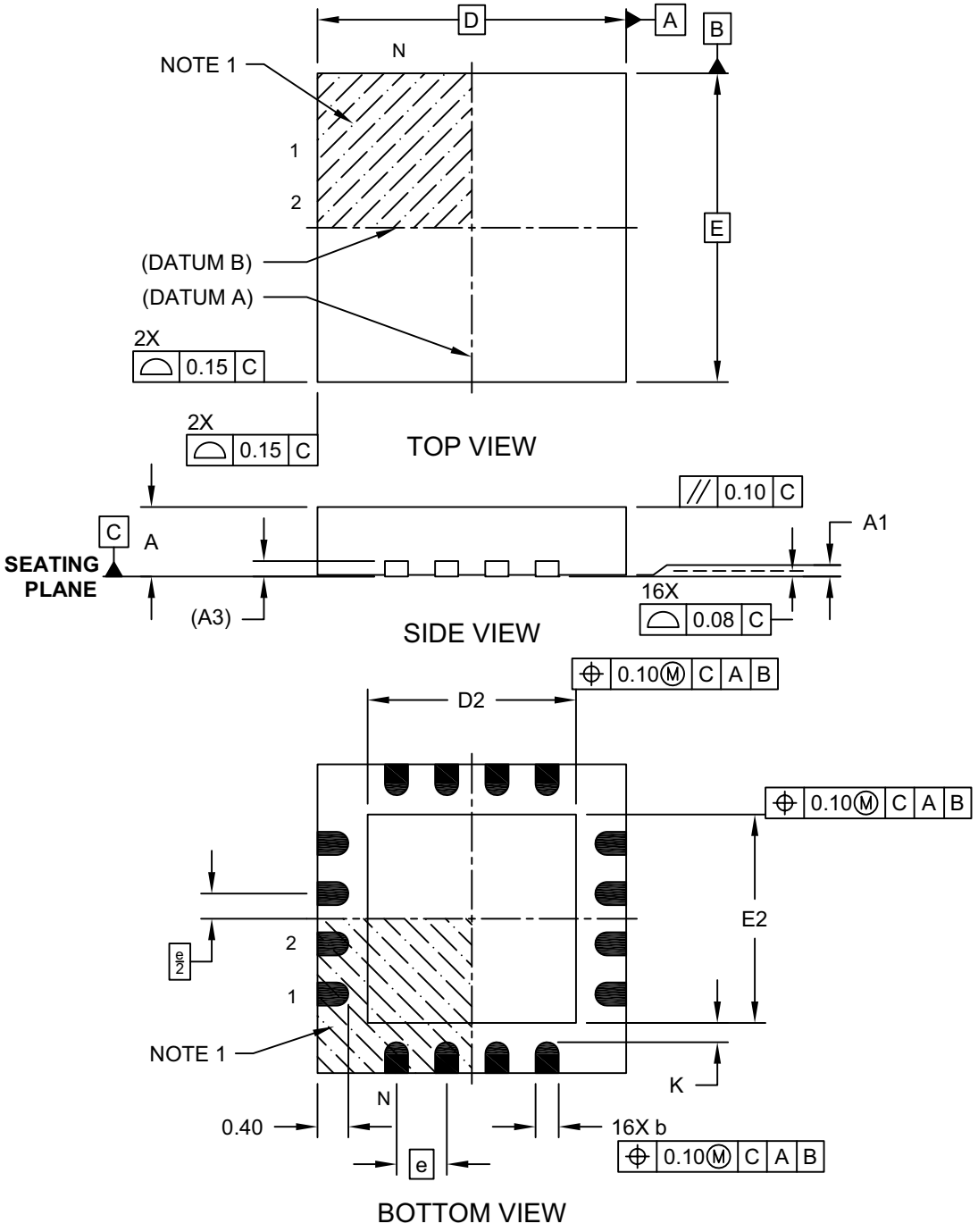
Extended Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

16-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4x0.9mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-127D Sheet 1 of 2