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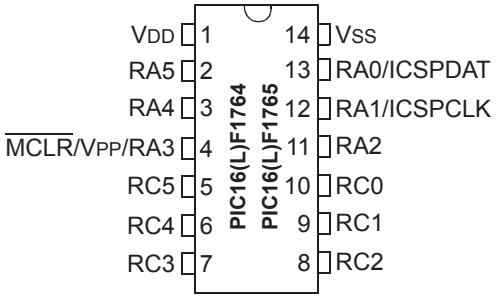
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 1x5b, 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-SOIC (0.154", 3.90mm Width)
Supplier Device Package	14-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1765t-i-sl

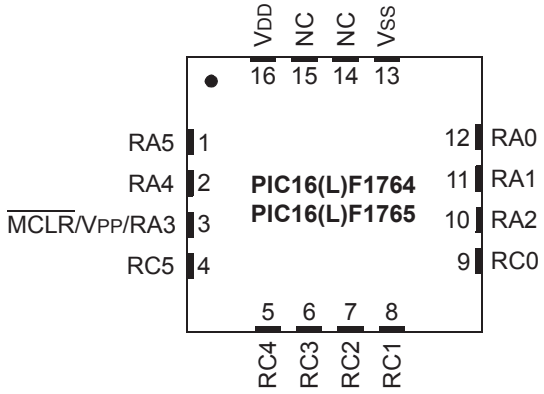
PIN DIAGRAMS

FIGURE 1: 14-PIN PDIP, SOIC, TSSOP



Note: See Table 3 for location of all peripheral functions.

FIGURE 2: 16-PIN QFN (4x4)



Note: See Table 3 for location of all peripheral functions.

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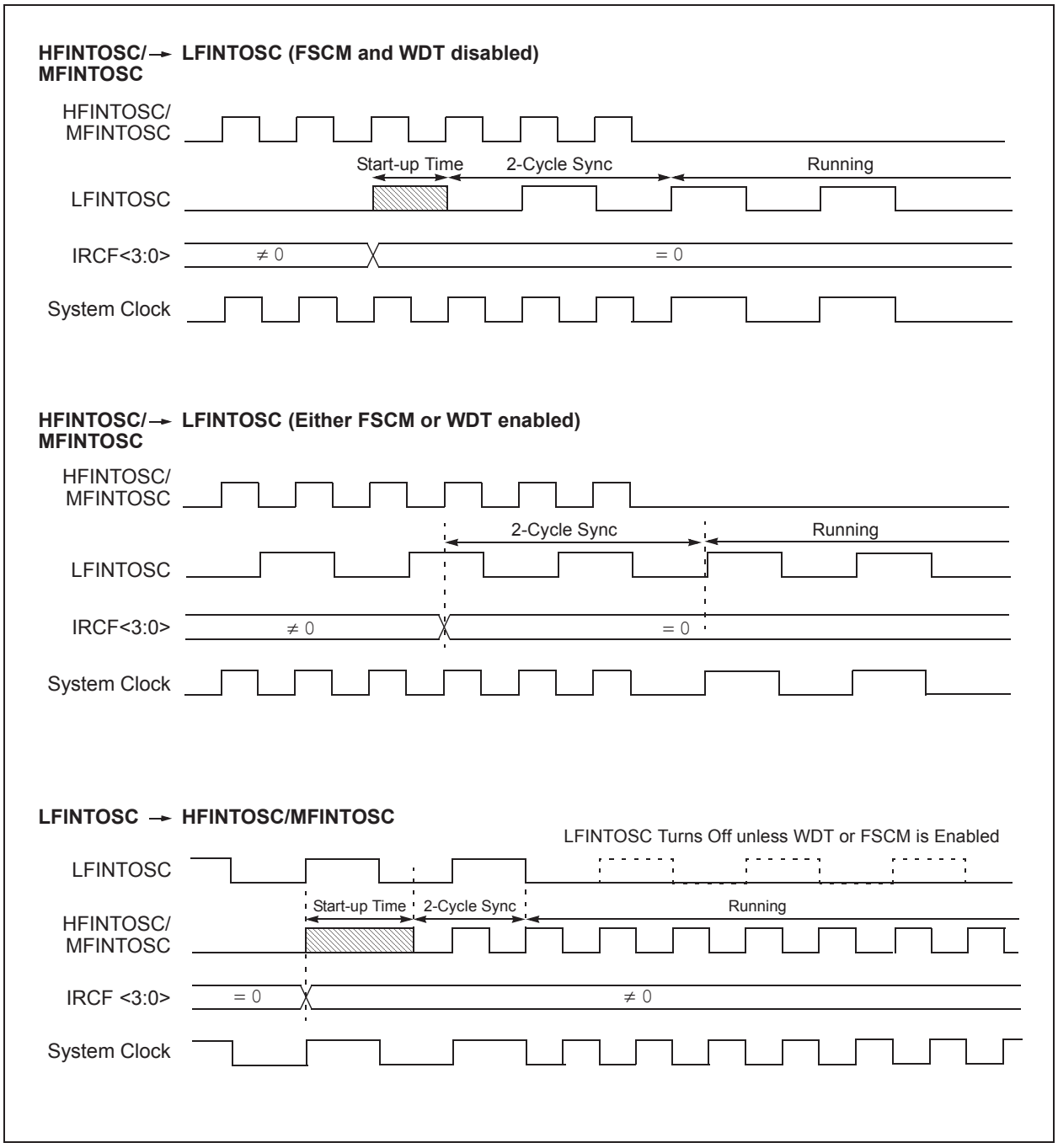
TABLE 3-13: PIC16(L)F1768/9 MEMORY MAP (BANKS 27-30)

	Bank 27		Bank 28		Bank 29		Bank 30
D8Ch	—	E0Ch	—	E8Ch	—	F0Ch	—
D8Dh	—	E0Dh	—	E8Dh	—	F0Dh	—
D8Eh	PWMEN	E0Eh	—	E8Eh	—	F0Eh	—
D8Fh	PWMLD	E0Fh	PPSLOCK	E8Fh	—	F0Fh	CLCDATA
D90h	PWMOUT	E10h	INTPPS	E90h	RA0PPS	F10h	CLC1CON
D91h	PWM5PHL	E11h	T0CKIPPS	E91h	RA1PPS	F11h	CLC1POL
D92h	PWM5PHH	E12h	T1CKIPPS	E92h	RA2PPS	F12h	CLC1SEL0
D93h	PWM5DCL	E13h	T1GPPS	E93h	—	F13h	CLC1SEL1
D94h	PWM5DCH	E14h	CCP1PPS	E94h	RA4PPS	F14h	CLC1SEL2
D95h	PWM5PRL	E15h	CCP2PPS	E95h	RA5PPS	F15h	CLC1SEL3
D96h	PWM5PRH	E16h	COG1INPPS	E96h	—	F16h	CLC1GLS0
D97h	PWM5OFL	E17h	COG2INPPS	E97h	—	F17h	CLC1GLS1
D98h	PWM5OFH	E18h	—	E98h	—	F18h	CLC1GLS2
D99h	PWM5TMRL	E19h	T2INPPS	E99h	—	F19h	CLC1GLS3
D9Ah	PWM5TMRH	E1Ah	T3CKIPPS	E9Ah	—	F1Ah	CLC2CON
D9Bh	PWM5CON	E1Bh	T3GPPS	E9Bh	—	F1Bh	CLC2POL
D9Ch	PWM5INTE	E1Ch	T4INPPS	E9Ch	RB4PPS	F1Ch	CLC2SEL0
D9Dh	PWM5INTF	E1Dh	T5CKIPPS	E9Dh	RB5PPS	F1Dh	CLC2SEL1
D9Eh	PWM5CLKCON	E1Eh	T5GPPS	E9Eh	RB6PPS	F1Eh	CLC2SEL2
D9Fh	PWM5LDCON	E1Fh	T6INPPS	E9Fh	RB7PPS	F1Fh	CLC2SEL3
DA0h	PWM5OFCON	E20h	SSPCLKPPS	EA0h	RC0PPS	F20h	CLC2GLS0
DA1h	PWM6PHL	E21h	SSPDATPPS	EA1h	RC1PPS	F21h	CLC2GLS1
DA2h	PWM6PHH	E22h	SSPSSPPS	EA2h	RC2PPS	F22h	CLC2GLS2
DA3h	PWM6DCL	E23h	—	EA3h	RC3PPS	F23h	CLC2GLS3
DA4h	PWM6DCH	E24h	RXPPS	EA4h	RC4PPS	F24h	CLC3CON
DA5h	PWM6PRL	E25h	CKPPS	EA5h	RC5PPS	F25h	CLC3POL
DA6h	PWM6PRH	E26h	—	EA6h	RC6PPS	F26h	CLC3SEL0
DA7h	PWM6OFL	E27h	—	EA7h	RC7PPS	F27h	CLC3SEL1
DA8h	PWM6OFH	E28h	CLCIN0PPS	EA8h	—	F28h	CLC3SEL2
DA9h	PWM6TMRL	E29h	CLCIN1PPS	EA9h	—	F29h	CLC3SEL3
DAAh	PWM6TMRH	E2Ah	CLCIN2PPS	EAAh	—	F2Ah	CLC3GLS0
DABh	PWM6CON	E2Bh	CLCIN3PPS	EABh	—	F2Bh	CLC3GLS1
DACh	PWM6INTE	E2Ch	PRG1FPPS	EACh	—	F2Ch	CLC3GLS2
DADh	PWM6INTF	E2Dh	PRG1RPPS	EADh	—	F2Dh	CLC3GLS3
DAEh	PWM6CLKCON	E2Eh	PRG2FPPS	EAEh	—	F2Eh	—
DAFh	PWM6LDCON	E2Fh	PRG2RPPS	EAFh	—	F2Fh	—
DB0h	PWM6OFCON	E30h	MD1CHPPS	EB0h	—	F30h	—
DB1h	—	E31h	MD1CLPPS	EB1h	—	F31h	—
DB2h	—	E32h	MD1MODPPS	EB2h	—	F32h	—
DB3h	—	E33h	MD2CHPPS	EB3h	—	F33h	—
DB4h	—	E34h	MD2CLPPS	EB4h	—	F34h	—
DB5h	—	E35h	MD2MODPPS	EB5h	—	F35h	—
DB6h	—	E36h	—	EB6h	—	F36h	—
DB7h	—	E37h	—	EB7h	—	F37h	—
DB8h	—	E38h	—	EB8h	—	F38h	—
DB9h	—	E39h	—	EB9h	—	F39h	—
DBAh	—	E3Ah	—	EBAh	—	F3Ah	—
DBBh	—	E3Bh	—	EBBh	—	F3Bh	—
DBCh	—	E3Ch	—	EBCh	—	F3Ch	—
DBDh	—	E3Dh	—	EBDh	—	F3Dh	—
DBEh	—	E3Eh	—	EBEh	—	F3Eh	—
DBFh	—	E3Fh	—	EBFh	—	F3Fh	—
DC0h — DEFh		E40h — E6Fh		EC0h — EEFh		F40h — F6Fh	

Legend: ☐ = Unimplemented data memory locations, read as '0',

FIGURE 5-7: INTERNAL OSCILLATOR SWITCH TIMING



5.4 Two-Speed Clock Start-up Mode

Two-Speed Clock Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the Internal Oscillator Block, INTOSC, as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

Note:	Executing a `SLEEP` instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCSTAT register to remain clear.

5.4.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Words) = `1`; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS<1:0> (of the OSCCON register) = `00`.
- FOSC<2:0> bits in the Configuration Words configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

TABLE 5-1: OSCILLATOR SWITCHING DELAYS

Switch From	Switch To	Frequency	Oscillator Delay
Sleep	LFINTOSC MFINTOSC HFINTOSC(1)	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-up Delay (TWARM)(2)
Sleep	EC, RC(1)	DC- 32 MHz	2 cycles
LFINTOSC	EC, RC(1)	DC-32 MHz	1 Cycle of Each
Sleep	Secondary Oscillator LP, XT, HS(1)	32 kHz-20 MHz	1024 Clock Cycles (OST)
Any Clock Source	MFINTOSC HFINTOSC(1)	31.25 kHz-500 kHz 31.25 kHz-16 MHz	2 μs (approx.)
Any Clock Source	LFINTOSC	31 kHz	1 Cycle of Each
Any Clock Source	Secondary Oscillator	32 kHz	1024 Clock Cycles (OST)
PLL Inactive	PLL Active	16-32 MHz	2 ms (approx.)

Note 1: PLL is inactive.

2: See Table 36-8.

6.0 RESETS

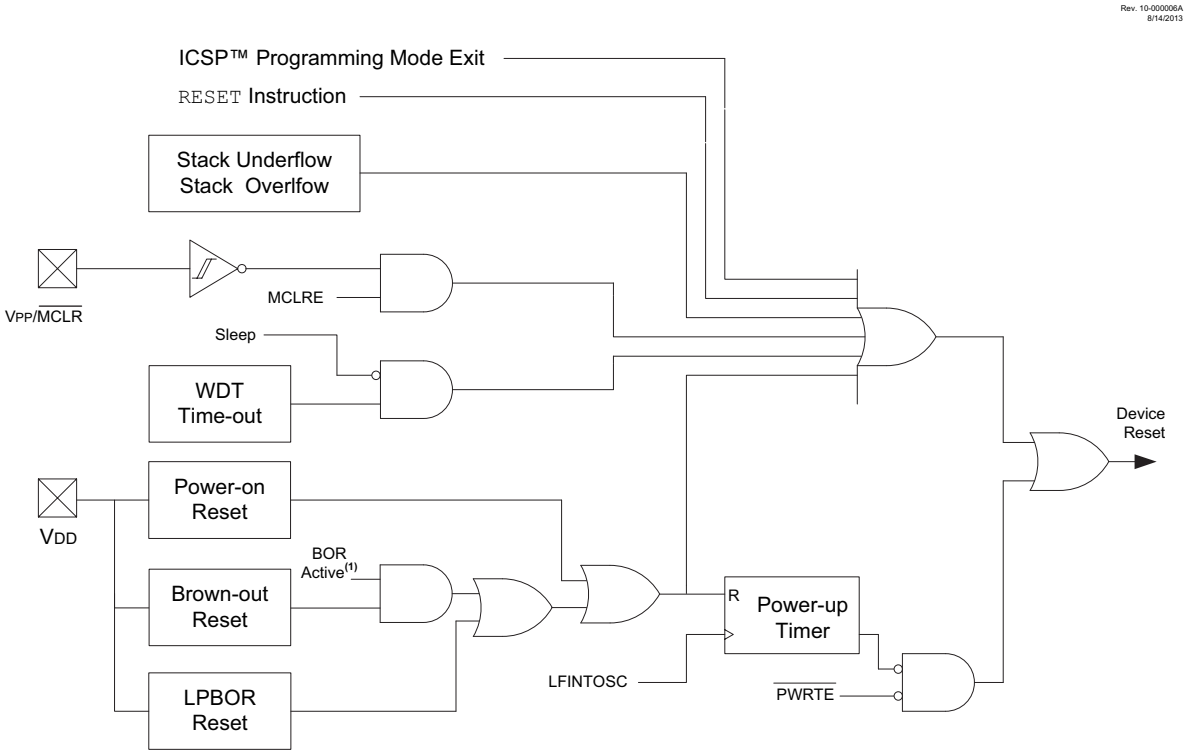
There are multiple ways to reset this device:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- Low-Power Brown-out Reset (LPBOR)
- $\overline{\text{MCLR}}$ Reset
- WDT Reset
- RESET instruction
- Stack Overflow
- Stack Underflow
- Programming mode exit

To allow VDD to stabilize, an optional power-up timer can be enabled to extend the Reset time after a BOR or POR event.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 6-1.

FIGURE 6-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: See Table 6-1 for BOR active conditions.

6.2.1 BOR IS ALWAYS ON

When the BOREN<1:0> bits of the Configuration Words are programmed to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

6.2.2 BOR IS OFF IN SLEEP

When the BORENx bits of the Configuration Words are programmed to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

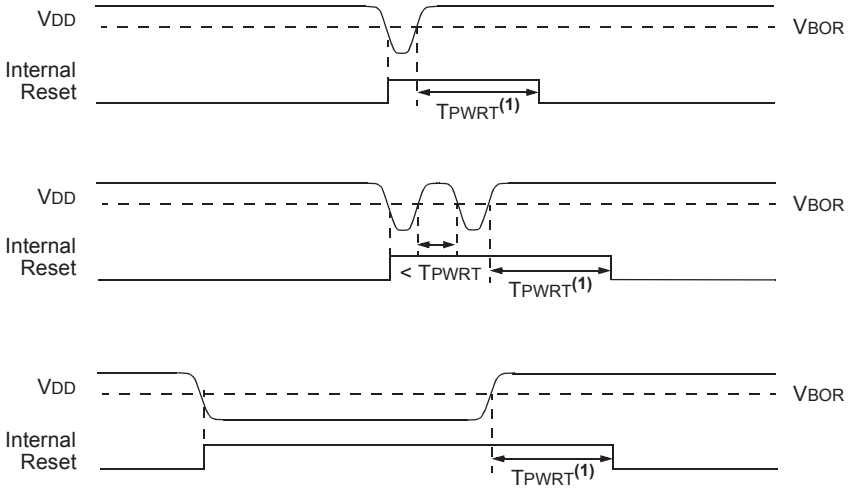
6.2.3 BOR CONTROLLED BY SOFTWARE

When the BORENx bits of the Configuration Words are programmed to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

FIGURE 6-2: BROWN-OUT SITUATIONS



Note 1: TPWRT delay only if the $\overline{\text{PWRTE}}$ bit is programmed to '0'.

REGISTER 11-13: WPUB: WEAK PULL-UP PORTB REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
WPUB<7:4>(1,2)				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **WPUB<7:4>**: Weak Pull-up PORTB Register bits(1,2)
1 = Pull-up is enabled
0 = Pull-up is disabled

bit 3-0 **Unimplemented:** Read as '0'

Note 1: The global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 11-14: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
ODB<7:4>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **ODB<7:4>:** PORTB Open-Drain Enable bits
For RB<7:4> Pins:
1 = Port pin operates as an open-drain drive (sink current only)
0 = Port pin operates as a standard push-pull drive (source and sink current)

bit 3-0 **Unimplemented:** Read as '0'

11.5 PORTC Registers

11.5.1 DATA REGISTER

PORTC is a 6-bit wide bidirectional port in the PIC16(L)F1764/5 devices and 8-bit wide bidirectional port in the PIC16(L)F1768/9 devices. The corresponding Data Direction register is TRISC (Register 11-18). Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 11-1 shows how to initialize an I/O port.

Reading the PORTC register (Register 11-17) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are Read-Modify-Write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORTC Data Latch (LATC).

11.5.2 DIRECTION CONTROL

The TRISC register (Register 11-18) controls the PORTC pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISC register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

11.5.3 INPUT THRESHOLD CONTROL

The INLVLC register (Register 11-24) controls the input voltage threshold for each of the available PORTC input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTC register and also the level at which an Interrupt-On-Change occurs, if that feature is enabled. See Table 36-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

11.5.4 OPEN-DRAIN CONTROL

The ODCONC register (Register 11-22) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONC bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONC bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

11.5.5 SLEW RATE CONTROL

The SLRCONC register (Register 11-23) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONC bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONC bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

11.5.6 ANALOG CONTROL

The ANSELC register (Register 11-20) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELC bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELC bits has no effect on digital output functions. A pin with TRISx clear and ANSELC set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing Read-Modify-Write instructions on the affected port.

Note:	The ANSELC bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSELx bits must be initialized to '0' by user software.

11.5.7 PORTC FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the Peripheral Pin Select logic. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as ADC and comparator inputs, are not shown in the Peripheral Pin Select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELC register. Digital output functions may continue to control the pin when it is in Analog mode.

11.5.8 HIGH-CURRENT DRIVE CONTROL

The output drivers on RC4 and RC5 are capable of sourcing and sinking up to 100 mA. This extra drive capacity can be enabled and disabled with the control bits in the HIDRVC register (Register 11-25).

24.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for all CCP modules.

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to 10 bits of resolution. The period, duty cycle and resolution are controlled by the following registers:

- T2PR/T4PR/T6PR registers
- T2CON/T4CON/T6CON registers
- CCPRxH:CCPRxL register pair

Figure 24-3 shows a simplified block diagram of PWM operation.

Note 1:	The corresponding TRISx bit must be cleared to enable the PWM output on the CCPx pin.
2:	Clearing the CCPxCON register will relinquish control of the CCPx pin.

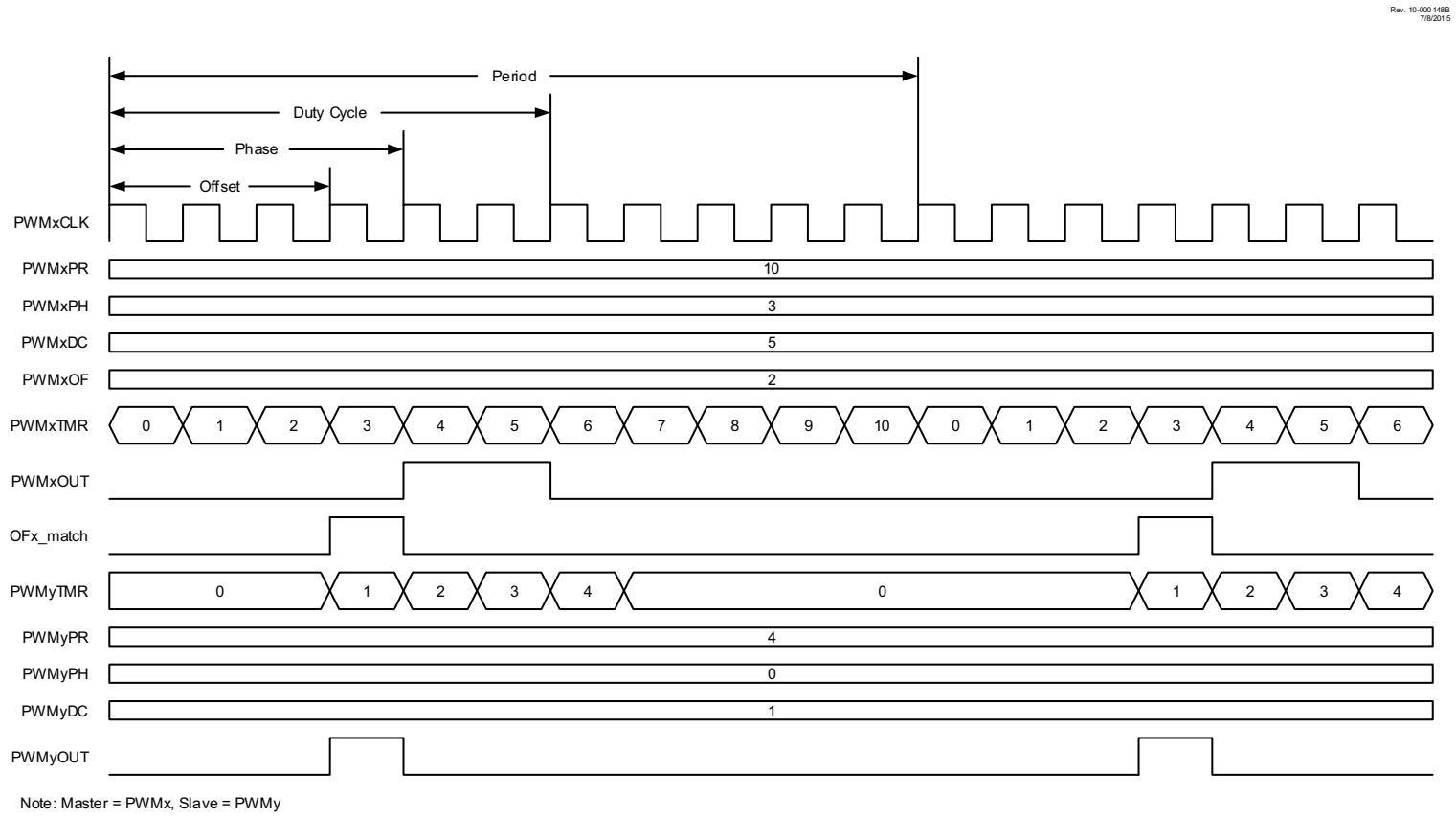
24.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Disable the CCPx pin output driver by setting the associated TRISx bit.
2. Select the timer associated with the PWM by setting the CCPTMRS register.
3. Load the associated T2PR/T4PR/T6PR register with the PWM period value.
4. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
5. Load the CCPRxH:CCPRxL register pair with the PWM duty cycle value.
6. Configure and start the timer selected in Step 2:
   - Clear the timer interrupt flag bit of the PIRx register. See Note below.
   - Configure the CKPSx bits of the TxCON register with the timer prescale value.
   - Enable the timer by setting the ON bit of the TxCON register.
7. Enable PWM output pin:
   - Wait until the timer overflows and the timer interrupt bit of the PIRx register is set. See Note below.
   - Enable the CCPx pin output driver by clearing the associated TRISx bit.

Note:	In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then Step 6 may be ignored.

FIGURE 26-10: ONE-SHOT SLAVE RUN MODE WITH SYNC START TIMING DIAGRAM



26.4 Reload Operation

Four of the PWM module control register pairs and one control bit are double-buffered so that all can be updated simultaneously. These include:

- PWMxPHH:PWMxPHL register pair
- PWMxDCH:PWMxDCL register pair
- PWMxPRH:PWMxPRL register pair
- PWMxOFH:PWMxOFL register pair
- ODO control bit

When written to, these registers do not immediately affect the operation of the PWM. By default, writes to these registers will not be loaded into the PWM operating buffer registers until after the arming conditions are met. The arming control has two methods of operation:

- Immediate
- Triggered

The LDT bit of the PWMxLDCON register controls the arming method. Both methods require the LDA bit to be set. All four buffer pairs will load simultaneously at the loading event.

26.4.1 IMMEDIATE RELOAD

When the LDT bit is clear, then the Immediate mode is selected and the buffers will be loaded at the first period event after the LDA bit is set. Immediate reloading is used when a PWM module is operating stand-alone or when the PWM module is operating as a master to other slave PWM modules.

26.4.2 TRIGGERED RELOAD

When the LDT bit is set, then the Triggered mode is selected and a trigger event is required for the LDA bit to take effect. The trigger source is the buffer load event of one of the other PWM modules in the device. The triggering source is selected by the LDS bit of the PWMxLDCON register. The buffers will be loaded at the first period event following the trigger event. Triggered reloading is used when a PWM module is operating as a slave to another PWM and it is necessary to synchronize the buffer reloads in both modules.

Note 1: The buffer load operation clears the LDA bit.

2: If the LDA bit is set at the same time as PWMxTMR = PWMxPR, the LDA bit is ignored until the next period event. Such is the case when triggered reload is selected and the triggering event occurs simultaneously with the target's period event.

26.5 Operation in Sleep Mode

Each PWM module will continue to operate in Sleep mode when either the HFINTOSC or LFINTOSC is selected as the clock source by PWMxCLKCON<1:0>.

26.6 Interrupts

Each PWM module has four independent interrupts based on the phase, duty cycle, period and offset match events. The interrupt flag is set on the rising edge of each of these signals. Refer to Figures 26-12 and 26-13 for detailed timing diagrams of the match signals.

REGISTER 26-13: PWMxOFH: PWMx OFFSET COUNT HIGH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
OF<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **OF<15:8>**: PWMx Offset High bits
Upper eight bits of PWMx offset count.

REGISTER 26-14: PWMxOFL: PWMx OFFSET COUNT LOW REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
OF<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **OF<7:0>**: PWMx Offset Low bits
Lower eight bits of PWMx offset count.

REGISTER 27-3: COGxRIS0: COGx RISING EVENT INPUT SELECTION REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
RIS7	RIS6	RIS5	RIS4	RIS3	RIS2	RIS1	RIS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **RIS7:** COGx Rising Event Input Source 7 Enable bit
1 = PWM3 output is enabled as a rising event input
0 = PWM3 output has no effect on the rising event

bit 6 **RIS6:** COGx Rising Event Input Source 6 Enable bit
1 = CCP2 output is enabled as a rising event input
0 = CCP2 output has no effect on the rising event

bit 5 **RIS5:** COGx Rising Event Input Source 5 Enable bit
1 = CCP1 output is enabled as a rising event input
0 = CCP1 output has no effect on the rising event

bit 4 **RIS4:** COGx Rising Event Input Source 4 Enable bit
1 = Comparator 4 output is enabled as a rising event input
0 = Comparator 4 output has no effect on the rising event

bit 3 **RIS3:** COGx Rising Event Input Source 3 Enable bit
1 = Comparator 3 output is enabled as a rising event input
0 = Comparator 3 output has no effect on the rising event

bit 2 **RIS2:** COGx Rising Event Input Source 2 Enable bit
1 = Comparator 2 output is enabled as a rising event input
0 = Comparator 2 output has no effect on the rising event

bit 1 **RIS1:** COGx Rising Event Input Source 1 Enable bit
1 = Comparator 1 output is enabled as a rising event input
0 = Comparator 1 output has no effect on the rising event

bit 0 **RIS0:** COGx Rising Event Input Source 0 Enable bit
1 = Pin selected with COGxINPPS register is enabled as rising event input
0 = Pin selected with COGxINPPS register has no effect on the rising event

REGISTER 27-19: COGxPHF: COGx FALLING EVENT PHASE DELAY COUNT REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	PHF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **PHF<5:0>:** Falling Event Phase Delay Count Value bits
= Number of COGx clock periods to delay falling event

TABLE 27-4: SUMMARY OF REGISTERS ASSOCIATED WITH COGx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELB(1)	ANSB<7:4>				—	—	—	—	143
ANSELC	ANSC<7:6>(1)		—	—	ANSC<3:0>				148
COGxASD0	ASE	ARSEN	ASDBD<1:0>		ASDAC<1:0>		—	—	326
COGxASD1	AS7E	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E	327
COGxBLKR	—	—	BLKR<5:0>						330
COGxBLKF	—	—	BLKF<5:0>						330
COGxCON0	EN	LD	—	CS<1:0>		MD<2:0>			312
COGxCON1	RDBS	FDBS	—	—	POLD	POLC	POLB	POLA	313
COGxDBR	—	—	DBR<5:0>						329
COGxDBF	—	—	DBF<5:0>						329
COGxFIS0	FIS7	FIS6	FIS5	FIS4	FIS3	FIS2	FIS1	FIS0	320
COGxFIS1	FIS15(1)	FIS14	FIS13	FIS12	FIS11	FIS10	FIS9	FIS8	321
COGxFSIM0	FSIM7	FSIM6	FSIM5	FSIM4	FSIM3	FSIM2	FSIM1	FSIM0	322
COGxFSIM1	FSIM15(1)	FSIM14	FSIM13	FSIM12	FSIM11	FSIM10	FSIM9	FSIM8	324
COGxPHR	—	—	PHR<5:0>						330
COGxPHF	—	—	PHF<5:0>						331
COGxPPS	—	—	—	COG1PPS<4:0>					154, 156
COGxRIS0	RIS7	RIS6	RIS5	RIS4	RIS3	RIS2	RIS1	RIS0	314
COGxRIS1	RIS15(1)	RIS14	RIS13	RIS12	RIS11	RIS10	RIS9	RIS8	315
COGxRSIM0	RSIM7	RSIM6	RSIM5	RSIM4	RSIM3	RSIM2	RSIM1	RSIM0	316
COGxRSIM1	RSIM15(1)	RSIM14	RSIM13	RSIM12	RSIM11	RSIM10	RSIM9	RSIM8	318
COGxSTR	SDATD	SDATC	SDATB	SDATA	STRD	STRC	STRB	STRA	328
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
RxyPPS	—	—	—	RxyPPS<4:0>					154

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by COG.

Note 1: PIC16(L)F1768/9 only.

30.0 PROGRAMMABLE RAMP GENERATOR (PRG) MODULE

The Programmable Ramp Generator (PRG) module is designed to provide rising and falling linear ramps. Typical applications include slope compensation for fixed frequency, continuous current and Current mode switched power supplies. Slope compensation is a necessary feature of these power supplies because it prevents frequency instabilities at duty cycles greater than 50%.

The PRG has the following features:

- Linear positive and negative voltage ramp outputs
- Programmable current source/sink
- Internal and external reference voltage selection
- Internal and external timing source selection

A simplified block diagram of the PRG is shown in Figure 30-1.

30.1 Fundamental Operation

The PRG can be operated in three voltage ramp generator modes:

- Falling Voltage (slope compensation)
- Rising Voltage
- Alternating Rising and Falling Voltage

In the Rising or Falling mode, an internal capacitor is discharged when the set_falling timing input is true and charged by an internally generated constant current when the set_rising timing input is true. The resulting linear ramp starts at the selected voltage input level and resets back to that level when the ramp is terminated by the set_falling timing input. The set_falling input dominates when both timing inputs are true.

To control the operation with a single-ended source, select the same source for both the set_rising and set_falling inputs and invert the polarity of one of them with the corresponding polarity control bit.

In the Alternating mode, the capacitor is not discharged but alternates between being charged in one direction then the other.

Input selections are identical for all modes. The input voltage is supplied by any of the following:

- The PRGxIN0 or PRGxIN1 pins
- The buffered output of the internal Fixed Voltage Reference (FVR),
- Any of the internal DACs.

The timing sources are selected from the following:

- The synchronized output of any comparator
- Any PWM output
- Any I/O pin

The ramp output is available as an input to any of the comparators or op amps.

30.1.1 SLOPE COMPENSATION

Slope compensation works by quickly discharging an internal capacitor at the beginning of each PWM period. One side of the internal capacitor is connected to the voltage input source and the other side is connected to the internal current sink. The internal current sink charges this capacitor at a programmable rate. As the capacitor charges, the capacitor voltage is subtracted from the voltage source, producing a linear voltage decay at the required rate (see Figure 30-2). The ramp terminates and the capacitor is discharged when the set_falling timing input goes true. The next ramp starts when the set_rising timing input goes true.

Enabling the optional one-shot by setting the OS bit of the PRGxCON0 register ensures that the capacitor is fully discharged by overriding the set_rising timing input and holding the shorting switch closed for at least the one-shot period, typically 50 ns. Edge-sensitive timing inputs that occur during the one-shot period will be ignored. Level-sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

30.1.2 RAMP GENERATION

Ramp generation is similar to slope compensation except that the slope is either both rising and falling or just rising.

30.1.2.1 Alternating Rising/Falling Ramps

The alternating rising/falling ramp generation function works by employing the built-in current source and sink, and relying on the synchronous control of the internal analog switches and timing sources to ramp the module's output voltage up, and then subsequently, down.

Once initialized, the output voltage is ramped up linearly by the current source at a programmable rate until the set_falling timing source goes true, at which point the current source is disengaged. At the same time, the current sink is engaged to linearly ramp down the output voltage, also at a programmable rate, until the set_rising timing input goes true thereby reversing the ramp slope. The process then repeats to create a saw tooth like waveform, as shown in Figure 30-3 and Figure 30-4.

The set_rising and set_falling timing inputs can be either edge or level-sensitive, which is selected with the respective REDG and FEDG bits of the PRGxCON0 register. Edge-sensitive operation is recommended for periodic signals, such as clocks, and level-sensitive operation is recommended for analog limit triggers, such as comparator outputs.

When the one-shot is enabled (OS bit is set), then both the falling and rising ramps will persist for a minimum of the one-shot period. Edge-sensitive timing inputs that occur during the one-shot period will be ignored. Level-sensitive timing inputs that occur during, and extend beyond, the one-shot period will be suspended until the end of the one-shot time.

32.4 I²C MODE OPERATION

All MSSP I²C communication is byte-oriented and shifted out, MSb first. Six SFR registers and two interrupt flags interface the module with the PIC® microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

32.4.1 BYTE FORMAT

All communication in I²C is done in 9-bit segments. A byte is sent from a master to a slave or vice-versa, followed by an Acknowledge bit sent back. After the eighth falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an Acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

32.4.2 DEFINITION OF I²C TERMINOLOGY

There is language and terminology in the description of I²C communication that have definitions specific to I²C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Philips® I²C specification.

32.4.3 SDA AND SCL PINS

Selection of any I²C mode with the SSPEN bit set, forces the SCL and SDA pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRISx bits.

Note 1: Data is tied to output zero when an I²C mode is enabled.

2: Any device pin can be selected for SDA and SCL functions with the PPS peripheral. These functions are bidirectional. The SDA input is selected with the SSPDATPPS registers. The SCL input is selected with the SSPCLKPPS registers. Outputs are selected with the RxyPPS registers. It is the user's responsibility to make the selections so that both the input and the output for each function is on the same pin.

32.4.4 SDA HOLD TIME

The hold time of the SDA pin is selected by the SDAHT bit of the SSPxCON3 register. Hold time is the time SDA is held valid after the falling edge of SCL. Setting the SDAHT bit selects a longer 300 ns minimum hold time and may help on buses with large capacitance.

TABLE 32-2: I²C BUS TERMS

TERM	Description
Transmitter	The device which shifts data out onto the bus.
Receiver	The device which shifts data in from the bus.
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.
Slave	The device addressed by the master.
Multi-master	A bus with more than one device that can initiate data transfers.
Arbitration	Procedure to ensure that only one master at a time controls the bus. Winning arbitration ensures that the message is not corrupted.
Synchronization	Procedure to synchronize the clocks of two or more devices on the bus.
Idle	No master is controlling the bus, and both SDA and SCL lines are high.
Active	Any time one or more master devices is controlling the bus.
Addressed Slave	Slave device that has received a matching address and is actively being clocked by a master.
Matching Address	Address byte that is clocked into a slave that matches the value stored in SSPxADD.
Write Request	Slave receives a matching address with R/$\overline{W}$ bit clear and is ready to clock in data.
Read Request	Master sends an address byte with the R/$\overline{W}$ bit set, indicating that it wishes to clock data out of the slave. This data is the next and all following bytes until a Restart or Stop.
Clock Stretching	When a device on the bus hold SCL low to stall communication.
Bus Collision	Any time the SDA line is sampled low by the module while it is outputting and expected high state.

33.4.1 AUTO-BAUD DETECT

The EUSART module supports automatic detection and calibration of the baud rate.

In the Auto-Baud Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. The Baud Rate Generator is used to time the period of a received 55h (ASCII "U"), which is the Sync character for the LIN bus. The unique feature of this character is that it has five rising edges including the Stop bit edge.

Setting the ABDEN bit of the BAUDxCON register starts the auto-baud calibration sequence. While the ABD sequence takes place, the EUSART state machine is held in Idle. On the first rising edge of the receive line, after the Start bit, the SPxBRG begins counting up using the BRG counter clock, as shown in Figure 33-6. The fifth rising edge will occur on the RX pin at the end of the eighth bit period. At that time, an accumulated value totaling the proper BRG period is left in the SPxBRGH, SPxBRGL register pair, the ABDEN bit is automatically cleared and the RCIF interrupt flag is set. The value in the RCxREG needs to be read to clear the RCIF interrupt. RCxREG content should be discarded. When calibrating for modes that do not use the SPxBRGH register, the user can verify that the SPxBRGL register did not overflow by checking for 00h in the SPxBRGH register.

The BRG auto-baud clock is determined by the BRG16 and BRGH bits as shown in Table 33-6. During ABD, both the SPxBRGH and SPxBRGL registers are used as a 16-bit counter, independent of the BRG16 bit setting. While calibrating the baud rate period, the SPxBRGH and SPxBRGL registers are clocked at 1/8th the BRG base clock rate. The resulting byte measurement is the average bit time when clocked at full speed.

Note 1: If the WUE bit is set with the ABDEN bit, Auto-Baud Detection will occur on the byte following the Break character (see **Section 33.4.3 "Auto-Wake-up on Break"**).

2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.

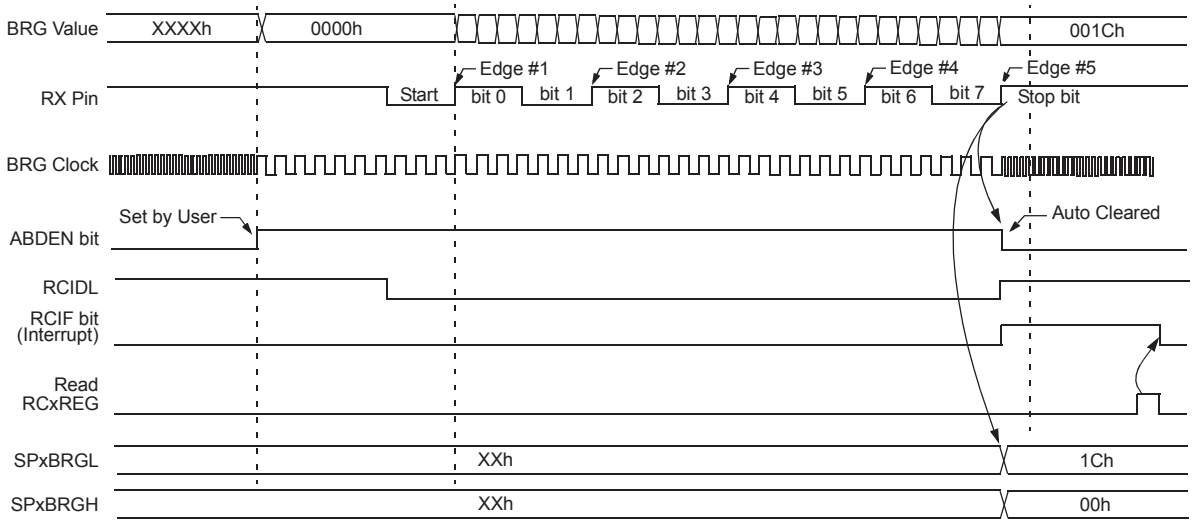
3: During the auto-baud process, the auto-baud counter starts counting at one. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPxBRGH:SPxBRGL register pair.

TABLE 33-6: BRG COUNTER CLOCK RATES

BRG16	BRGH	BRG Base Clock	BRG ABD Clock
0	0	FOSC/64	FOSC/512
0	1	FOSC/16	FOSC/128
1	0	FOSC/16	FOSC/128
1	1	FOSC/4	FOSC/32

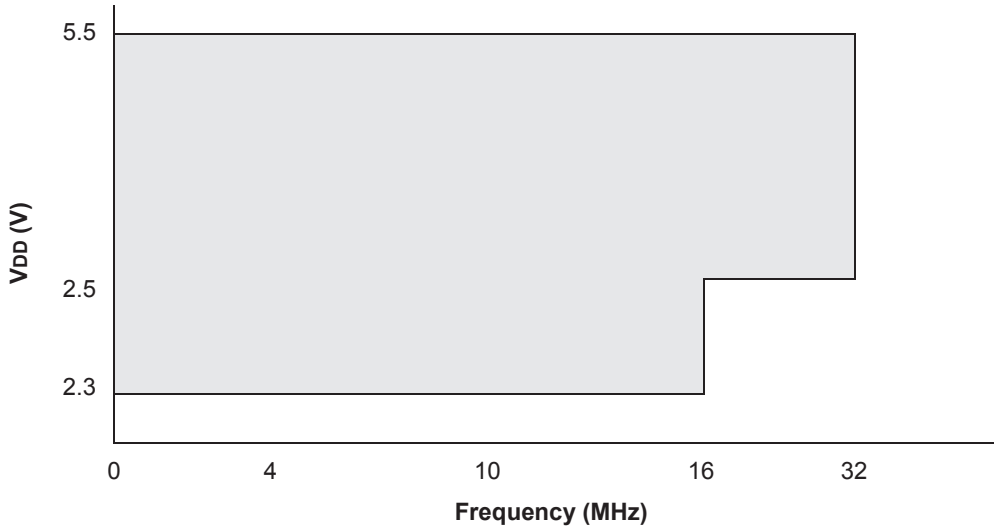
Note: During the ABD sequence, the SPxBRGL and SPxBRGH registers are both used as a 16-bit counter, independent of the BRG16 setting.

FIGURE 33-6: AUTOMATIC BAUD RATE CALIBRATION



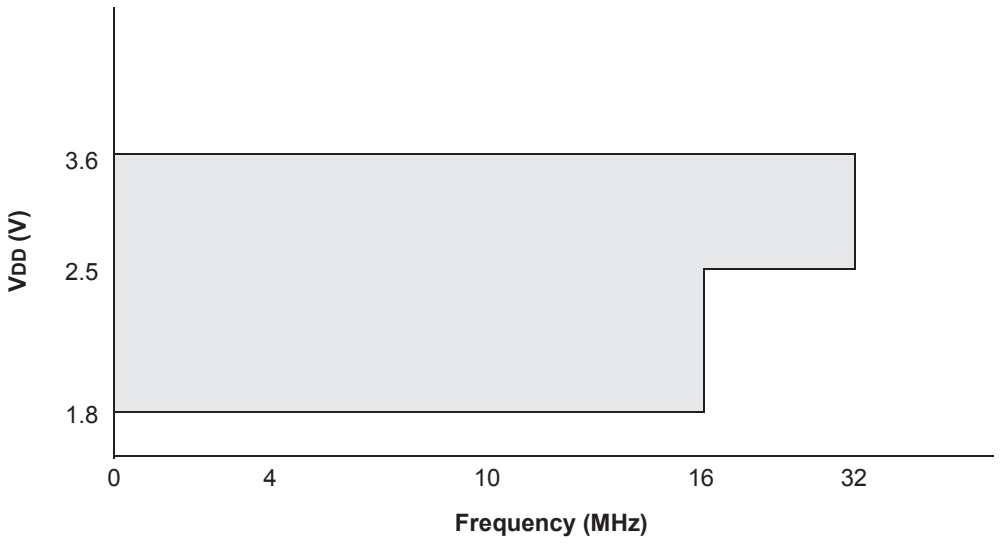
Note 1: The ABD sequence requires the **EUSART** module to be configured in Asynchronous mode.

FIGURE 36-1: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16F1764/5/8/9 ONLY



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 36-7 for each Oscillator mode's supported frequencies.

FIGURE 36-2: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C, PIC16LF1764/5/8/9 ONLY



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 36-7 for each Oscillator mode's supported frequencies.

TABLE 36-20: 10-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions (unless otherwise stated)
V_{DD} = 3.0V, T_A = +25°C
See **Section 37.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.

Param No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
DAC01*	C_{LSB}	Step-Size	—	$V_{DD}/1024$	—	V	
DAC02	C_{INL}	Integral Error(2)	—	—	±1.5	LSb	For codes: 0x004 to 0x3FB
DAC03	C_{DNL}	Differential Error(2)	—	—	±1	LSb	
DAC04	C_{OFF}	Offset Error(2)	—	—	±3	LSb	
DAC05	C_{GN}	Gain Error(2)	—	—	±3	LSb	
DAC06*	C_R	Unit Resistor Value (R)	—	300	—	Ω	
DAC07*	C_{ST}	Settling Time(1)	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while DACR<9:0> transitions from 0x000 to 0x3FF.

2: Buffered by op amp in unity gain.

TABLE 36-21: 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions (unless otherwise stated)
V_{DD} = 3.0V, T_A = +25°C
See **Section 37.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.

Param No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
DAC10*	C_{LSB}	Step-Size	—	$V_{DD}/32$	—	V	
DAC11	C_{ACC}	Absolute Accuracy(2)	—	—	±0.5	LSb	
DAC12*	C_R	Unit Resistor Value (R)	—	6000	—	Ω	
DAC13*	C_{ST}	Settling Time(1)	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while DACR<4:0> transitions from 0x00 to 0x1F.

2: Buffered by op amp in unity gain.

TABLE 36-22: ZERO-CROSS PIN SPECIFICATIONS

Operating Conditions (unless otherwise stated)
V_{DD} = 3.0V, T_A = +25°C

Param. No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
ZC01	Z_{CPINV}	Voltage on Zero-Cross Pin	—	0.75	—	V	
ZC02	Z_{CDRV}	Maximum Source or Sink Current	—	—	600	µA	
ZC04	Z_{CISW}	Response Time Rising Edge	—	1	—	µs	
		Response Time Falling Edge	—	1	—	µs	
ZC05	Z_{COUT}	Response Time Rising Edge	—	1	—	µs	
		Response Time Falling Edge	—	1	—	µs	

* These parameters are characterized but not tested.