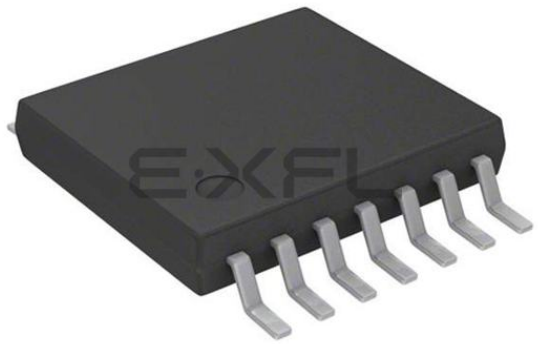

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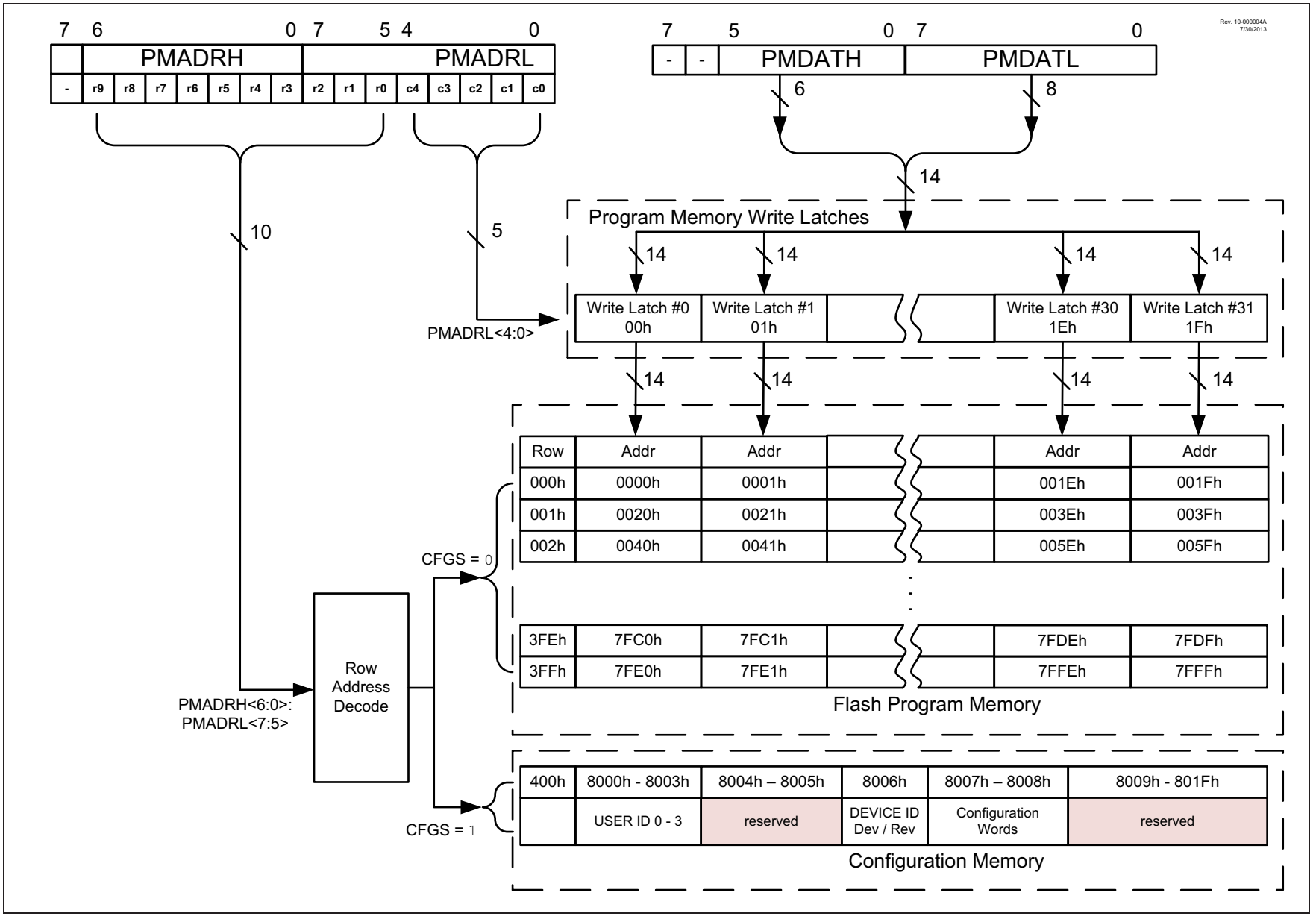
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	12
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 8x10b; D/A 1x5b, 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1765t-i-st

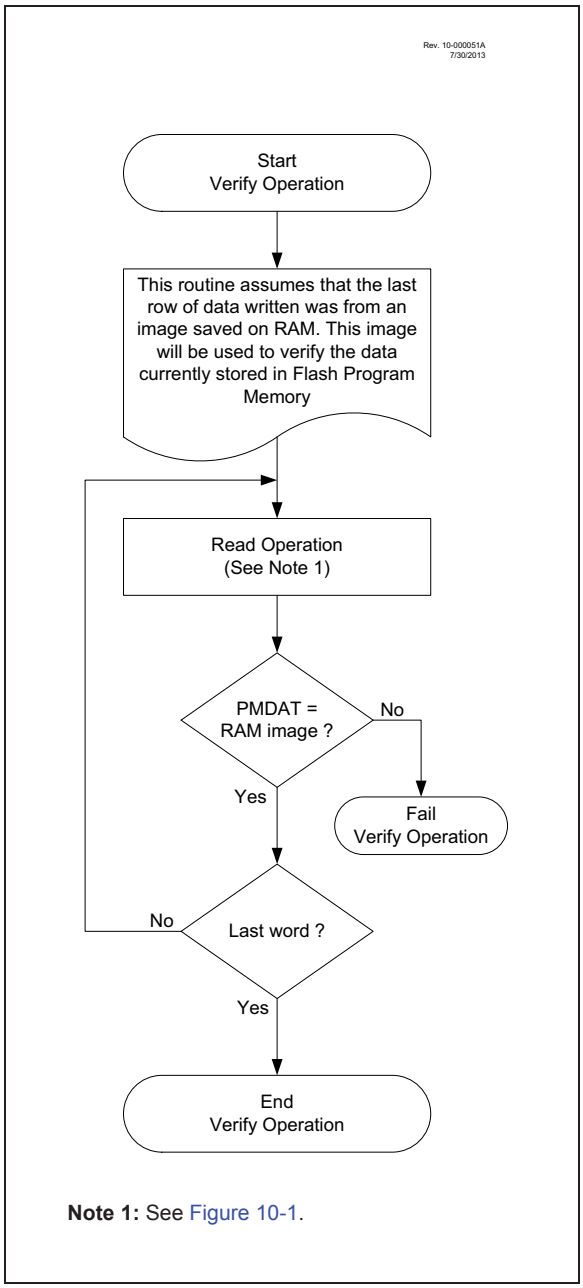
FIGURE 10-5: BLOCK WRITES TO FLASH PROGRAM MEMORY WITH 32 WRITE LATCHES



10.5 Write/Verify

It is considered good programming practice to verify that program memory writes agree with the intended value. Since program memory is stored as a full page then the stored program memory contents are compared with the intended data stored in RAM after the last write is complete.

FIGURE 10-8: FLASH PROGRAM MEMORY VERIFY FLOWCHART



Note 1: See Figure 10-1.

11.2 Register Definitions: PORTA

REGISTER 11-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x/x	R/W-x/x	R-x/x	R/W-x/x	R/W-x/x	R/W-x/x
—	—	RA<5:0>(1)					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RA<5:0>**: PORTA I/O Value bits(1)

1 = Port pin is ≥ VIH

0 = Port pin is ≤ VIL

Note 1: Writes to PORTA are actually written to the corresponding LATA register. Reads from PORTA are the return of actual I/O pin values.

REGISTER 11-2: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	U-1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	TRISA<5:4>		—(1)	TRISA<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **TRISA<5:4>:** PORTA Tri-State Control bit

1 = PORTA pin is configured as an input (tri-stated)

0 = PORTA pin is configured as an output

bit 3 **Unimplemented:** Read as '1'(1)

bit 2-0 **TRISA<2:0>:** PORTA Tri-State Control bit

1 = PORTA pin is configured as an input (tri-stated)

0 = PORTA pin is configured as an output

Note 1: Unimplemented, read as '1'.

11.3 PORTB Registers (PIC16(L)F1768/9 only)

11.3.1 DATA REGISTER

PORTB is a 4-bit wide, bidirectional port. The corresponding Data Direction register is TRISB (Register 11-10). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enable the output driver and put the contents of the output latch on the selected pin). Example 11-1 shows how to initialize an I/O port.

Reading the PORTB register (Register 11-9) reads the status of the pins, whereas writing to it, will write to the PORT latch. All write operations are Read-Modify-Write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORTB Data Latch (LATB).

11.3.2 DIRECTION CONTROL

The TRISB register (Register 11-10) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

11.3.3 OPEN-DRAIN CONTROL

The ODCONB register (Register 11-14) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONB bit is set, the corresponding port output becomes an open-drain driver, capable of sinking current only. When an ODCONB bit is cleared, the corresponding port output pin is the standard push-pull drive, capable of sourcing and sinking current.

11.3.4 SLEW RATE CONTROL

The SLRCONB register (Register 11-15) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONB bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONB bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

11.3.5 INPUT THRESHOLD CONTROL

The INLVLB register (Register 11-16) controls the input voltage threshold for each of the available PORTB input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTB register and also the level at which an Interrupt-On-Change occurs, if that feature is enabled. See Table 36-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

11.3.6 ANALOG CONTROL

The ANSELB register (Register 11-12) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

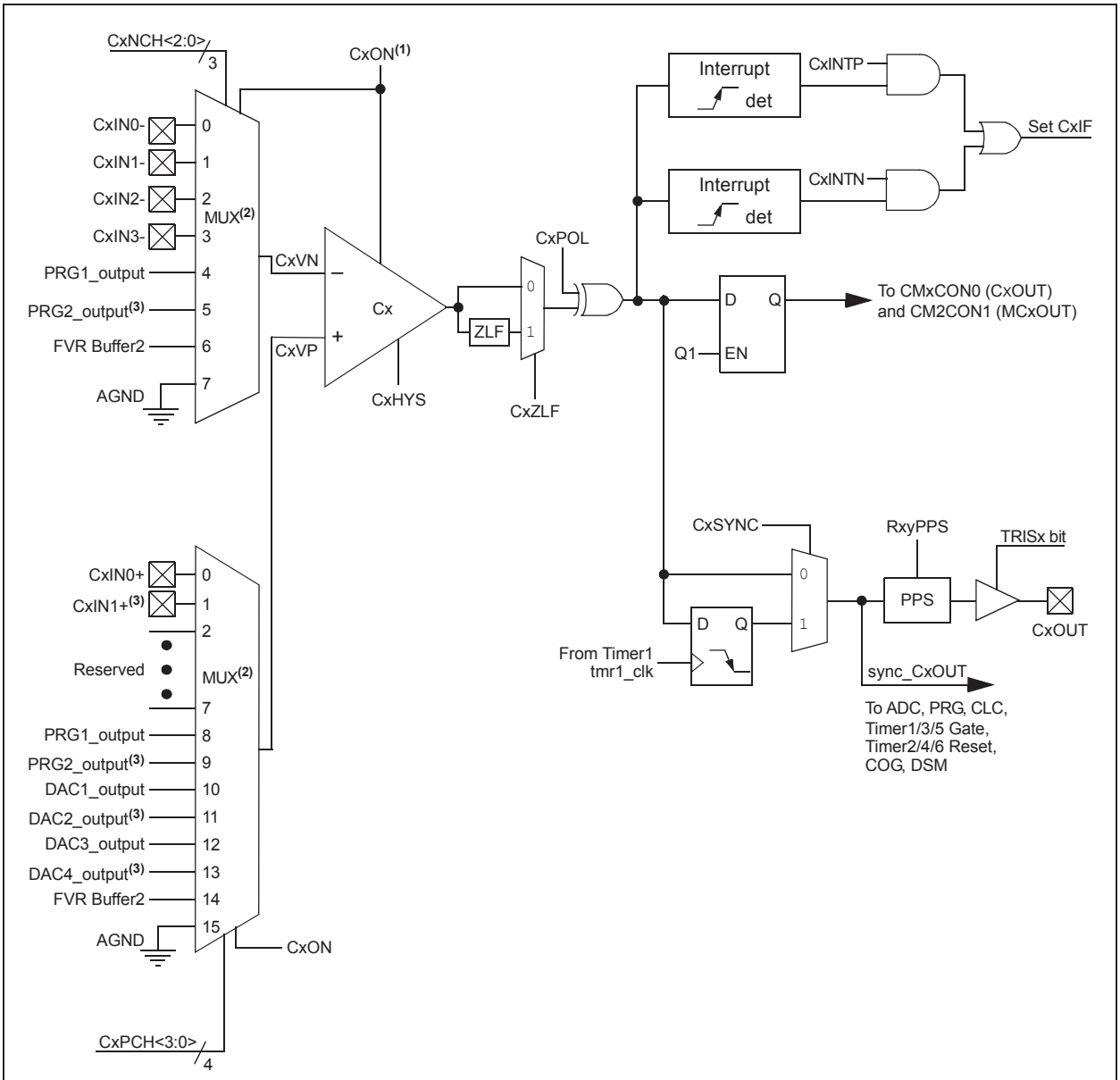
The state of the ANSELB bits has no effect on digital output functions. A pin with TRIS clear and the ANSELB bit set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing Read-Modify-Write instructions on the affected port.

Note:	The ANSELB bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSELx bits must be initialized to '0' by user software.

11.3.7 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the Peripheral Pin Select logic. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more information. Analog input functions, such as ADC and op amp inputs, are not shown in the Peripheral Pin Select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELB register. Digital output functions may continue to control the pin when it is in Analog mode.

FIGURE 19-2: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM



Note 1: When CxON = 0, the comparator will produce a '0' at the output.
2: When CxON = 0, all multiplexer inputs are disconnected.
3: Only on PIC16(L)F1768/9

20.9 Register Definitions: ZCD Control

Long bit name prefixes for the Zero-Cross Detect peripheral are shown in Table 20-1. Refer to **Section 1.1.2.2 "Long Bit Names"** for more information

TABLE 20-1: BIT NAME PREFIXES

Peripheral	Bit Name Prefix
ZCD1	ZCD1

REGISTER 20-1: ZCDxCON: ZERO-CROSS DETECTION x CONTROL REGISTER

R/W-0/0	U-0	R-x/x	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
EN(1)	—	OUT	POL	—	—	INTP	INTN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7 **EN:** Zero-Cross Detection Enable bit(1)
1 = Zero-Cross Detect is enabled; ZCD pin is forced to output to source and sink current
0 = Zero-Cross Detect is disabled; ZCD pin operates according to PPS and TRISx controls

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Zero-Cross Detection Logic Level bit
POL bit = 0:
1 = ZCD pin is sinking current
0 = ZCD pin is sourcing current
POL bit = 1:
1 = ZCD pin is sourcing current
0 = ZCD pin is sinking current

bit 4 **POL:** Zero-Cross Detection Logic Output Polarity bit
1 = ZCD logic output is inverted
0 = ZCD logic output is not inverted

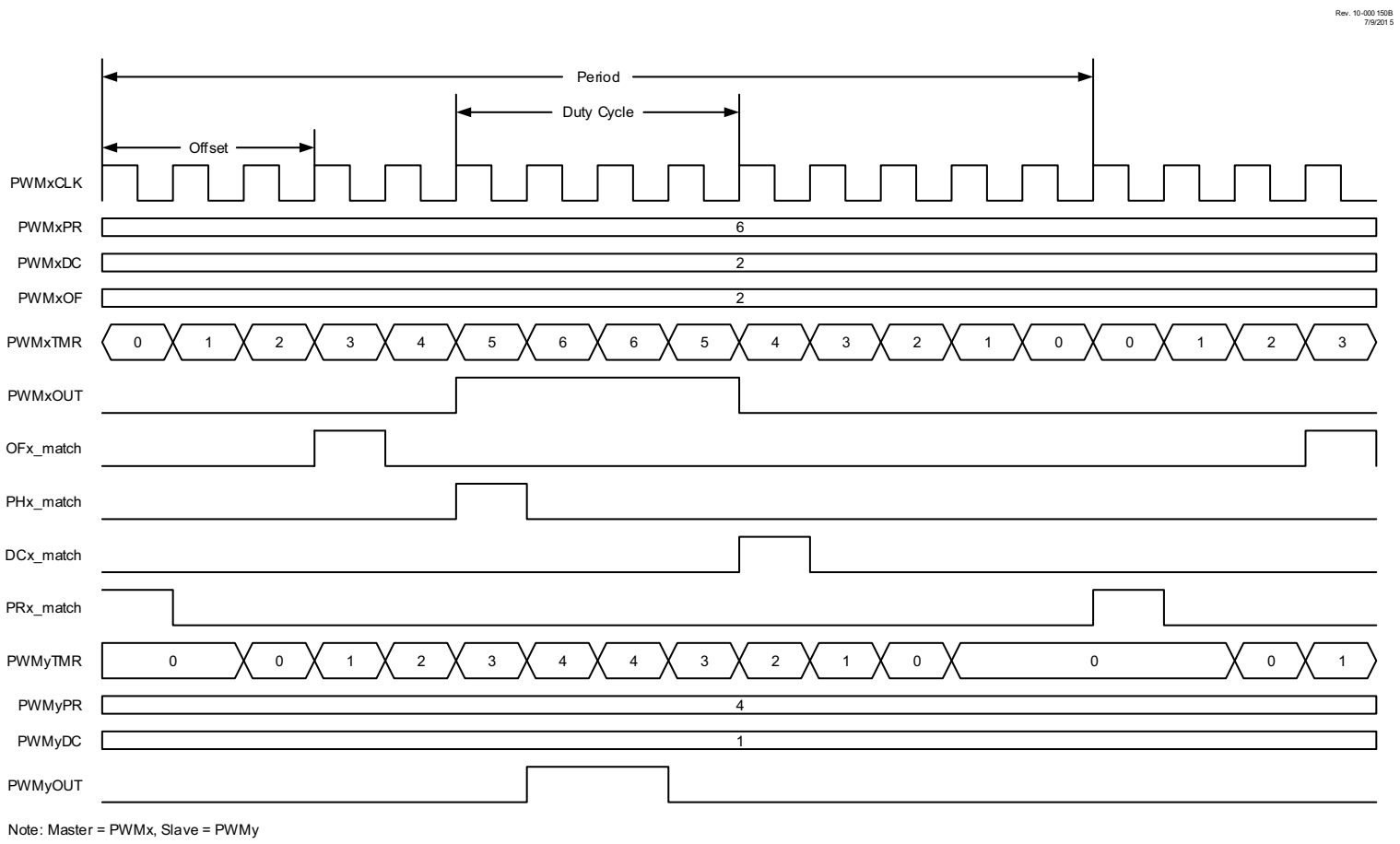
bit 3-2 **Unimplemented:** Read as '0'

bit 1 **INTP:** Zero-Cross Positive Edge Interrupt Enable bit
1 = ZCDIF bit is set on low-to-high OUT transition
0 = ZCDIF bit is unaffected by low-to-high OUT transition

bit 0 **INTN:** Zero-Cross Negative Edge Interrupt Enable bit
1 = ZCDIF bit is set on high-to-low OUT transition
0 = ZCDIF bit is unaffected by high-to-low OUT transition

Note 1: The EN bit has no effect when the $\overline{\text{ZCD}}$ Configuration bit is cleared.

FIGURE 26-12: OFFSET MATCH ON INCREMENTING TIMER TIMING DIAGRAM



REGISTER 27-4: COGxRIS1: COGx RISING EVENT INPUT SELECTION REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
RIS15(1)	RIS14	RIS13	RIS12	RIS11	RIS10	RIS9	RIS8
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **RIS15:** COGx Rising Event Input Source 15 Enable bit(1)
- 1 = DSM2 MD2_out is enabled as a rising event input
- 0 = DSM2 MD2_out has no effect on the rising event

bit 6 **RIS14:** COGx Rising Event Input Source 14 Enable bit
- 1 = DSM1 MD1_out output is enabled as a rising event input
- 0 = DSM1 MD1_out has no effect on the rising event

bit 5 **RIS13:** COGx Rising Event Input Source 13 Enable bit
- 1 = CLC3 output is enabled as a rising event input
- 0 = CLC3 output has no effect on the rising event

bit 4 **RIS12:** COGx Rising Event Input Source 12 Enable bit
- 1 = CLC2 output is enabled as a rising event input
- 0 = CLC2 output has no effect on the rising event

bit 3 **RIS11:** COGx Rising Event Input Source 11 Enable bit
- 1 = CLC1 output is enabled as a rising event input
- 0 = CLC1 output has no effect on the rising event

bit 2 **RIS10:** COGx Rising Event Input Source 10 Enable bit
- 1 = PWM6 output is enabled as a rising event input
- 0 = PWM6 output has no effect on the rising event

bit 1 **RIS9:** COGx Rising Event Input Source 9 Enable bit
- 1 = PWM5 output is enabled as a rising event input
- 0 = PWM5 output has no effect on the rising event

bit 0 **RIS8:** COGx Rising Event Input Source 8 Enable bit
- 1 = PWM4 output is enabled as rising event input
- 0 = PWM4 output has no effect on the rising event

Note 1: PIC16(L)F1768/9 only. Otherwise unimplemented, read as '0'.

REGISTER 27-5: COGxRSIM0: COGx RISING EVENT SOURCE INPUT MODE REGISTER 0 (CONTINUED)

bit 1 **RSIM1:** COGx Rising Event Input Source 1 Mode bit

RIS1 = 1:

1 = Comparator 1 low-to-high transition will cause a rising event after rising event phase delay
0 = Comparator 1 high level will cause an immediate rising event

RIS1 = 0:

Comparator 1 has no effect on rising event.

bit 0 **RSIM0:** COGx Rising Event Input Source 0 Mode bit

RIS0 = 1:

1 = Pin selected with COGxINPPS register low-to-high transition will cause a rising event after rising event phase delay
0 = Pin selected with COGxINPPS register high level will cause an immediate rising event

RIS0 = 0:

Pin selected with COGxINPPS register has no effect on rising event.

REGISTER 27-12: COGxASD1: COGx AUTO-SHUTDOWN CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
AS7E	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7 **AS7E:** COGx Auto-shutdown Source Enable bit 7
- 1 = COGx is shutdown when Timer4_output is high
- 0 = Timer4_output has no effect on shutdown

bit 6 **AS6E:** COGx Auto-shutdown Source Enable bit 6
- 1 = COGx is shutdown when Timer2_output is high
- 0 = Timer2_output has no effect on shutdown

bit 5 **AS5E:** COGx Auto-shutdown Source Enable bit 5
- 1 = COGx is shutdown when CLC LC2_out is low
- 0 = CLC2 output has no effect on shutdown

bit 4 **AS4E:** COGx Auto-shutdown Source Enable bit 4
- 1 = COGx is shutdown when Comparator sync_C4OUT is low
- 0 = Comparator 4 output has no effect on shutdown

bit 3 **AS3E:** COGx Auto-shutdown Source Enable bit 3
- 1 = COGx is shutdown when Comparator sync_C3OUT is low
- 0 = Comparator 3 output has no effect on shutdown

bit 2 **AS2E:** COGx Auto-shutdown Source Enable bit 2
- 1 = COGx is shutdown when Comparator sync_C2OUT is low
- 0 = Comparator 2 output has no effect on shutdown

bit 1 **AS1E:** COGx Auto-shutdown Source Enable bit 1
- 1 = COGx is shutdown when comparator sync_C1OUT is low
- 0 = Comparator 1 output has no effect on shutdown

bit 0 **AS0E:** COGx Auto-shutdown Source Enable bit 0
- 1 = COGx is shutdown when pin selected with COGxINPPS register is low
- 0 = Pin selected with COGxINPPS register has no effect on shutdown

REGISTER 28-6: CLCxSEL3: GENERIC CLCx DATA 4 SELECT REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	D4S<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **D4S<5:0>:** CLCx Data 4 Input Selection bits
See Table 28-1.

REGISTER 28-7: CLCxGLS0: CLCx GATE 1 LOGIC SELECT REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **G1D4T:** Gate 1 Data 4 True (non-inverted) bit
1 = d4T is gated into g1
0 = d4T is not gated into g1

bit 6 **G1D4N:** Gate 1 Data 4 Negated (inverted) bit
1 = d4N is gated into g1
0 = d4N is not gated into g1

bit 5 **G1D3T:** Gate 1 Data 3 True (non-inverted) bit
1 = d3T is gated into g1
0 = d3T is not gated into g1

bit 4 **G1D3N:** Gate 1 Data 3 Negated (inverted) bit
1 = d3N is gated into g1
0 = d3N is not gated into g1

bit 3 **G1D2T:** Gate 1 Data 2 True (non-inverted) bit
1 = d2T is gated into g1
0 = d2T is not gated into g1

bit 2 **G1D2N:** Gate 1 Data 2 Negated (inverted) bit
1 = d2N is gated into g1
0 = d2N is not gated into g1

bit 1 **G1D1T:** Gate 1 Data 1 True (non-inverted) bit
1 = d1T is gated into g1
0 = d1T is not gated into g1

bit 0 **G1D1N:** Gate 1 Data 1 Negated (inverted) bit
1 = d1N is gated into g1
0 = d1N is not gated into g1

31.0 DATA SIGNAL MODULATOR (DSM)

The Data Signal Modulator (DSM) is a peripheral that allows the user to mix a data stream, also known as a modulator signal, with a carrier signal to produce a modulated output.

Both the carrier and the modulator signals are supplied to the DSM module either internally, from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical “AND” operation of both the carrier and modulator signals and then provided to the MDxOUT pin.

The carrier signal is comprised of two distinct and separate signals: a Carrier High (CARH) signal and a Carrier Low (CARL) signal. During the time in which the Modulator (MOD) signal is in a logic high state, the DSM mixes the Carrier High signal with the Modulator signal. When the Modulator signal is in a logic low state, the DSM mixes the Carrier Low signal with the Modulator signal.

Using this method, the DSM can generate the following types of key modulation schemes:

- Frequency-Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Additionally, the following features are provided within the DSM module:

- Carrier Synchronization
- Carrier Source Polarity Select
- Carrier Source Pin Disable
- Programmable Modulator Data
- Modulator Source Pin Disable
- Modulated Output Polarity Select
- Slew Rate Control

Figure 31-1 shows a simplified block diagram of the Data Signal Modulator peripheral.

FIGURE 31-1: SIMPLIFIED BLOCK DIAGRAM OF THE DATA SIGNAL MODULATOR

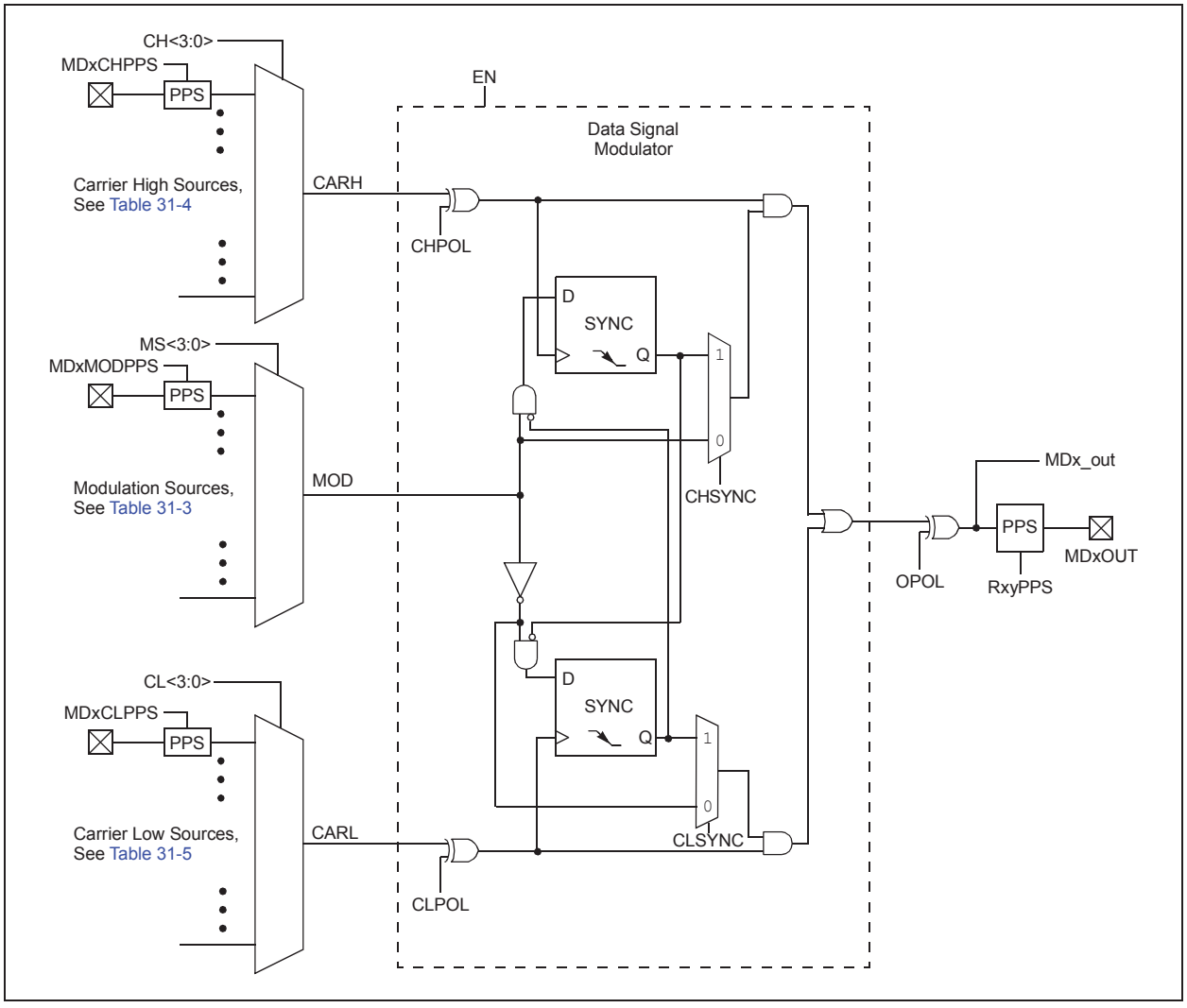


FIGURE 32-8: SLAVE SELECT SYNCHRONOUS WAVEFORM

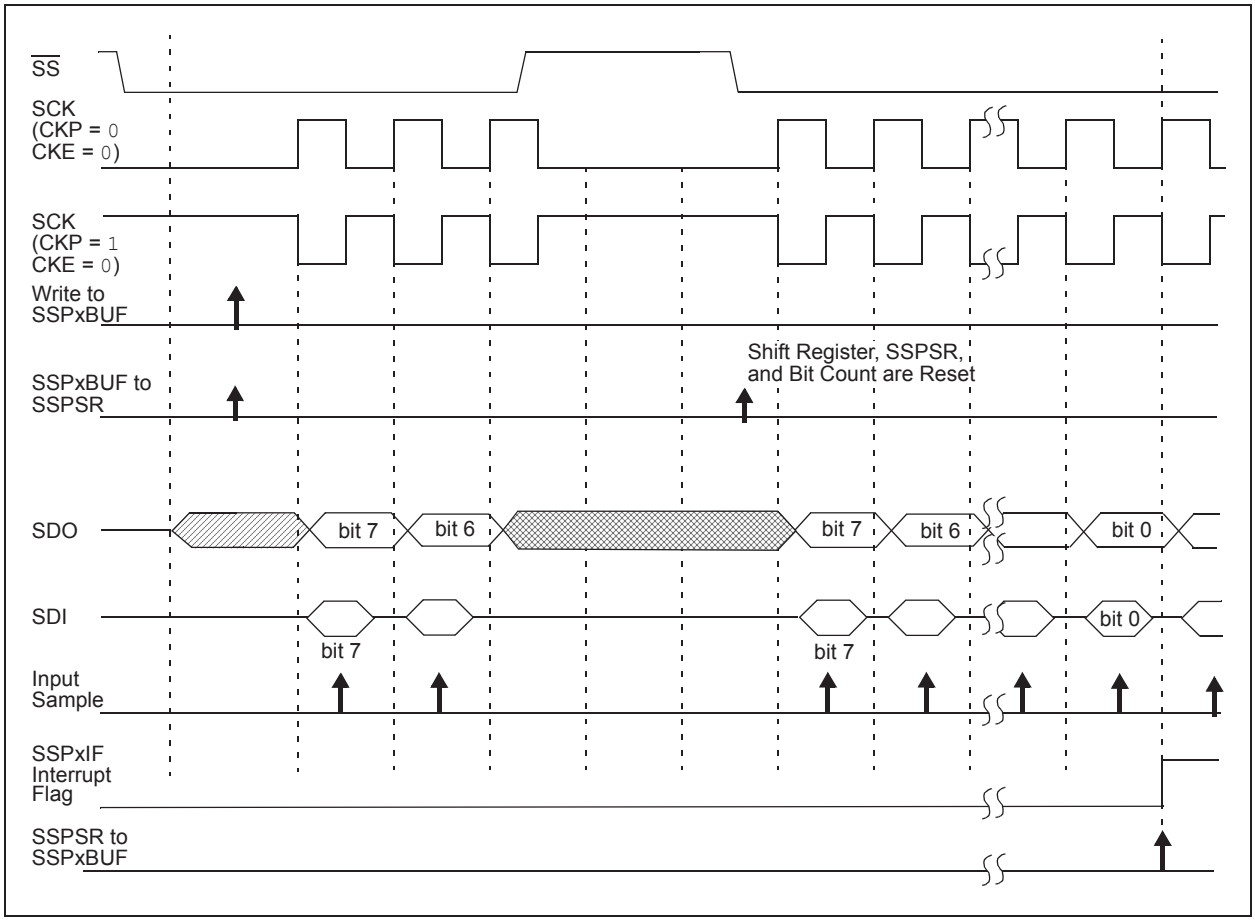
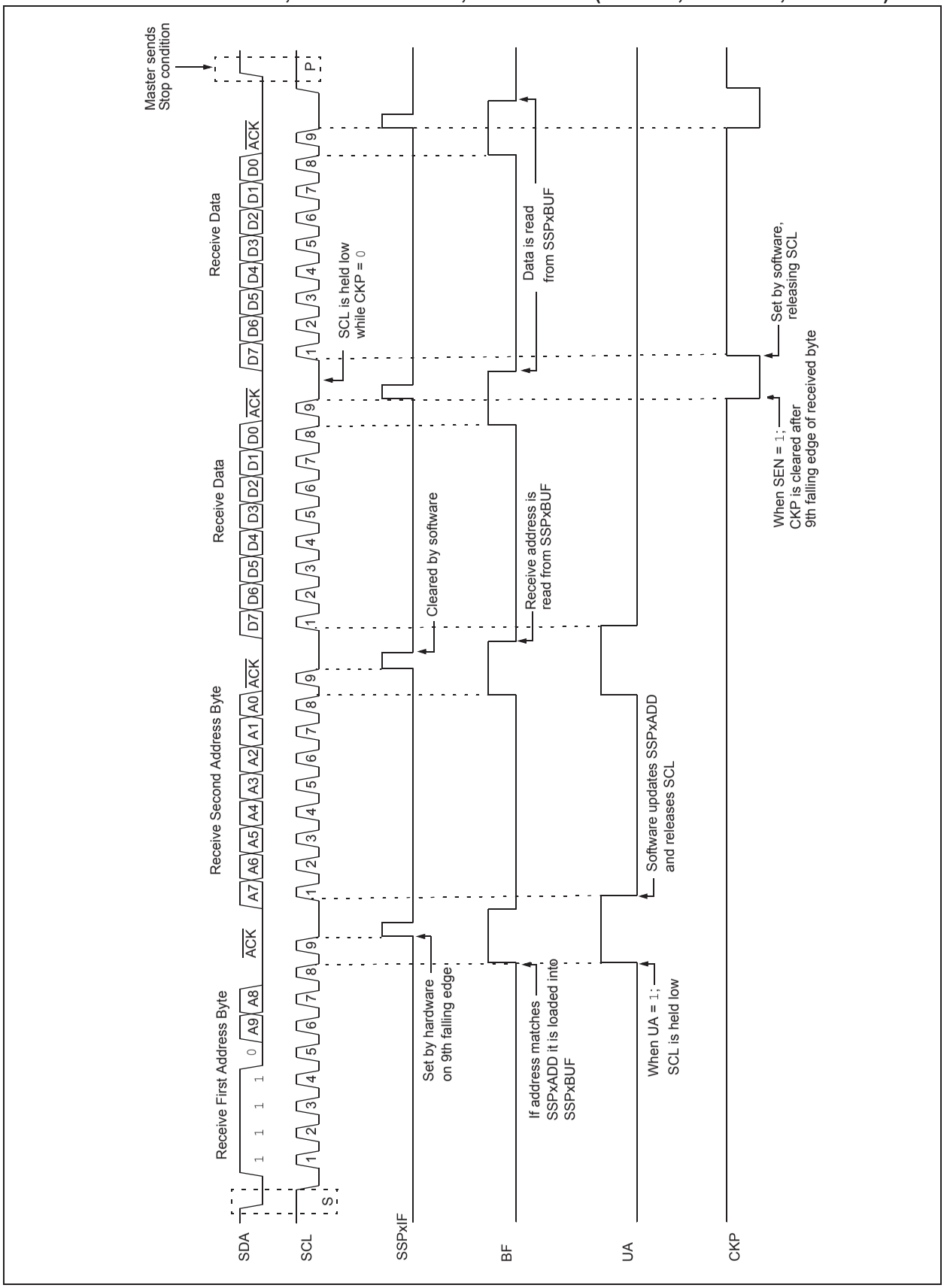


FIGURE 32-20: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)



32.7 BAUD RATE GENERATOR

The MSSP module has a Baud Rate Generator available for clock generation in both I^2C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSPxADD register (Register 32-6). When a write occurs to SSPxBUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

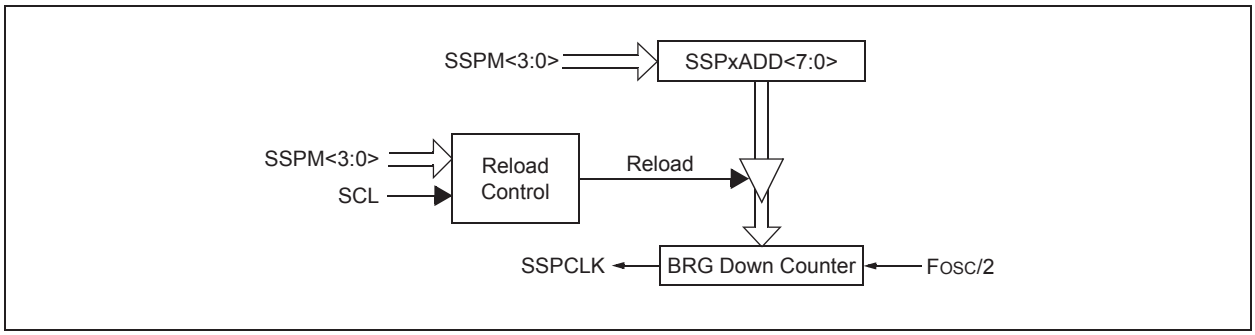
An internal signal “Reload” in Figure 32-40 triggers the value from SSPxADD to be loaded into the BRG counter. This occurs twice for each oscillation of the module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP is being operated in.

Table 32-4 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPxADD.

EQUATION 32-1:

$$F_{CLOCK} = \frac{F_{OSC}}{(SSPxADD + 1)(4)}$$

FIGURE 32-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSPxADD when used as a Baud Rate Generator for I^2C; this is an implementation limitation.

TABLE 32-4: MSSP CLOCK RATE w/BRG

FOSC	FCY	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note: Refer to the I/O port electrical specifications in Table 36-10 and Figure 36-7 to ensure the system is designed to support I/O timing requirements.

BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

BRA	Relative Branch
Syntax:	[*label*] BRA label [*label*] BRA $+k
Operands:	-256 ≤ label - PC + 1 ≤ 255 -256 ≤ k ≤ 255
Operation:	(PC) + 1 + k → PC
Status Affected:	None
Description:	Add the signed 9-bit literal 'k' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + k. This instruction is a 2-cycle instruction. This branch has a limited range.

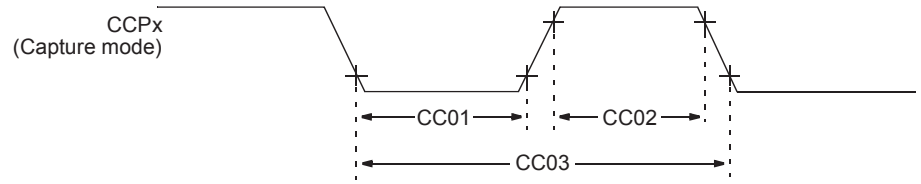
BRW	Relative Branch with W
Syntax:	[*label*] BRW
Operands:	None
Operation:	(PC) + (W) → PC
Status Affected:	None
Description:	Add the contents of W (unsigned) to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 1 + (W). This instruction is a 2-cycle instruction.

BSF	Bit Set f
Syntax:	[*label*] BSF f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	1 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

BTFSC	Bit Test f, Skip if Clear
Syntax:	[*label*] BTFSC f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b ≤ 7
Operation:	skip if (f<b>) = 0
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

BTFSS	Bit Test f, Skip if Set
Syntax:	[*label*] BTFSS f,b
Operands:	0 ≤ f ≤ 127 0 ≤ b < 7
Operation:	skip if (f<b>) = 1
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2-cycle instruction.

FIGURE 36-11: CAPTURE/COMPARE/PWM TIMINGS (CCP)



Note: Refer to Figure 36-4 for load conditions.

TABLE 36-13: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP)

Standard Operating Conditions (unless otherwise stated)								
Param No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
CC01*	TccL	CCPx Input Low Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC02*	TccH	CCPx Input High Time	No Prescaler	0.5TCY + 20	—	—	ns	
			With Prescaler	20	—	—	ns	
CC03*	TccP	CCPx Input Period		$\frac{3\ T_{CY} + 40}{N}$	—	—	ns	N = prescale value

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

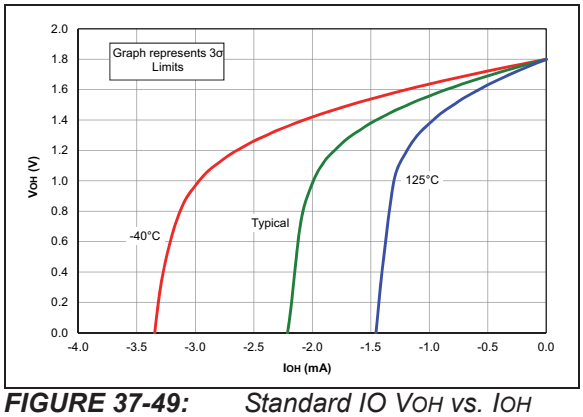


FIGURE 37-49: *Standard IO VOH vs. IOH Over Temperature, VDD = 1.8V, PIC16LF1764/5/8/9 Only.*

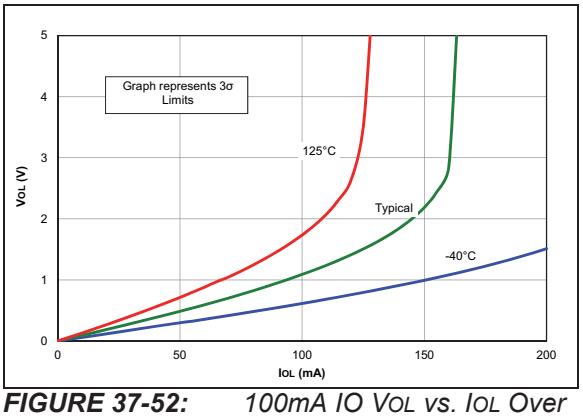


FIGURE 37-52: *100mA IO VOL vs. IOL Over Temperature, VDD = 5.5V, PIC16F1764/5/8/9 Only.*

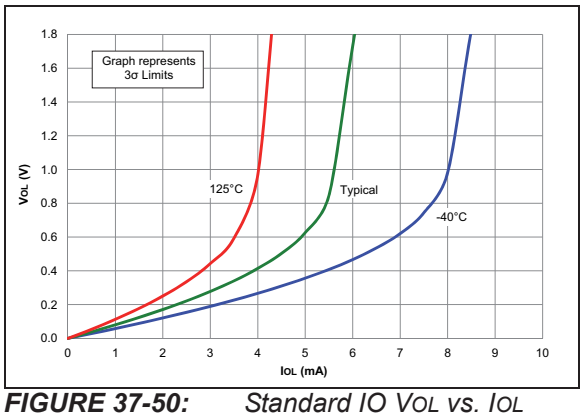


FIGURE 37-50: *Standard IO VOL vs. IOL Over Temperature, VDD = 1.8V, PIC16LF1764/5/8/9 Only.*

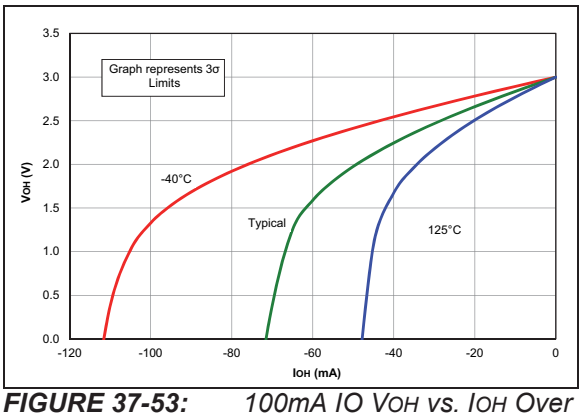


FIGURE 37-53: *100mA IO VOH vs. IOH Over Temperature, VDD = 3.0V.*

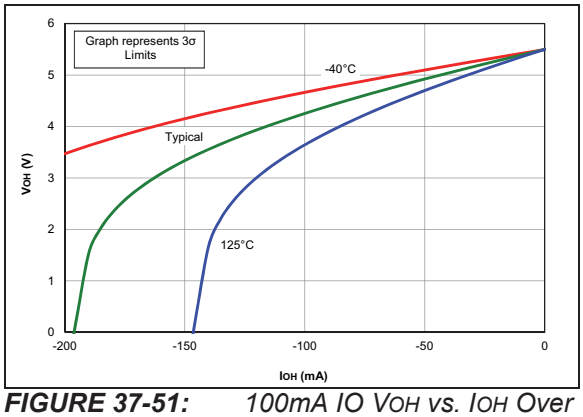


FIGURE 37-51: *100mA IO VOH vs. IOH Over Temperature, VDD = 5.5V, PIC16F1764/5/8/9 Only.*

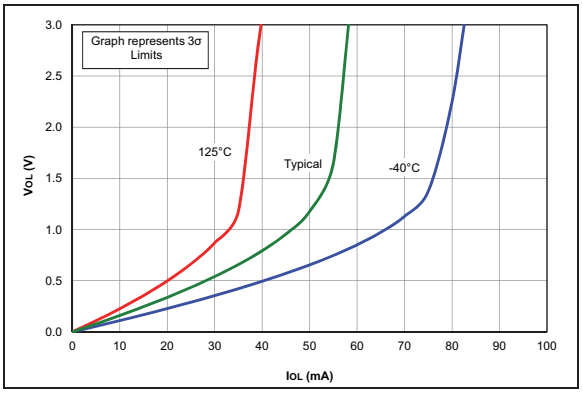


FIGURE 37-54: *VOL vs. IOL Over Temperature, VDD = 3.0V.*

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

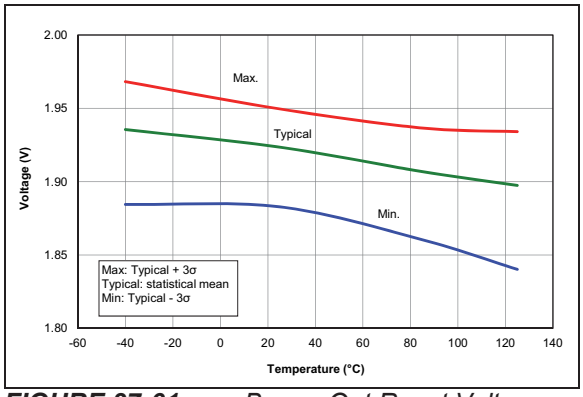


FIGURE 37-61: *Brown-Out Reset Voltage, Low Trip Point (BORV = 1), PIC16LF1764/5/8/9 Only.*

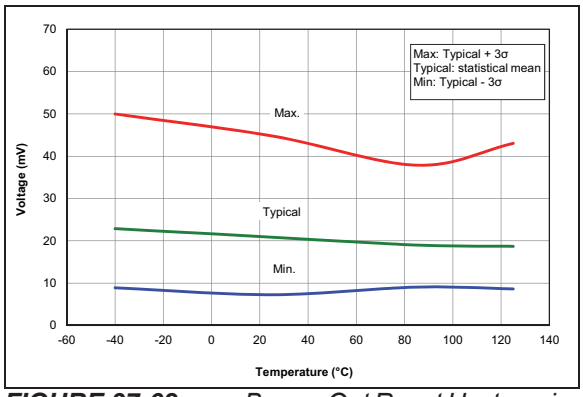


FIGURE 37-62: *Brown-Out Reset Hysteresis, Low Trip Point (BORV = 1), PIC16LF1764/5/8/9 Only.*

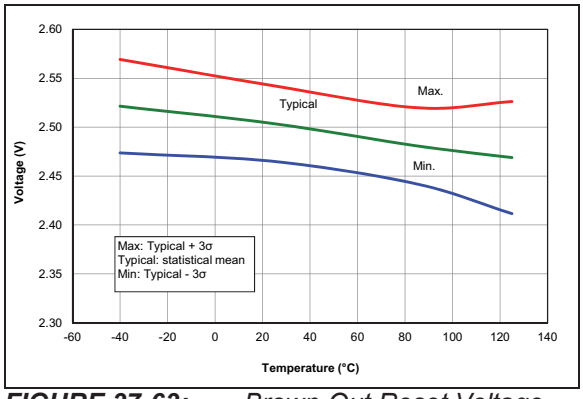


FIGURE 37-63: *Brown-Out Reset Voltage, Low Trip Point (BORV = 1), PIC16F1764/5/8/9 Only.*

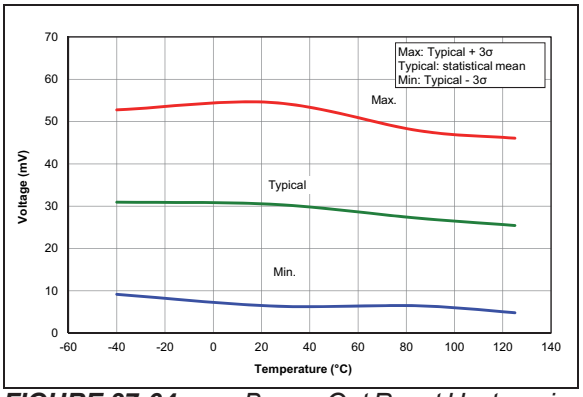


FIGURE 37-64: *Brown-Out Reset Hysteresis, Low Trip Point (BORV = 1), PIC16F1764/5/8/9 Only.*

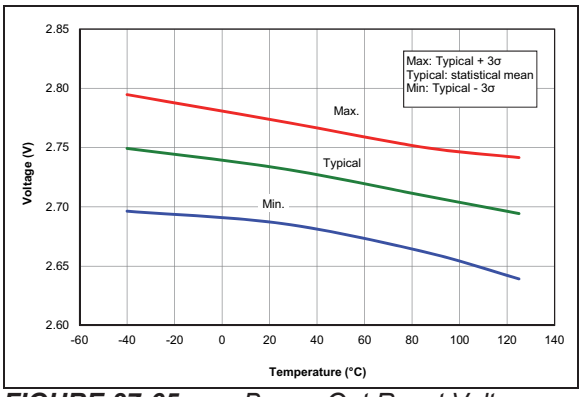


FIGURE 37-65: *Brown-Out Reset Voltage, High Trip Point (BORV = 0).*

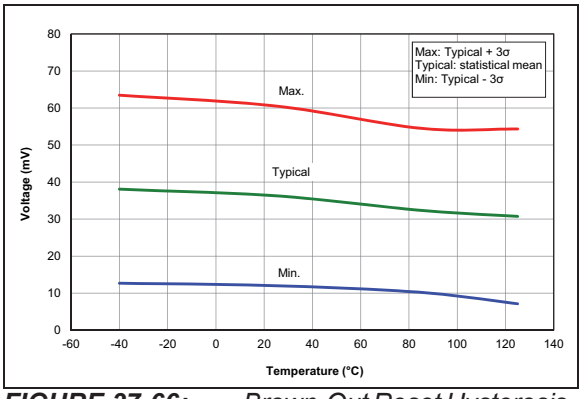


FIGURE 37-66: *Brown-Out Reset Hysteresis, High Trip Point (BORV = 0).*

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

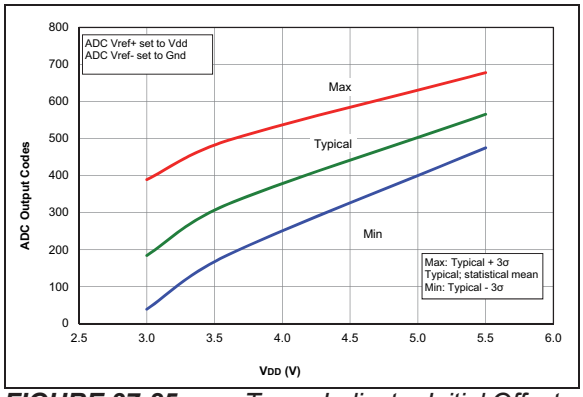


FIGURE 37-85: *Temp. Indicator Initial Offset, High Range, Temp. = 20°C, PIC16F1764/5/8/9 Only..*

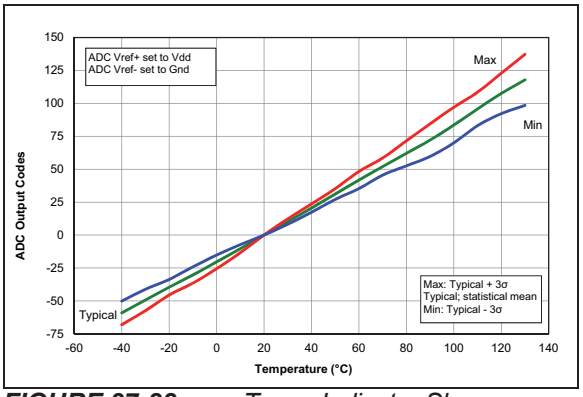


FIGURE 37-88: *Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 5.5V, PIC16F1764/5/8/9 Only.*

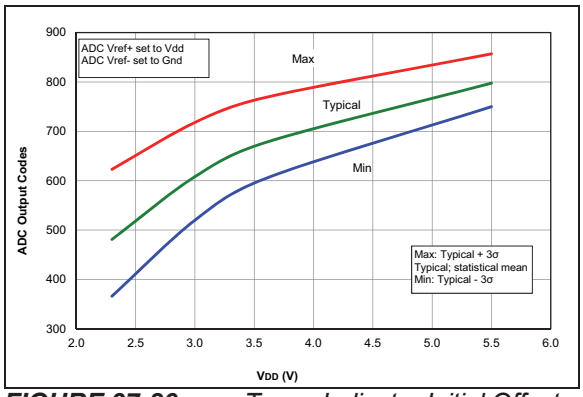


FIGURE 37-86: *Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16F1764/5/8/9 Only.*

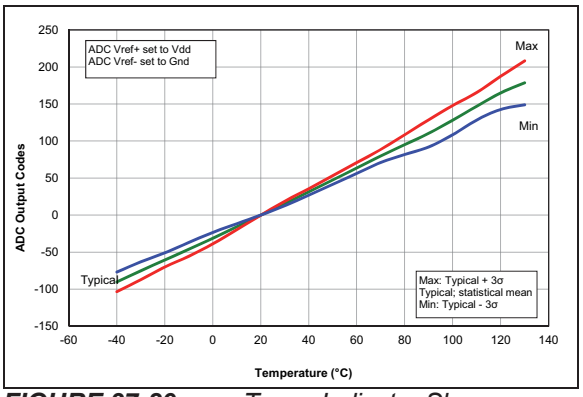


FIGURE 37-89: *Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 3.6V, PIC16F1764/5/8/9 Only.*

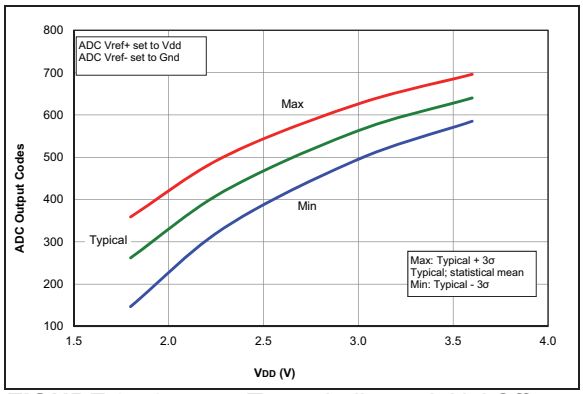


FIGURE 37-87: *Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16LF1764/5/8/9 Only.*

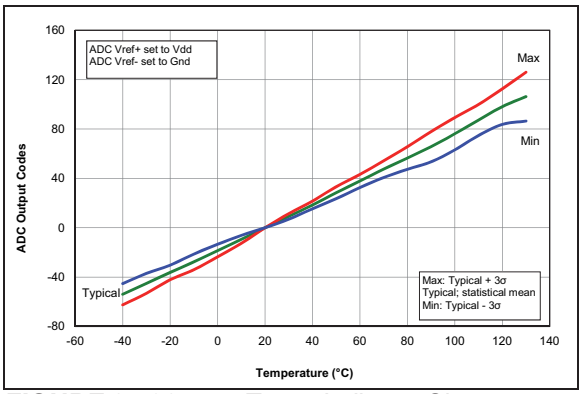


FIGURE 37-90: *Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 3.0V, PIC16F1764/5/8/9 Only.*