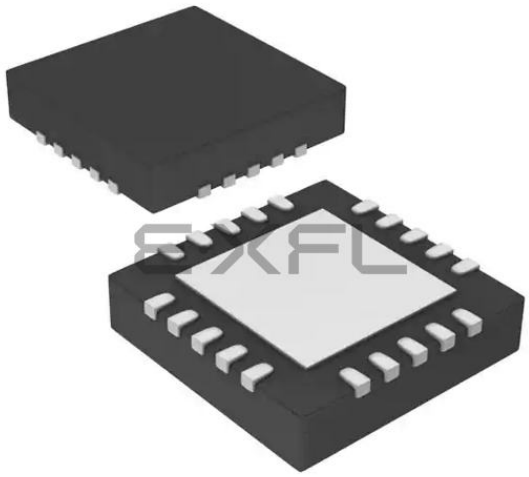

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1768-e-ml

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1768/9) (CONTINUED)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Programmable Ramp Generator	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RC3	7	4	AN7	—	—	OPA2OUT OPA1IN1- OPA1IN1+	C1IN3- C2IN3- C3IN3- C4IN3-	—	PRG2IN0 PRG1IN1	T5G(1)	—	CCP2(1)	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RC4	6	3	—	—	—	—	—	—	PRG1R(1) PRG2R(1)	T3G(1)	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	Y	—
RC5	5	2	—	—	—	—	—	—	PRG1F(1) PRG2F(1)	T3CKI(1)	—	CCP1(1)	—	—	—	—	—	IOC	Y	Y	—
RC6	8	5	AN8	—	—	OPA2IN0-	—	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	IOC	Y	—	—
RC7	9	6	AN9	—	—	OPA2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
OUT(2)	—	—	—	—	—	—	C1OUT	—	—	—	PWM3	CCP1	COG1A	CLC1OUT	MD1OUT	DT(3)	SDO	—	—	—	—
	—	—	—	—	—	—	C2OUT	—	—	—	PWM4	CCP2	COG1B	CLC2OUT	MD2OUT	TX	SDA(3)	—	—	—	—
	—	—	—	—	—	—	C3OUT	—	—	—	PWM5	—	COG1C	CLC3OUT	—	CK	SCK	—	—	—	—
	—	—	—	—	—	—	C4OUT	—	—	—	PWM6	—	COG1D	—	—	—	SCL(3)	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2A	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2B	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2C	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2D	—	—	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection register. See Table 12-1.
2: All pin outputs default to PORT latch data. Any input capable pin can be selected as a digital peripheral output with the PPS Output Selection registers. See Table 12-2.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: Input only.

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4.2 Register Definitions: Configuration Words

REGISTER 4-1: CONFIG1: CONFIGURATION WORD 1

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1
FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$(1)	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **FCMEN:** Fail-Safe Clock Monitor Enable bit
1 = On Fail-Safe Clock Monitor and Internal/External Switchover mode are both enabled
0 = Off Fail-Safe Clock Monitor is disabled

bit 12 **IESO:** Internal External Switchover bit
1 = On Internal/External Switchover mode is enabled
0 = Off Internal/External Switchover mode is disabled

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
If FOSC<2:0> Configuration bits are Set to LP, XT, HS modes:
This bit is ignored, CLKOUT function is disabled. Oscillator function on the CLKOUT pin.
All other FOSC<2:0> modes:
1 = On CLKOUT function is disabled. I/O function on the CLKOUT pin
0 = Off CLKOUT function is enabled on the CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits
11 = On BOR is enabled
10 = NSLEEP BOR is enabled during operation and disabled in Sleep
01 = SBODEN BOR is controlled by the SBOREN bit of the BORCON register
00 = Off BOR is disabled

bit 8 **Unimplemented:** Read as '1'

bit 7 **$\overline{\text{CP}}$:** Code Protection bit(1)
1 = Off Program memory code protection is disabled
0 = On Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/VPP Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = On $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$; weak pull-up is enabled
0 = Off $\overline{\text{MCLR}}$/VPP pin function is a digital input, $\overline{\text{MCLR}}$ is internally disabled; weak pull-up is under control of the WPUA3 bit

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
1 = Off PWRT is disabled
0 = On PWRT is enabled

Note 1: The entire Flash program memory will be erased when the code protection is turned off during an erase. When a bulk erase program memory command is executed, the entire Program Flash Memory and configuration memory will be erased.

5.2.2.5 Internal Oscillator Frequency Selection

The system clock speed can be selected via software using the Internal Oscillator Frequency Select bits IRCF<3:0> of the OSCCON register.

The postscaled output of the 16 MHz HFINTOSC, 500 kHz MFINTOSC, and 31 Hz LFINTOSC connect to a multiplexer (see Figure 5-1). The Internal Oscillator Frequency Select bits, IRCF<3:0> of the OSCCON register, select the frequency output of the internal oscillators. One of the following frequencies can be selected via software:

- 32 MHz (requires 4x PLL)
- 16 MHz
- 8 MHz
- 4 MHz
- 2 MHz
- 1 MHz
- 500 kHz (default after Reset)
- 250 kHz
- 125 kHz
- 62.5 kHz
- 31.25 kHz
- 31 kHz (LFINTOSC)

Note:	Following any Reset, the IRCF<3:0> bits of the OSCCON register are set to '0111' and the frequency selection is set to 500 kHz. The user can modify the IRCFx bits to select a different frequency.

The IRCF<3:0> bits of the OSCCON register allow duplicate selections for some frequencies. These duplicate choices can offer system design trade-offs. Lower power consumption can be obtained when changing oscillator sources for a given frequency. Faster transition times can be obtained between frequency changes that use the same oscillator source.

5.2.2.6 32 MHz Internal Oscillator Frequency Selection

The Internal Oscillator Block can be used with the 4x PLL associated with the External Oscillator Block to produce a 32 MHz internal system clock source. The following settings are required to use the 32 MHz internal clock source:

- The FOSCx bits in the Configuration Words must be set to use the INTOSC source as the device system clock (FOSC<2:0> = 100).
- The SCSx bits in the OSCCON register must be cleared to use the clock determined by FOSC<2:0> in the Configuration Words (SCS<1:0> = 00).
- The IRCFx bits in the OSCCON register must be set to the 8 MHz HFINTOSC to use (IRCF<3:0> = 1110).
- The SPLLEN bit in the OSCCON register must be set to enable the 4x PLL or the PLLEN bit of the Configuration Words must be programmed to a '1'.

Note:	When using the PLLEN bit of the Configuration Words, the 4x PLL cannot be disabled by software and the SPLLEN option will not be available.

The 4x PLL is not available for use with the internal oscillator when the SCSx bits of the OSCCON register are set to '1x'. The SCSx bits must be set to '00' to use the 4x PLL with the internal oscillator.

5.2.2.7 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-7). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

1. IRCF<3:0> bits of the OSCCON register are modified.
2. If the new clock is shut down, a clock start-up delay is started.
3. Clock switch circuitry waits for a falling edge of the current clock.
4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
5. The new clock is now active.
6. The OSCSTAT register is updated as required.
7. Clock switch is complete.

See Figure 5-7 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 5-1.

Start-up delay specifications are located in the oscillator tables of **Section 36.0 "Electrical Specifications"**.

5.3 Clock Switching

The system clock source can be switched between external and internal clock sources via software using the System Clock Select (SCS) bits of the OSCCON register. The following clock sources can be selected using the SCS<1:0> bits:

- Default system oscillator determined by the FOSCx bits in the Configuration Words
- Timer1 32 kHz crystal oscillator
- Internal Oscillator Block (INTOSC)

5.3.1 SYSTEM CLOCK SELECT (SCS) BITS

The System Clock Select (SCS<1:0>) bits of the OSCCON register select the system clock source that is used for the CPU and peripherals.

- When SCS<1:0> = 00, the system clock source is determined by the value of the FOSC<2:0> bits in the Configuration Words.
- When SCS<1:0> = 01, the system clock source is the secondary oscillator.
- When SCS<1:0> = 1x, the system clock source is chosen by the internal oscillator frequency selected by the IRCF<3:0> bits of the OSCCON register. After a Reset, the SCSx bits of the OSCCON register are always cleared.

Note:	Any automatic clock switch, which may occur from Two-Speed Start-up or Fail-Safe Clock Monitor, does not update the SCS bits of the OSCCON register. The user can monitor the OSTS bit of the OSCSTAT register to determine the current system clock source.

When switching between clock sources, a delay is required to allow the new clock to stabilize. These oscillator delays are shown in Table 5-1.

5.3.2 OSCILLATOR START-UP TIMER STATUS (OSTS) BIT

The Oscillator Start-up Timer Status (OSTS) bit of the OSCSTAT register indicates whether the system clock is running from the external clock source, as defined by the FOSC<2:0> bits in the Configuration Words, or from the internal clock source. In particular, OSTS indicates that the Oscillator Start-up Timer (OST) has timed out for LP, XT or HS modes. The OST does not reflect the status of the secondary oscillator.

5.3.3 SECONDARY OSCILLATOR

The secondary oscillator is a separate crystal oscillator associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the SOSCO and SOSCI device pins.

The secondary oscillator is enabled using the OSCEN control bit in the T1CON register. See **Section 22.0 "Timer1/3/5 Module with Gate Control"** for more information about the Timer1 peripheral.

5.3.4 SECONDARY OSCILLATOR READY (SOSCR) BIT

The user must ensure that the secondary oscillator is ready to be used before it is selected as a system clock source. The Secondary Oscillator Ready (SOSCR) bit of the OSCSTAT register indicates whether the secondary oscillator is ready to be used. After the SOSCR bit is set, the SCSx bits can be configured to select the secondary oscillator.

5.3.5 CLOCK SWITCH BEFORE SLEEP

When a clock switch from an old clock to a new clock is requested just prior to entering Sleep mode, it is necessary to confirm that the switch is complete before the sleep instruction is executed. Failure to do so may result in an incomplete switch and consequential loss of the system clock altogether. Clock switching is confirmed by monitoring the clock status bits in the OSCSTAT register. Switch confirmation can be accomplished by sensing that the ready bit for the new clock is set or the ready bit for the old clock is cleared. For example, when switching between the internal oscillator with the PLL and the internal oscillator without the PLL, monitor the PLLR bit. When PLLR is set, the switch to 32 MHz operation is complete. Conversely, when PLLR is cleared, the switch from 32 MHz operation to the selected internal clock is complete.

9.6 Register Definitions: Watchdog Control

REGISTER 9-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0
—	—	WDTPS<4:0>(1)					SWDTEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-m/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as '0'

bit 5-1 **WDTPS<4:0>:** Watchdog Timer Period Select bits(1)

Bit Value = Prescale Rate
- 11111 = Reserved, results in minimum interval (1:32)
- •
- •
- •
- 10011 = Reserved, results in minimum interval (1:32)
- 10010 = 1:8388608 (2^{23}) (Interval 256s nominal)
- 10001 = 1:4194304 (2^{22}) (Interval 128s nominal)
- 10000 = 1:2097152 (2^{21}) (Interval 64s nominal)
- 01111 = 1:1048576 (2^{20}) (Interval 32s nominal)
- 01110 = 1:524288 (2^{19}) (Interval 16s nominal)
- 01101 = 1:262144 (2^{18}) (Interval 8s nominal)
- 01100 = 1:131072 (2^{17}) (Interval 4s nominal)
- 01011 = 1:65536 (Interval 2s nominal) (Reset value)
- 01010 = 1:32768 (Interval 1s nominal)
- 01001 = 1:16384 (Interval 512 ms nominal)
- 01000 = 1:8192 (Interval 256 ms nominal)
- 00111 = 1:4096 (Interval 128 ms nominal)
- 00110 = 1:2048 (Interval 64 ms nominal)
- 00101 = 1:1024 (Interval 32 ms nominal)
- 00100 = 1:512 (Interval 16 ms nominal)
- 00011 = 1:256 (Interval 8 ms nominal)
- 00010 = 1:128 (Interval 4 ms nominal)
- 00001 = 1:64 (Interval 2 ms nominal)
- 00000 = 1:32 (Interval 1 ms nominal)

bit 0 **SWDTEN:** Software Enable/Disable for Watchdog Timer bit

If WDTE<1:0> = 1x:
This bit is ignored.

If WDTE<1:0> = 01:
1 = WDT is turned on
0 = WDT is turned off

If WDTE<1:0> = 00:
This bit is ignored.

Note 1: Times are approximate. WDT time is based on 31 kHz LFINTOSC.

11.6 Register Definitions: PORTC

REGISTER 11-17: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RC<7:0>(1,2)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **RC<7:0>**: PORTC General Purpose I/O Pin bits(1,2)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTC are actually written to corresponding LATC register. Reads from the PORTC register are the return of actual I/O pin values.
2: RC<7:6> are available on PIC16(L)F1768/9 only.

REGISTER 11-18: TRISC: PORTC TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISC<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits(1)
1 = PORTC pin is configured as an input (tri-stated)
0 = PORTC pin is configured as an output

Note 1: TRISC<7:6> are available on PIC16(L)F1768/9 only.

REGISTER 16-4: ADRESH: ADC RESULT REGISTER HIGH (ADFM = 0)

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
ADRES<9:2>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **ADRES<9:2>:** ADC Result Register bits
Upper eight bits of 10-bit conversion result.

REGISTER 16-5: ADRESL: ADC RESULT REGISTER LOW (ADFM = 0)

R/W-x/u	R/W-x/u	r-x/u	r-x/u	r-x/u	r-x/u	r-x/u	r-x/u
ADRES<1:0>		—	—	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	r = Reserved bit
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **ADRES<1:0>:** ADC Result Register bits
Lower two bits of 10-bit conversion result.

bit 5-0 **Reserved:** Do not use.

FIGURE 26-12: OFFSET MATCH ON INCREMENTING TIMER TIMING DIAGRAM

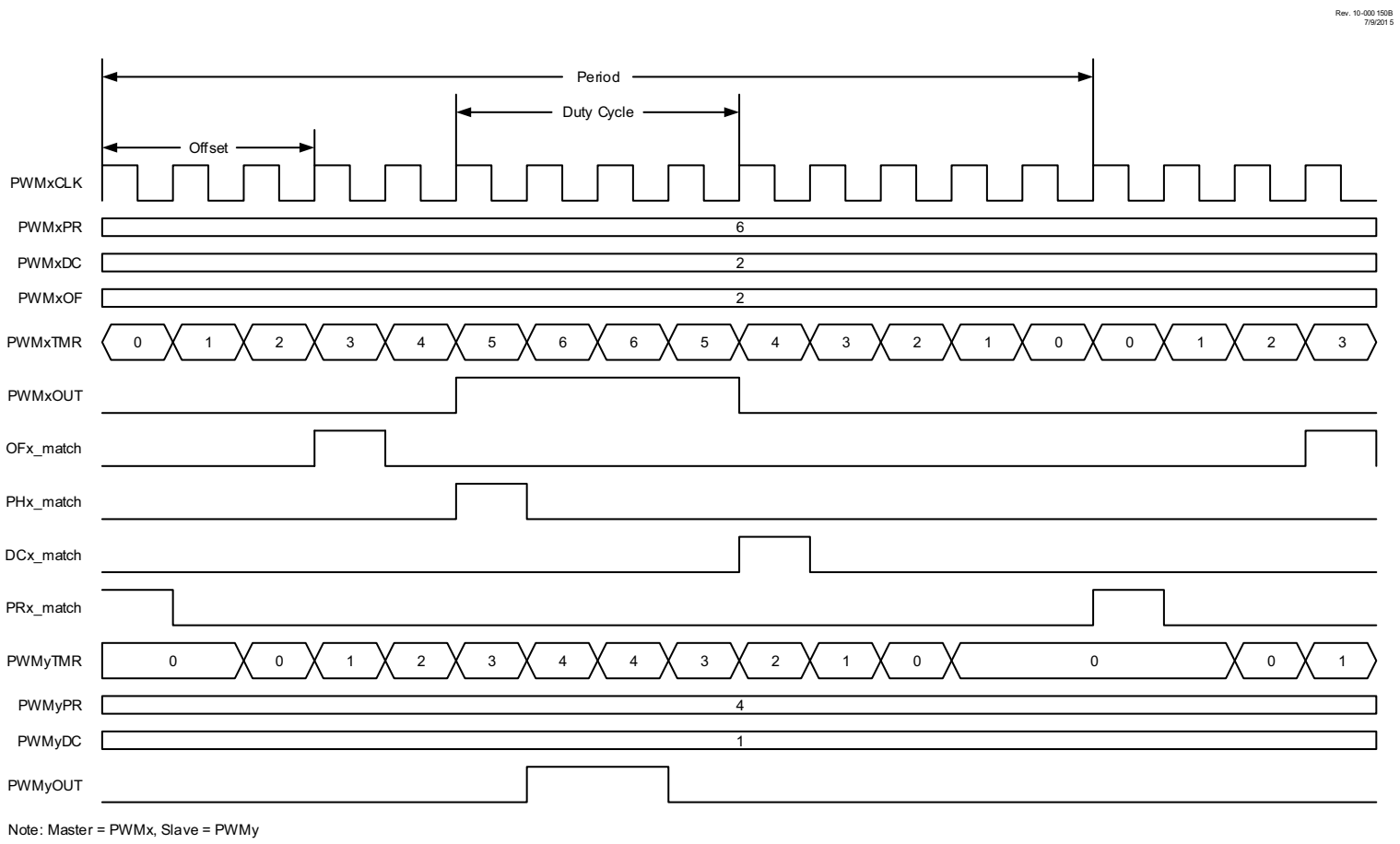


TABLE 26-2: SUMMARY OF REGISTERS ASSOCIATED WITH PWMx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		84
PWMEN	—	—	MPWM6EN(1)	MPWM5EN	—	—	—	—	291
PWMLD	—	—	MPWM6LD(1)	MPWM5LD	—	—	—	—	291
PWMOUT	—	—	MPWM6OUT(1)	MPWM5OUT	—	—	—	—	291
PWM5PHL	PH<7:0>								286
PWM5PHH	PH<15:8>								286
PWM5DCL	DC<7:0>								287
PWM5DCH	DC<15:8>								287
PWM5PRH	PR<15:8>								288
PWM5PRL	PR<7:0>								288
PWM5OFH	OF<15:8>								289
PWM5OFL	OF<7:0>								289
PWM5TMRH	TMR<15:8>								290
PWM5TMRL	TMR<7:0>								290
PWM5CON	EN	—	OUT	POL	MODE<1:0>		—	—	280
PWM5INTE	—	—	—	—	OFIE	PHIE	DCIE	PRIE	281
PWM5INTF	—	—	—	—	OFIF	PHIF	DCIF	PRIF	282
PWM5CLKCON	—	PS<2:0>			—	—	CS<1:0>		283
PWM5LDCON	LDA	LDT(1)	—	—	—	—	—	LDS(1)	284
PWM5OFCON	—	OFM<1:0>(1)		OFO	—	—	—	OFS(1)	285
PWM6PHL(1)	PH<7:0>								286
PWM6PHH(1)	PH<15:8>								286
PWM6DCL(1)	DC<7:0>								287
PWM6DCH(1)	DC<15:8>								287
PWM6PRL(1)	PR<7:0>								288
PWM6PRH(1)	PR<15:8>								288
PWM6OFL(1)	OF<7:0>								289
PWM6OFH(1)	OF<15:8>								289
PWM6TMRL(1)	TMR<7:0>								290
PWM6TMRH(1)	TMR<15:8>								290
PWM6CON(1)	EN	—	OUT	POL	MODE<1:0>		—	—	280
PWM6INTE(1)	—	—	—	—	OFIE	PHIE	DCIE	PRIE	281
PWM6INTF(1)	—	—	—	—	OFIF	PHIF	DCIF	PRIF	282
PWM6CLKCON(1)	—	PS<2:0>			—	—	CS<1:0>		283
PWM6LDCON(1)	LDA	LDT(1)	—	—	—	—	—	LDS(1)	284
PWM6OFCON(1)	—	OFM<1:0>(1)		OFO	—	—	—	OFS(1)	285

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PWM.

Note 1: PIC16(L)F1768/9 only

TABLE 26-3: SUMMARY OF CONFIGURATION WORDS WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	63
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

REGISTER 27-6: COGxRSIM1: COGx RISING EVENT SOURCE INPUT MODE REGISTER 1 (CONTINUED)

bit 1 **RSIM9:** COGx Rising Event Input Source 9 Mode bit

RIS9 = 1:

1 = PWM5 output low-to-high transition will cause a rising event after rising event phase delay
0 = PWM5 output high level will cause an immediate rising event

RIS9 = 0:

PWM5 output has no effect on rising event.

bit 0 **RSIM8:** COGx Rising Event Input Source 8 Mode bit

RIS8 = 1:

1 = PWM4 output low-to-high transition will cause a rising event after rising event phase delay
0 = PWM4 output high level will cause an immediate rising event

RIS8 = 0:

PWM4 output has no effect on rising event.

Note 1: PIC16(L)F1768/9 only. Otherwise unimplemented, read as '0'.

30.9 Slope Compensation Application

An example slope compensation circuit is shown in Figure 30-6. The PRG input voltage is PRGxIN which shares an I/O pin with the op amp output. The op amp output is designed to operate at the expected peak current sense voltage, which we'll call VREF. The PRG output voltage starts at VREF and should fall at a rate less than half the target circuit current sense voltage rate of rise. Therefore, the compensator slope, expressed as volts per µs, can be computed by Equation 30-1.

EQUATION 30-1: COMPENSATOR SLOPE

$$\frac{V}{\mu s} \geq \frac{\frac{V_{REF}}{2}}{PWM\ Period\ (\mu s)}$$

For example, when the circuit is using a 1Ω current sense resistor and the peak current is 1A, then the peak current expressed as a voltage is 1V. Therefore, for this example the op amp output should be designed to operate at 1V. If the power supply PWM frequency is 1 MHz, then the period is 1 µs. Therefore, the desired slope is 0.5 V/µs, which is computed as shown in Equation 30-2.

EQUATION 30-2: CALCULATION EXAMPLE

$$\frac{\frac{V_{REF}}{2}}{PWM\ Period\ (\mu s)} = \frac{\frac{1}{2}}{1\mu s} = 0.5V/\mu s$$

Note: The setting for 0.5V/µs is ISET<4:0> = 6

FIGURE 30-6: EXAMPLE SLOPE COMPENSATION CIRCUIT

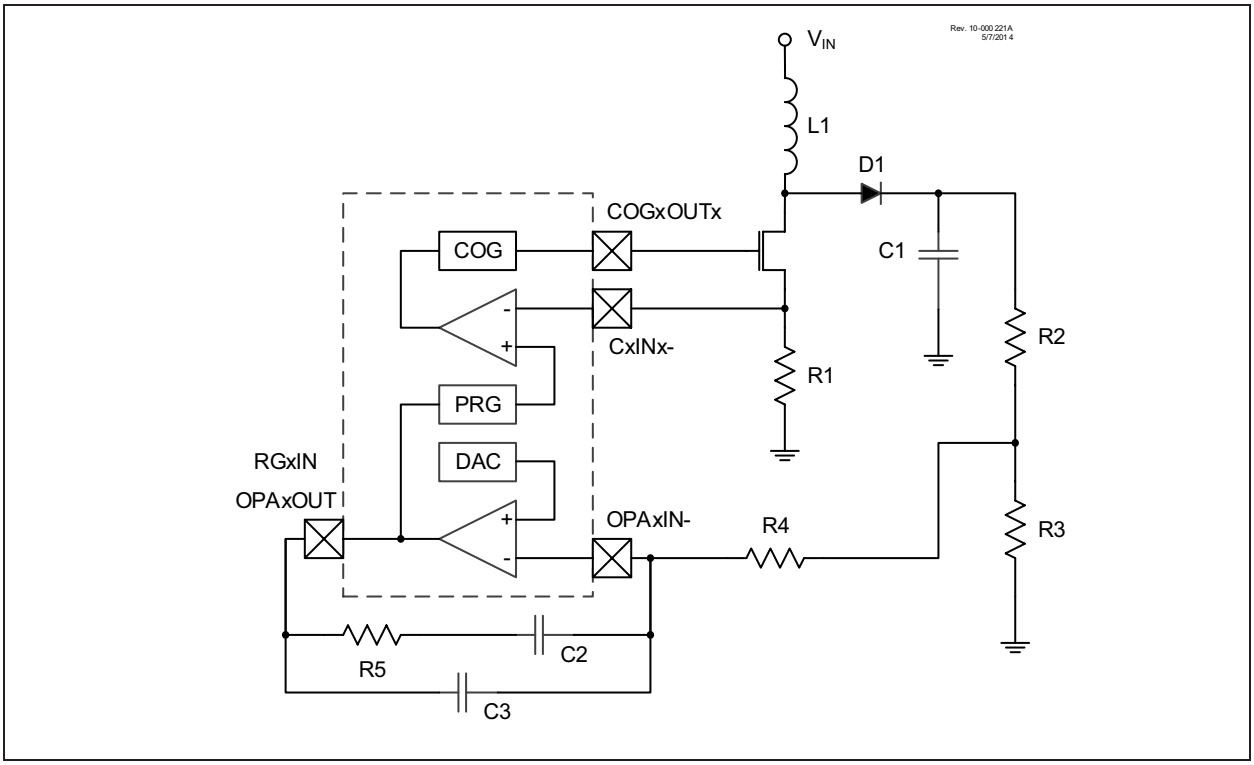


FIGURE 32-9: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

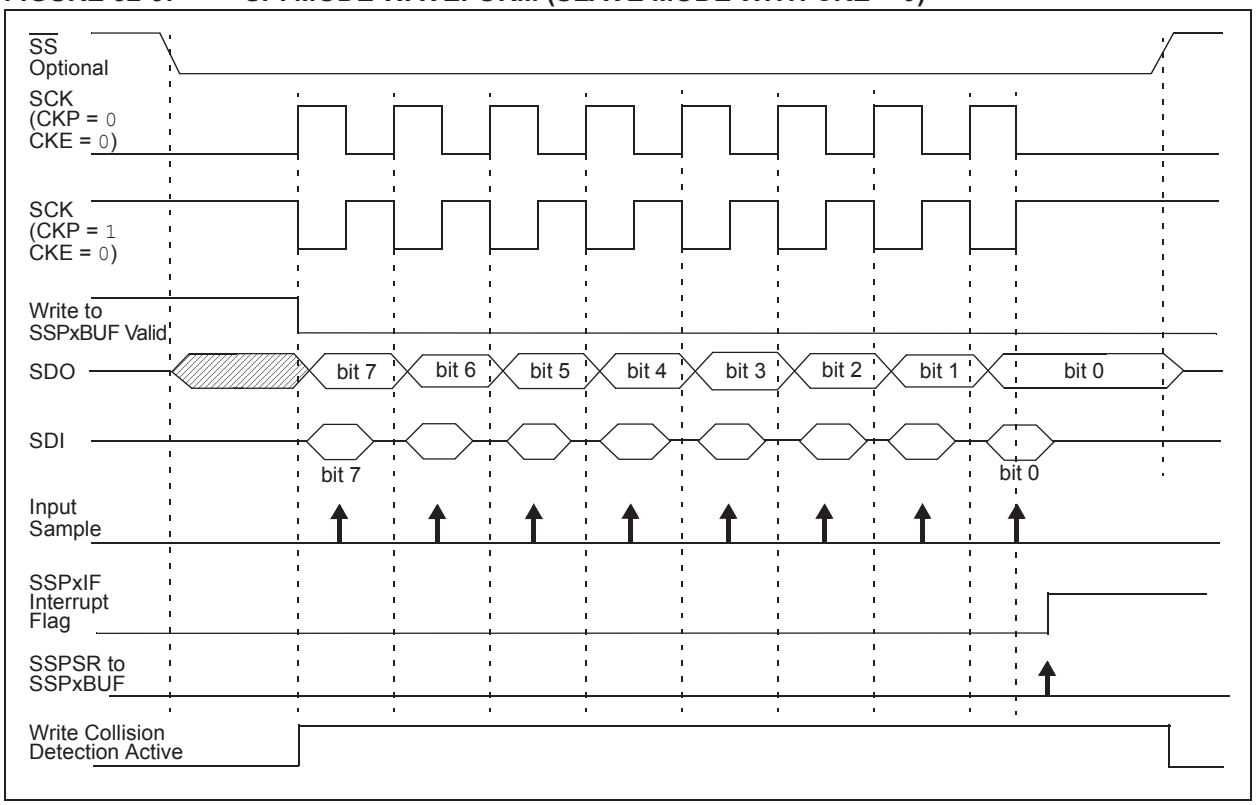
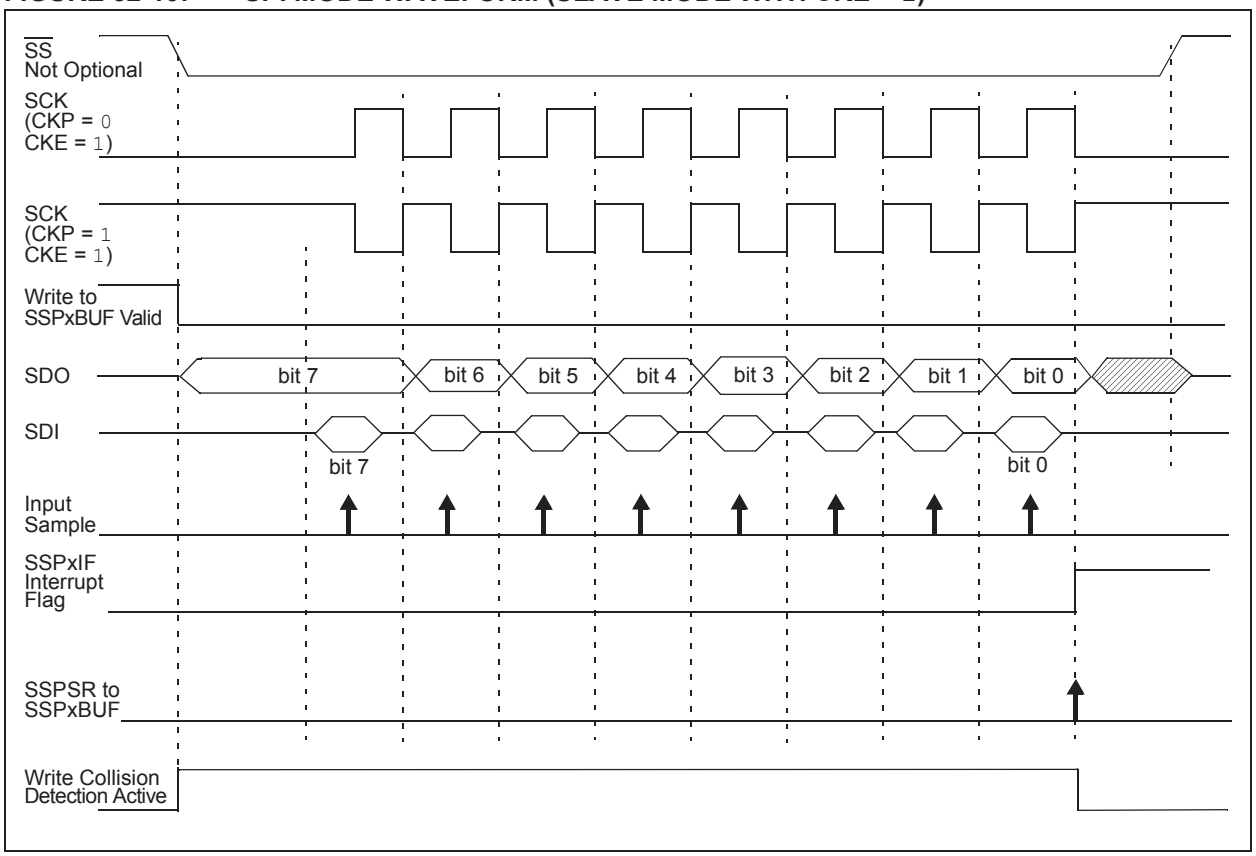


FIGURE 32-10: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



32.4.9 ACKNOWLEDGE SEQUENCE

The 9th SCL pulse for any transferred byte in I^{2}C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge ($\overline{ACK}$) is an active-low signal, pulling the SDA line low indicates to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an $\overline{ACK}$ is placed in the ACKSTAT bit of the SSPxCON2 register.

Slave software, when the AHEN and DHEN bits are set, allows the user to set the $\overline{ACK}$ value sent back to the transmitter. The ACKDT bit of the SSPxCON2 register is set/cleared to determine the response.

Slave hardware will generate an $\overline{ACK}$ response if the AHEN and DHEN bits of the SSPxCON3 register are clear.

There are certain conditions where an $\overline{ACK}$ will not be sent by the slave. If the BF bit of the SSPxSTAT register or the SSPOV bit of the SSPxCON1 register are set when a byte is received.

When the module is addressed, after the eighth falling edge of SCL on the bus, the ACKTIM bit of the SSPxCON3 register is set. The ACKTIM bit indicates the Acknowledge time of the active bus. The ACKTIM status bit is only active when the AHEN bit or DHEN bit is enabled.

32.5 I^{2}C Slave Mode Operation

The MSSP Slave mode operates in one of four modes selected by the SSPM<3:0> bits of SSPxCON1 register. The modes can be divided into 7-Bit and 10-Bit Addressing modes. 10-Bit Addressing mode operates the same as 7-bit with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operate the same as the other modes, with SSPxIF additionally getting set upon detection of a Start, Restart or Stop condition.

32.5.1 SLAVE MODE ADDRESSES

The SSPxADD register (Register 32-6) contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPxBUF register and an interrupt is generated. If the value does not match, the module goes Idle and no indication is given to the software that anything happened.

The SSP Mask register (Register 32-5) affects the address matching process. See **Section 32.5.8 "SSP Mask Register"** for more information.

32.5.1.1 I^{2}C Slave 7-Bit Addressing Mode

In 7-Bit Addressing mode, the LSb of the received data byte is ignored when determining if there is an address match.

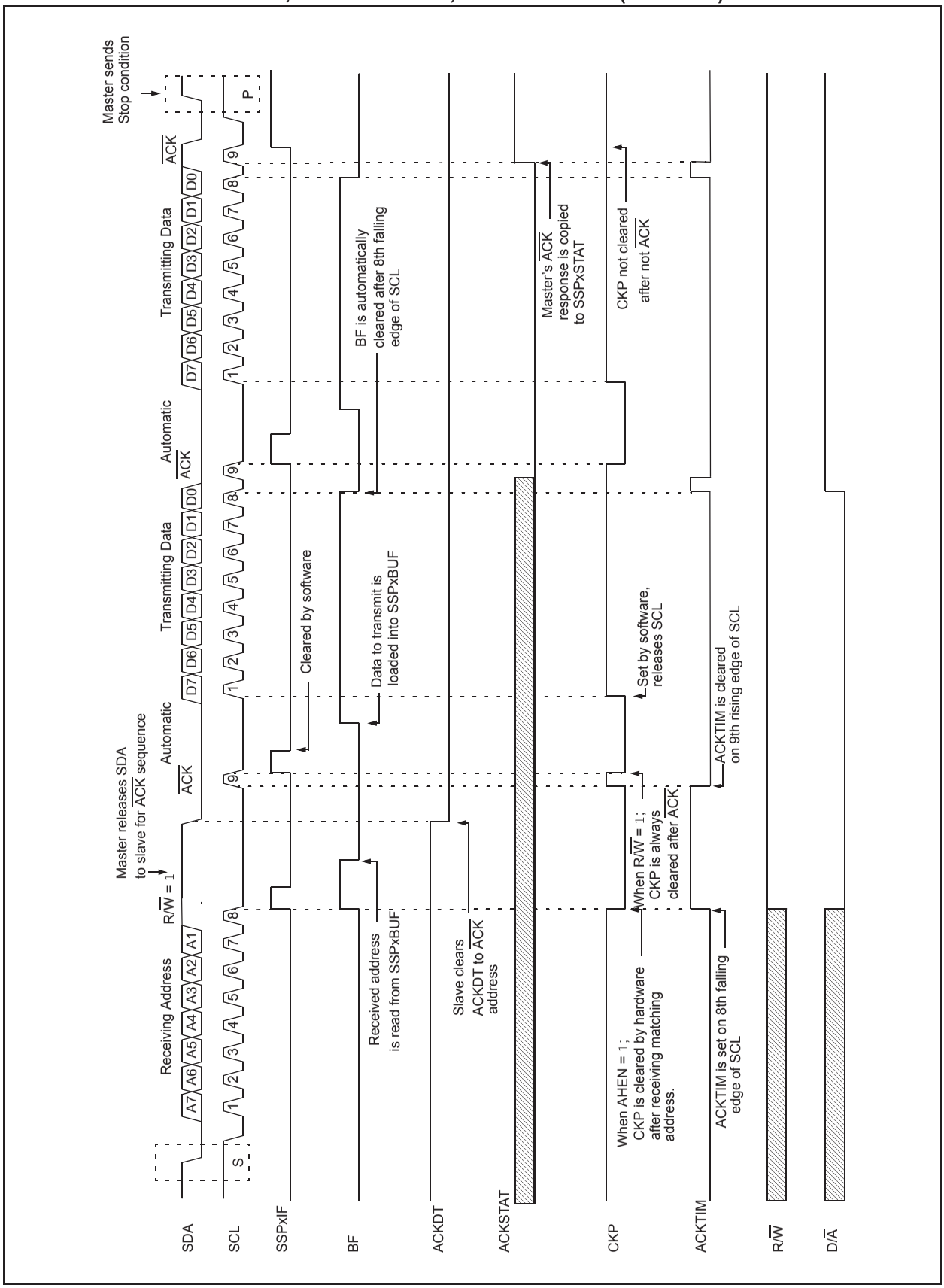
32.5.1.2 I^{2}C Slave 10-Bit Addressing Mode

In 10-Bit Addressing mode, the first received byte is compared to the binary value of '1 1 1 1 0 A9 A8 0'. A9 and A8 are the two MSbs of the 10-bit address and stored in bits 2 and 1 of the SSPxADD register.

After the Acknowledge of the high byte, the UA bit is set and SCL is held low until the user updates SSPxADD with the low address. The low address byte is clocked in and all eight bits are compared to the low address value in SSPxADD. Even if there is not an address match, SSPxIF and UA are set, and SCL is held low until SSPxADD is updated to receive a high byte again. When SSPxADD is updated, the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-Bit Addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/$\overline{W}$ bit set. The slave hardware will then Acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.

FIGURE 32-19: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)



33.1.2.8 Asynchronous Reception Setup

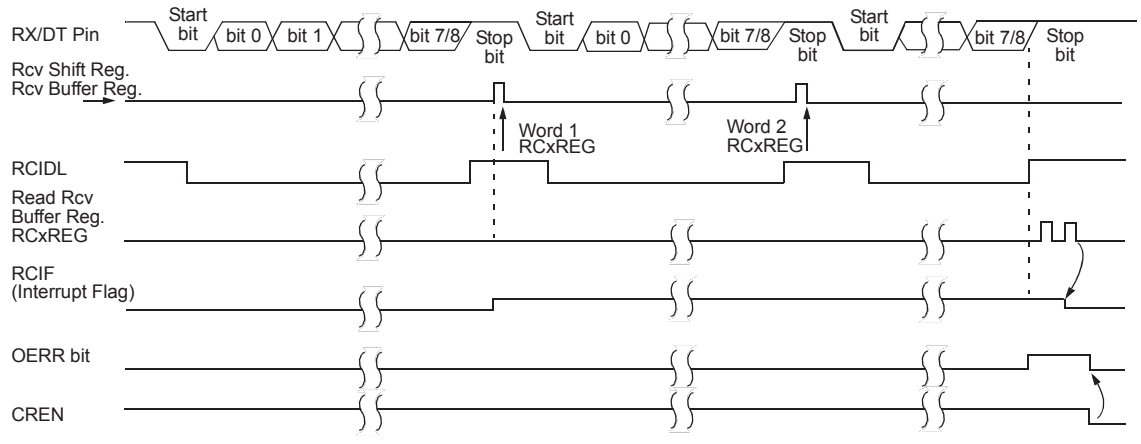
1. Initialize the SPxBRGH, SPxBRGL register pair, and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 33.4 "EUSART Baud Rate Generator (BRG)"**).
2. Clear the ANSELx bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register, and the GIE and PEIE bits of the INTCON register.
5. If 9-bit reception is desired, set the RX9 bit.
6. Enable reception by setting the CREN bit.
7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
8. Read the RCxSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

33.1.2.9 9-bit Address Detection Mode Setup

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

1. Initialize the SPxBRGH, SPxBRGL register pair, and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 33.4 "EUSART Baud Rate Generator (BRG)"**).
2. Clear the ANSELx bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register, and the GIE and PEIE bits of the INTCON register.
5. Enable 9-bit reception by setting the RX9 bit.
6. Enable address detection by setting the ADDEN bit.
7. Enable reception by setting the CREN bit.
8. The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
9. Read the RCxSTA register to get the error flags. The ninth data bit will always be set.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCxREG register. Software determines if this is the device's address.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

FIGURE 33-5: ASYNCHRONOUS RECEPTION



Note: This timing diagram shows three words appearing on the RX input. The RCxREG (receive buffer) is read after the third word, causing the OERR (Overrun) bit to be set.

33.5 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data, but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

33.5.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for synchronous master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXxSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXxSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCxSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCxSTA register enables the EUSART.

33.5.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

33.5.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUDxCON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock. Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

33.5.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXxREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXxREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXxREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXxREG.

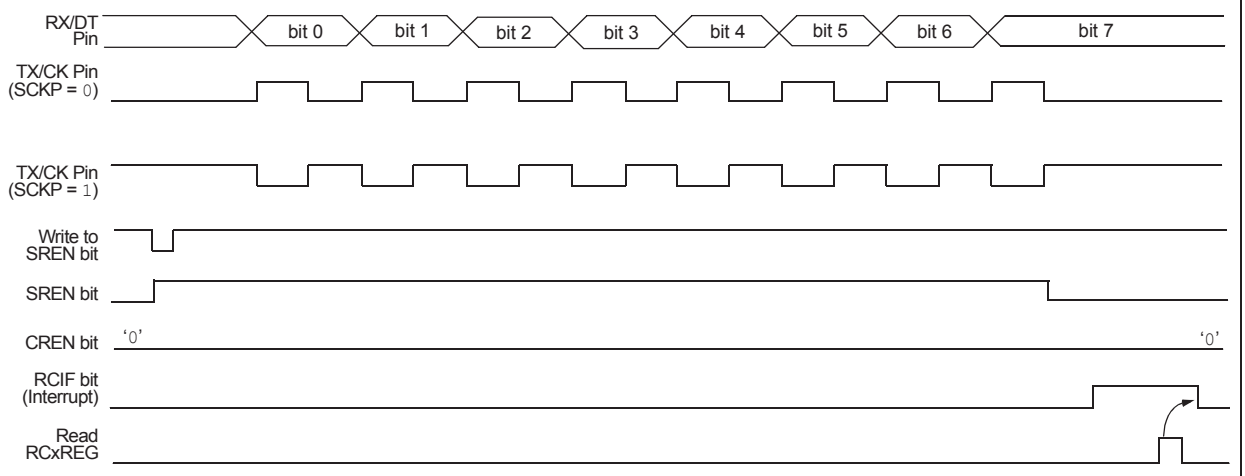
Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

Note:	The TSR register is not mapped in data memory, so it is not available to the user.

33.5.1.4 Synchronous Master Transmission Setup

1. Initialize the SPxBRGH, SPxBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 33.4 "EUSART Baud Rate Generator (BRG)"**).
2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
3. Disable Receive mode by clearing bits, SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXIE bit of the PIE1 register, and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXxREG register.

FIGURE 33-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

TABLE 33-8: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELB(1)	ANSB<7:4>				—	—	—	—	143
ANSELC	ANSC<7:6>(1)		—	—	ANSC<3:0>				148
BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	442
CKPPS	—	—	—	CKPPS<4:0>					154, 156
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	102
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	105
RC1REG	EUSART Receive Data Register								436*
RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	441
RXPPS	—	—	—	RXPPS<4:0>					154, 156
RxyPPS	—	—	—	RxyPPS<4:0>					154
SP1BRGL	BRG<7:0>								443*
SP1BRGH	BRG<15:8>								443*
TRISA	—	—	TRISA<5:4>		—(2)	TRISA<2:0>			136
TRISB(1)	TRISB<7:4>				—	—	—	—	142
TRISC	TRISC<7:6>(1)		TRISC<5:0>						147
TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	440

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous master reception.

* Page provides register information.

Note 1: PIC16(L)F1768/9 only.

2: Unimplemented, read as '1'.

36.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} – Operating Supply Voltage(1)

PIC16LF1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +1.8V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +3.6V

PIC16F1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +2.3V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +5.5V

T_A – Operating Ambient Temperature Range

Industrial Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +85°C

Extended Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

TABLE 36-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)					
Param No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	70.0	°C/W	14-pin PDIP package
			95.3	°C/W	14-pin SOIC package
			100.0	°C/W	14-pin TSSOP package
			51.5	°C/W	16-pin QFN 4x4 mm package
			62.2	°C/W	20-pin PDIP package
			87.3	°C/W	20-pin SSOP
			77.7	°C/W	20-pin SOIC package
			43.0	°C/W	20-pin QFN 4x4 mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	32.75	°C/W	14-pin PDIP package
			31.0	°C/W	14-pin SOIC package
			24.4	°C/W	14-pin TSSOP package
			5.4	°C/W	16-pin QFN 4x4 mm package
			27.5	°C/W	20-pin PDIP package
			31.1	°C/W	20-pin SSOP
			23.1	°C/W	20-pin SOIC package
			5.3	°C/W	20-pin QFN 4x4 mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ (1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \Sigma (I_{OL} * V_{OL}) + \Sigma (I_{OH} * (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = P_{DMAX} (T_J - T_A)/\theta_{JA}$ (2)

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature, T_J = Junction Temperature.