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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1768-e-ss

TABLE 1-2: PIC16(L)F1764/5 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/T1CKI/T2IN/CLCIN3/ MD1MOD/SOSCI/OSC1/CLKIN	RA5	TTL/ST	CMOS	General purpose I/O.
	T1CKI(1)	TTL/ST	—	Timer1 clock input.
	T2IN(1)	TTL/ST	—	Timer2 clock input.
	CLCIN3(1)	TTL/ST	—	CLC Input 3.
	MD1MOD(1)	TTL/ST	—	Data Signal Modulator modulation input.
	SOSCI	—	XTAL	Secondary Oscillator connection.
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	CLKIN	ST	—	External Clock input (EC mode).
RC0/AN4/OPA1IN+/C2IN0+/ T5CKI/SCL/SCK	RC0	TTL/ST	CMOS	General purpose I/O.
	AN4	AN		ADC Channel 4 input.
	OPA1IN+	AN	—	Operational Amplifier 1 non-inverting input.
	C2IN0+	AN	—	Comparator 2 positive input.
	T5CKI(1)	TTL/ST	—	Timer5 clock input.
	SCL(1,3)	I^2C	—	I^2C clock output.
	SCK(1)	TTL/ST	—	SPI clock input.
RC1/AN5/OPA1IN-/C1IN1-/ C2IN1-/T4IN/CLCIN2/SDI/SDA	RC1	TTL/ST	CMOS	General purpose I/O.
	AN5	AN	XTAL	ADC Channel 5 input.
	OPA1IN-	AN	—	Operational Amplifier 1 inverting input.
	C1IN1-	AN	—	Comparator 1 negative input.
	C2IN1-	AN	—	Comparator 2 negative input.
	T4IN(1)	TTL/ST	—	Timer4 clock input.
	CLCIN2(1)	TTL/ST	—	CLC Input 2.
	SDI(1)	TTL/ST	—	SPI data input.
	SDA(1)	I^2C	—	I^2C data output.
RC2/AN6/OPA1OUT/C1IN2-/ C2IN2-/PRG1IN0	RC2	TTL/ST	CMOS	General purpose I/O.
	AN6	AN	—	ADC Channel 6 input.
	OPA1OUT	—	AN	Operational Amplifier 1 output.
	C1IN2-	AN	—	Comparator 1 negative input.
	C2IN2-	AN	—	Comparator 2 negative input.
	PRG1IN0	AN	—	Ramp Generator 1 reference voltage input.
RC3/AN7/C1IN3-/C2IN3-/T5G/ CLCIN0/$\overline{SS}$	RC3	TTL/ST	CMOS	General purpose I/O.
	AN7	AN	—	ADC Channel 7 input.
	C1IN3-	AN	—	Comparator 1 negative input.
	C2IN3-	AN	—	Comparator 2 negative input.
	T5G(1)	TTL/ST	—	Timer5 gate input.
	CLCIN0(1)	TTL/ST	—	CLC Input 0.
	$\overline{SS}$(1)	TTL/ST	—	SPI Slave Select input.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 1-2: PIC16(L)F1764/5 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/T3G/PRG1R/CLCIN1/CK	RC4	TTL/ST	CMOS	General purpose I/O.
	T3G(1)	TTL/ST	—	Timer3 gate input.
	PRG1R(1)	TTL/ST	—	Ramp generator set_rising input.
	CLCIN1(1)	TTL/ST	—	CLC Input 1.
	CK(1)	TTL/ST	—	EUSART clock input.
RC5/T3CKI/PRG1F/CCP1/RX	RC5	TTL/ST	CMOS	General purpose I/O.
	T3CKI(1)	TTL/ST	—	Timer3 clock input.
	PRG1F(1)	TTL/ST	—	Ramp generator set_falling input.
	CCP1(1)	TTL/ST	—	CCP1 capture input.
	RX(1,3)	TTL/ST	—	EUSART receive input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	CCP1		CMOS	Compare/PWM1 output.
	MD1OUT		CMOS	Data Signal Modulator 1 output.
	PWM3		CMOS	PWM3 output.
	PWM5		CMOS	PWM5 output.
	COG1A		CMOS	Complementary Output Generator Output A.
	COG1B		CMOS	Complementary Output Generator Output B.
	COG1C		CMOS	Complementary Output Generator Output C.
	COG1D		CMOS	Complementary Output Generator Output D.
	SDA(3)		OD	I^2C data output.
	SCK		CMOS	SPI clock output.
	SCL(3)		OD	I^2C clock output.
	SDO		CMOS	SPI data output.
	TX		CMOS	EUSART asynchronous TX data out.
	CK		CMOS	EUSART synchronous clock out.
	DT(3)		CMOS	EUSART synchronous data output.
	CLC1OUT		CMOS	Configurable Logic Cell 1 output.
	CLC2OUT		CMOS	Configurable Logic Cell 2 output.
	CLC3OUT		CMOS	Configurable Logic Cell 3 output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

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TABLE 3-3: PIC16(L)F1764 MEMORY MAP (BANKS 0-7)

	BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	—	08Dh	—	10Dh	—	18Dh	—	20Dh	—	28Dh	—	30Dh	—	38Dh	—
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	—	08Fh	—	10Fh	CMOUT	18Fh	—	20Fh	—	28Fh	—	30Fh	—	38Fh	—
010h	—	090h	—	110h	CM1CON0	190h	—	210h	—	290h	—	310h	—	390h	—
011h	PIR1	091h	PIE1	111h	CM1CON1	191h	PMADRL	211h	SSP1BUF	291h	CCPR1L	311h	—	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1NSEL	192h	PMADRH	212h	SSP1ADD	292h	CCPR1H	312h	—	392h	IOCAN
013h	PIR3	093h	PIE3	113h	CM1PSEL	193h	PMDATL	213h	SSP1MSK	293h	CCP1CON	313h	—	393h	IOCAF
014h	PIR4	094h	PIE4	114h	CM2CON0	194h	PMDATH	214h	SSP1STAT	294h	CCP1CAP	314h	—	394h	—
015h	TMR0	095h	OPTION_REG	115h	CM2CON1	195h	PMCON1	215h	SSP1CON1	295h	—	315h	—	395h	—
016h	TMR1L	096h	PCON	116h	CM2NSEL	196h	PMCON2	216h	SSP1CON2	296h	—	316h	—	396h	—
017h	TMR1H	097h	WDTCON	117h	CM2PSEL	197h	VREGCON(1)	217h	SSP1CON3	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	—	198h	—	218h	—	298h	—	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	—	199h	RC1REG	219h	—	299h	—	319h	—	399h	IOCCF
01Ah	T2TMR	09Ah	OSCSTAT	11Ah	—	19Ah	TX1REG	21Ah	—	29Ah	—	31Ah	—	39Ah	—
01Bh	T2PR	09Bh	ADRESL	11Bh	—	19Bh	SP1BRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	MD1CON0
01Ch	T2CON	09Ch	ADRESH	11Ch	—	19Ch	SP1BRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	MD1CON1
01Dh	T2HLT	09Dh	ADCON0	11Dh	—	19Dh	RC1STA	21Dh	BORCON	29Dh	—	31Dh	—	39Dh	MD1SRC
01Eh	T2CLKCON	09Eh	ADCON1	11Eh	—	19Eh	TX1STA	21Eh	FVRCON	29Eh	CCPTMRS	31Eh	—	39Eh	MD1CARL
01Fh	T2RST	09Fh	ADCON2	11Fh	—	19Fh	BAUD1CON	21Fh	ZCD1CON	29Fh	—	31Fh	—	39Fh	MD1CARH
020h	General Purpose Register 80 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h 32Fh	General Purpose Register 16 Bytes	3A0h	Unimplemented Read as '0'
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		330h 36Fh	Unimplemented Read as '0'	3EFh	
070h	Common RAM 70h-7Fh	0F0h	Accesses 70h-7Fh	170h	Accesses 70h-7Fh	1F0h	Accesses 70h-7Fh	270h	Accesses 70h-7Fh	2F0h	Accesses 70h-7Fh	370h	Accesses 70h-7Fh	3F0h	Accesses 70h-7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: ☐ = Unimplemented data memory locations, read as '0'.

Note 1: Unimplemented on PIC16LF1764.

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TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 10											
50Ch — 50Eh	—	Unimplemented								—	—
50Fh	OPA1NCHS	—	—	—	—	NCH<3:0>				---- 0000	---- 0000
510h	OPA1PCHS	—	—	—	—	PCH<3:0>				---- 0000	---- 0000
511h	OPA1CON	EN	—	—	UG	—	ORPOL	ORM<1:0>		0--0 -000	0--0 -000
512h	OPA1ORS	—	—	—	ORS<4:0>					---0 0000	---0 0000
513h	OPA2NCHS(2)	—	—	—	—	NCH<3:0>				---- 0000	---- 0000
514h	OPA2PCHS(2)	—	—	—	—	PCH<3:0>				---- 0000	---- 0000
515h	OPA2CON(2)	EN	—	—	UG	—	ORPOL	ORM<1:0>		0--0 -000	0--0 -000
516h	OPA2ORS(2)	—	—	—	ORS<4:0>					---0 0000	---0 0000
517h — 51Fh	—	Unimplemented								—	—
Bank 11											
590h	DACLD	---	---	---	---	---	---	DAC2LD(2)	DAC1LD	---- --00	---- --00
591h	DAC1CON0	EN	FM	OE1	---	PSS<1:0>		NSS<1:0>		000- 0000	000- 0000
592h	DAC1REFL	REF<7:0>								0000 0000	0000 0000
593h	DAC1REFH	REF<15:8>								0000 0000	0000 0000
594h	DAC2CON0(2)	EN	FM	OE1	---	PSS<1:0>		NSS<1:0>		000- 0000	000- 0000
595h	DAC2REFL(2)	REF<7:0>								0000 0000	0000 0000
596h	DAC2REFH(2)	REF<15:8>								0000 0000	0000 0000
597h	DAC3CON0	EN	---	OE1	---	PSS<1:0>		NSS<1:0>		0-0- 0000	0-00 0000
598h	DAC3REF	---	---	---	REF<4:0>					---0 0000	---0 0000
599h	DAC4CON0(2)	EN	---	OE1	---	PSS<1:0>		NSS<1:0>		0-0- 0000	0-00 0000
59Ah	DAC4REF(2)	---	---	---	REF<4:0>					---0 0000	---0 0000
59Bh to 59Fh	—	Unimplemented								—	—

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1768/9 only.

3: PIC16(L)F1764/5 only.

4: Unimplemented on PIC16LF1764/5/8/9.

TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 12											
60Ch to 616h	—	Unimplemented								—	—
617h	PWM3DCL	DC<1:0>		—	—	—	—	—	—	xx-- ----	uu-- ----
618h	PWM3DCH	DC<9:2>								xxxx xxxx	uuuu uuuu
619h	PWM3CON	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
61Ah	PWM4DCL(2)	DC<1:0>		—	—	—	—	—	—	00-- ----	uu-- ----
61Bh	PWM4DCH(2)	DC<9:2>								0000 0000	uuuu uuuu
61Ch	PWM4CON(2)	EN	—	OUT	POL	—	—	—	—	0-00 ----	0-00 ----
61Dh — 61Fh	—	Unimplemented								—	—
Bank 13											
68Ch	—	Unimplemented								—	—
68Dh	COG1PHR	—	—	COG Rising Edge Phase Delay Count Register						--00 0000	--00 0000
68Eh	COG1PHF	—	—	COG Falling Edge Phase Delay Count Register						--00 0000	--00 0000
68Fh	COG1BLKR	—	—	COG Rising Edge Blanking Count Register						--00 0000	--00 0000
690h	COG1BLKF	—	—	COG Falling Edge Blanking Count Register						--00 0000	--00 0000
691h	COG1DBR	—	—	COG Rising Edge Dead-band Count Register						--00 0000	--00 0000
692h	COG1DBF	—	—	COG Falling Edge Dead-band Count Register						--00 0000	--00 0000
693h	COG1CON0	EN	LD	—	CS<1:0>		MD<2:0>			00-0 0000	00-0 0000
694h	COG1CON1	RDBS	FDBS	—	—	POLD	POLC	POLB	POLA	00-- 0000	00-- 0000
695h	COG1RIS0	RIS<7:0>								0000 0000	0000 0000
696h	COG1RIS1	RIS15(2)	RIS<14:8>							0000 0000	0000 0000
697h	COG1RSIM0	RSIM<7:0>								0000 0000	0000 0000
698h	COG1RSIM1	RSIM15(2)	RSIM<14:8>							0000 0000	0000 0000
699h	COG1FIS0	FIS<7:0>								0000 0000	0000 0000
69Ah	COG1FIS1	FIS15(2)	FIS<14:8>							0000 0000	0000 0000
69Bh	COG1FSIM0	FSIM<7:0>								0000 0000	0000 0000
69Ch	COG1FSIM1	FSIM15(2)	FSIM<14:8>							0000 0000	0000 0000
69Dh	COG1ASD0	ASE	ARSEN	ASDBD<1:0>		ASDAC<1:0>		—	—	0001 01--	0001 01--
69Eh	COG1ASD1	AS7E	AS6E	AS5E	AS4E	AS3E	AS2E	AS1E	AS0E	0000 0000	0000 0000
69Fh	COG1STR	SDATD	SDATC	SDATB	SDATA	STRD	STRC	STRB	STRA	0000 0000	0000 0000

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: PIC16(L)F1768/9 only.
3: PIC16(L)F1764/5 only.
4: Unimplemented on PIC16LF1764/5/8/9.

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5.2.1.4 4x PLL

The oscillator module contains a 4x PLL that can be used with both external and internal clock sources to provide a system clock source. The input frequency for the 4x PLL must fall within specifications. See the PLL Clock Timing Specifications in Table 36-9.

The 4x PLL may be enabled for use by one of two methods:

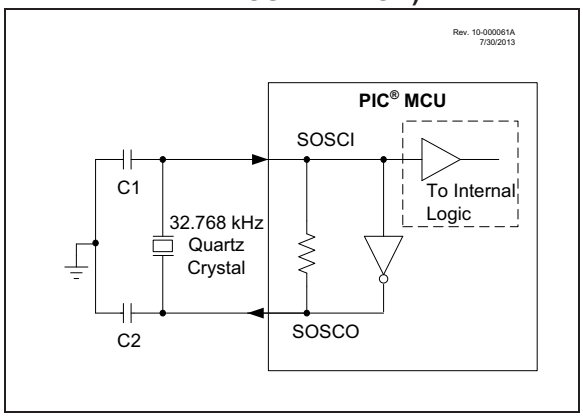
1. Program the PLLEN bit in the Configuration Words to a '1'.
2. Write the SPLLEN bit in the OSCCON register to a '1'. If the PLLEN bit in the Configuration Words is programmed to a '1', then the value of SPLLEN is ignored.

5.2.1.5 Secondary Oscillator

The secondary oscillator is a separate crystal oscillator that is associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the SOSCO and SOSCI device pins.

The secondary oscillator can be used as an alternate system clock source and can be selected during run time using clock switching. Refer to **Section 5.3 "Clock Switching"** for more information.

FIGURE 5-5: QUARTZ CRYSTAL OPERATION (SECONDARY OSCILLATOR)



Note 1: Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.

2: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

3: For oscillator design assistance, reference the following Microchip Application Notes:

- AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826)
- AN849, "*Basic PIC® Oscillator Design*" (DS00849)
- AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943)
- AN949, "*Making Your Oscillator Work*" (DS00949)
- TB097, "*Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS*" (DS91097)
- AN1288, "*Design Practices for Low-Power External Oscillators*" (DS01288)

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REGISTER 7-3: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
OSFIE	C2IE	C1IE	—	BCL1IE	C4IE(1)	C3IE(1)	CCP2IE(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit
- 1 = Enables the Oscillator fail interrupt
- 0 = Disables the Oscillator fail interrupt

bit 6 **C2IE:** Comparator C2 Interrupt Enable bit
- 1 = Enables the Comparator C2 interrupt
- 0 = Disables the Comparator C2 interrupt

bit 5 **C1IE:** Comparator C1 Interrupt Enable bit
- 1 = Enables the Comparator C1 interrupt
- 0 = Disables the Comparator C1 interrupt

bit 4 **Unimplemented:** Read as '0'

bit 3 **BCL1IE:** MSSP Bus Collision Interrupt Enable bit
- 1 = Enables the MSSP bus collision interrupt
- 0 = Disables the MSSP bus collision interrupt

bit 2 **C4IE:** TMR6 to T6PR Match Interrupt Enable bit(1)
- 1 = Enables the Comparator C4 interrupt
- 0 = Disables the Comparator C4 interrupt

bit 1 **C3IE:** TMR4 to T4PR Match Interrupt Enable bit(1)
- 1 = Enables the Comparator C3 interrupt
- 0 = Disables the Comparator C3 interrupt

bit 0 **CCP2IE:** CCP2 Interrupt Enable bit(1)
- 1 = Enables the CCP2 interrupt
- 0 = Disables the CCP2 interrupt

Note 1: PIC16(L)F1768/9 only.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

REGISTER 7-4: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PWM6IE(1)	PWM5IE	COG1IE	ZCDIE	COG2IE(1)	CLC3IE	CLC2IE	CLC1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **PWM6IE:** PWM6 Interrupt Enable bit(1)
- 1 = PWM6 interrupt is enabled
- 0 = PWM6 interrupt is disabled

bit 6 **PWM5IE:** PWM5 Interrupt Enable bit
- 1 = PWM5 interrupt is enabled
- 0 = PWM5 interrupt is disabled

bit 5 **COG1IE:** COG1 Auto-Shutdown Interrupt Enable bit
- 1 = COG1 interrupt is enabled
- 0 = COG1 interrupt is disabled

bit 4 **ZCDIE:** Zero-Cross Detection Interrupt Enable bit
- 1 = ZCD interrupt is enabled
- 0 = ZCD interrupt is disabled

bit 3 **COG2IE:** COG2 Auto-Shutdown Interrupt Enable bit(1)
- 1 = COG2 interrupt is enabled
- 0 = COG2 interrupt is disabled

bit 2 **CLC3IE:** CLC3 Interrupt Enable bit
- 1 = CLC3 interrupt is enabled
- 0 = CLC3 interrupt is disabled

bit 1 **CLC2IE:** CLC2 Interrupt Enable bit
- 1 = CLC2 interrupt is enabled
- 0 = CLC2 interrupt is disabled

bit 0 **CLC1IE:** CLC1 Interrupt Enable bit
- 1 = CLC1 interrupt is enabled
- 0 = CLC1 interrupt is disabled

Note 1: PIC16(L)F1768/9 only.

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

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11.6 Register Definitions: PORTC

REGISTER 11-17: PORTC: PORTC REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RC<7:0>(1,2)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **RC<7:0>**: PORTC General Purpose I/O Pin bits(1,2)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTC are actually written to corresponding LATC register. Reads from the PORTC register are the return of actual I/O pin values.
2: RC<7:6> are available on PIC16(L)F1768/9 only.

REGISTER 11-18: TRISC: PORTC TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISC<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **TRISC<7:0>:** PORTC Tri-State Control bits(1)
1 = PORTC pin is configured as an input (tri-stated)
0 = PORTC pin is configured as an output

Note 1: TRISC<7:6> are available on PIC16(L)F1768/9 only.

19.10 Analog Input Connection Considerations

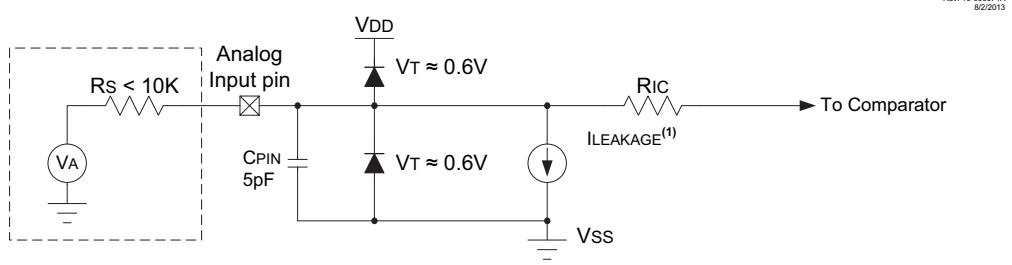
A simplified circuit for an analog input is shown in Figure 19-4. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of 10 kΩ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 19-4: ANALOG INPUT MODEL



Legend: CPIN = Input Capacitance
ILEAKAGE = Leakage Current at the pin due to various junctions
RIC = Interconnect Resistance
RS = Source Impedance
VA = Analog Voltage
VT = Threshold Voltage

Note 1: See I/O Ports in Table 36-4: I/O Ports.

25.10 Set-up Procedures

25.10.1 SETUP FOR PWM OPERATION USING PWMx OUTPUT PINS

The following steps should be taken when configuring the module for PWM operation using the PWMx output pins:

1. Disable the PWMx pin output driver(s) by setting the associated TRISx bit(s).
2. Clear the PWMxCON register.
3. Load the T2PR register with the PWM period value.
4. Load the PWMxDCH register and bits<7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
   - Configure the CKPSx bits of the T2CON register with the Timer2 prescale value.
   - Enable Timer2 by setting the ON bit of the T2CON register.
6. Enable the PWM output pin and wait until Timer2 overflows. TMR2IF bit of the PIR1 register is set. See Note below.
7. Enable the PWMx pin output driver(s) by clearing the associated TRISx bit(s) and setting the desired pin PPS control bits.
8. Configure the PWM module by loading the PWMxCON register with the appropriate values.

Note 1: In order to send a complete duty cycle and period on the first PWM output, the above steps must be followed in the order given. If it is not critical to start with a complete PWM signal, then move Step 8 to replace Step 4.

2: For operation with other peripherals only, disable PWMx pin outputs.

25.10.2 SETUP FOR PWM OPERATION TO OTHER DEVICE PERIPHERALS

The following steps should be taken when configuring the module for PWM operation to be used by other device peripherals:

1. Disable the PWMx pin output driver(s) by setting the associated TRISx bit(s).
2. Clear the PWMxCON register.
3. Load the T2PR register with the PWM period value.
4. Load the PWMxDCH register and bits<7:6> of the PWMxDCL register with the PWM duty cycle value.
5. Configure and start Timer2:
   - Clear the TMR2IF interrupt flag bit of the PIR1 register. See Note below.
   - Configure the CKPSx bits of the T2CON register with the Timer2 prescale value.
   - Enable Timer2 by setting the ON bit of the T2CON register.
6. Enable PWM output pin:
   - Wait until Timer2 overflows, TMR2IF bit of the PIR1 register is set. See Note below.
7. Configure the PWM module by loading the PWMxCON register with the appropriate values.

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then Step 6 may be ignored.

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27.11 Buffer Updates

Changes to the Phase, Dead-Band and Blanking Count registers need to occur simultaneously during COG operation to avoid unintended operation that may occur as a result of delays between each register write. This is accomplished with the LD bit of the COGxCON0 register and double-buffering of the Phase, Blanking and Dead-Band Count registers.

Before the COG module is enabled, writing the Count registers loads the count buffers without need of the LD bit. However, when the COG is enabled, the count buffer updates are suspended after writing the Count registers until after the LD bit is set. When the LD bit is set, the Phase, Dead-Band and Blanking register values are transferred to the corresponding buffers synchronous with COG operation. The LD bit is cleared by hardware when the transfer is complete.

27.12 Input and Output Pin Selection

The COG has one selection for an input from a device pin. That one input can be used as rising and falling event source or a Fault source. The COGxINPPS register is used to select the pin. Refer to registers, xxxPPS (Register 12-1) and RxyPPS (Register 12-2).

The Pin PPS Control registers are used to enable the COG outputs. Any combination of outputs to pins is possible including multiple pins for the same output. See the RxyPPS control register and **Section 12.2 "PPS Outputs"** for more details.

27.13 Operation During Sleep

The COG continues to operate in Sleep provided that the COG_clock, rising event, and falling event sources remain active.

The HFINTSOC remains active during Sleep when the COG is enabled and the HFINTOSC is selected as the COG_clock source.

27.14 Configuring the COG

The following steps illustrate how to properly configure the COG to ensure a synchronous start with the rising event input:

1. If a pin is to be used for the COG Fault or event input, use the COGxINPPS register to configure the desired pin.
2. Clear all ANSELx register bits associated with pins that are used for COG functions.
3. Ensure that the TRISx control bits corresponding to the COG outputs to be used are set so that all are configured as inputs. The COG module will enable the output drivers as needed later.
4. Clear the EN bit, if not already cleared.
5. Set desired dead-band times with the COGxDBR and COGxDBF registers, and select the source with the RDBS and FDBS bits of the COGxCON1 register.
6. Set desired blanking times with the COGxBLKR and COGxBLKF registers.
7. Set desired phase delay with the COGxPHR and COGxPHF registers.
8. Select the desired shutdown sources with the COGxASD1 register.
9. Setup the following controls in the COGxASD0 Auto-Shutdown register:
   - Select both output override controls to the desired levels (this is necessary, even if not using auto-shutdown because start-up will be from a shutdown state).
   - Set the ASE bit and clear the ARSEN bit.
10. Select the desired rising and falling event sources with the COGxRIS0, COGxRIS1, COGxFIS0 and COGxFIS1 registers.
11. Select the desired Rising and Falling Event modes with the COGxRSIM0, COGxRSIMI1, COGxFSIM0 and COGxFSIM1 registers.
12. Configure the following controls in the COGxCON1 register:
    - Set the polarity for each output
    - Select the desired dead-band timing sources
13. Configure the following controls in the COGxCON0 register:
    - Set the desired operating mode
    - Select the desired clock source
14. If one of the Steering modes is selected, then configure the following controls in the COGxSTR register:
    - Set the steering bits of the outputs to be used.
    - Set the desired static levels.
15. Set the EN bit.
16. Set the pin PPS controls to direct the COG outputs to the desired pins.
17. If auto-restart is to be used, set the ARSEN bit and the ASE will be cleared automatically; otherwise, clear the ASE bit to start the COG.

REGISTER 27-5: COGxRSIM0: COGx RISING EVENT SOURCE INPUT MODE REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
RSIM7	RSIM6	RSIM5	RSIM4	RSIM3	RSIM2	RSIM1	RSIM0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **RSIM7:** COGx Rising Event Input Source 7 Mode bit

RIS7 = 1:

1 = PWM3 output low-to-high transition will cause a rising event after rising event phase delay
0 = PWM3 output high level will cause an immediate rising event

RIS7 = 0:

PWM3 output has no effect on rising event.

bit 6 **RSIM6:** COGx Rising Event Input Source 6 Mode bit

RIS6 = 1:

1 = CCP2 output low-to-high transition will cause a rising event after rising event phase delay
0 = CCP2 output high level will cause an immediate rising event

RIS6 = 0:

CCP2 output has no effect on rising event.

bit 5 **RSIM5:** COGx Rising Event Input Source 5 Mode bit

RIS5 = 1:

1 = CCP1 output low-to-high transition will cause a rising event after rising event phase delay
0 = CCP1 output high level will cause an immediate rising event

RIS5 = 0:

CCP1 output has no effect on rising event.

bit 4 **RSIM4:** COGx Rising Event Input Source 4 Mode bit

RIS4 = 1:

1 = Comparator 4 output low-to-high transition will cause a rising event after rising event phase delay
0 = Comparator 4 output high level will cause an immediate rising event

RIS4 = 0:

Comparator 4 has no effect on rising event.

bit 3 **RSIM3:** COGx Rising Event Input Source 3 Mode bit

RIS3 = 1:

1 = Comparator 3 output low-to-high transition will cause a rising event after rising event phase delay
0 = Comparator 3 output high level will cause an immediate rising event

RIS3 = 0:

Comparator 3 output has no effect on rising event.

bit 2 **RSIM2:** COGx Rising Event Input Source 2 Mode bit

RIS2 = 1:

1 = Comparator 2 output low-to-high transition will cause a rising event after rising event phase delay
0 = Comparator 2 output high level will cause an immediate rising event

RIS2 = 0:

Comparator 2 has no effect on rising event.

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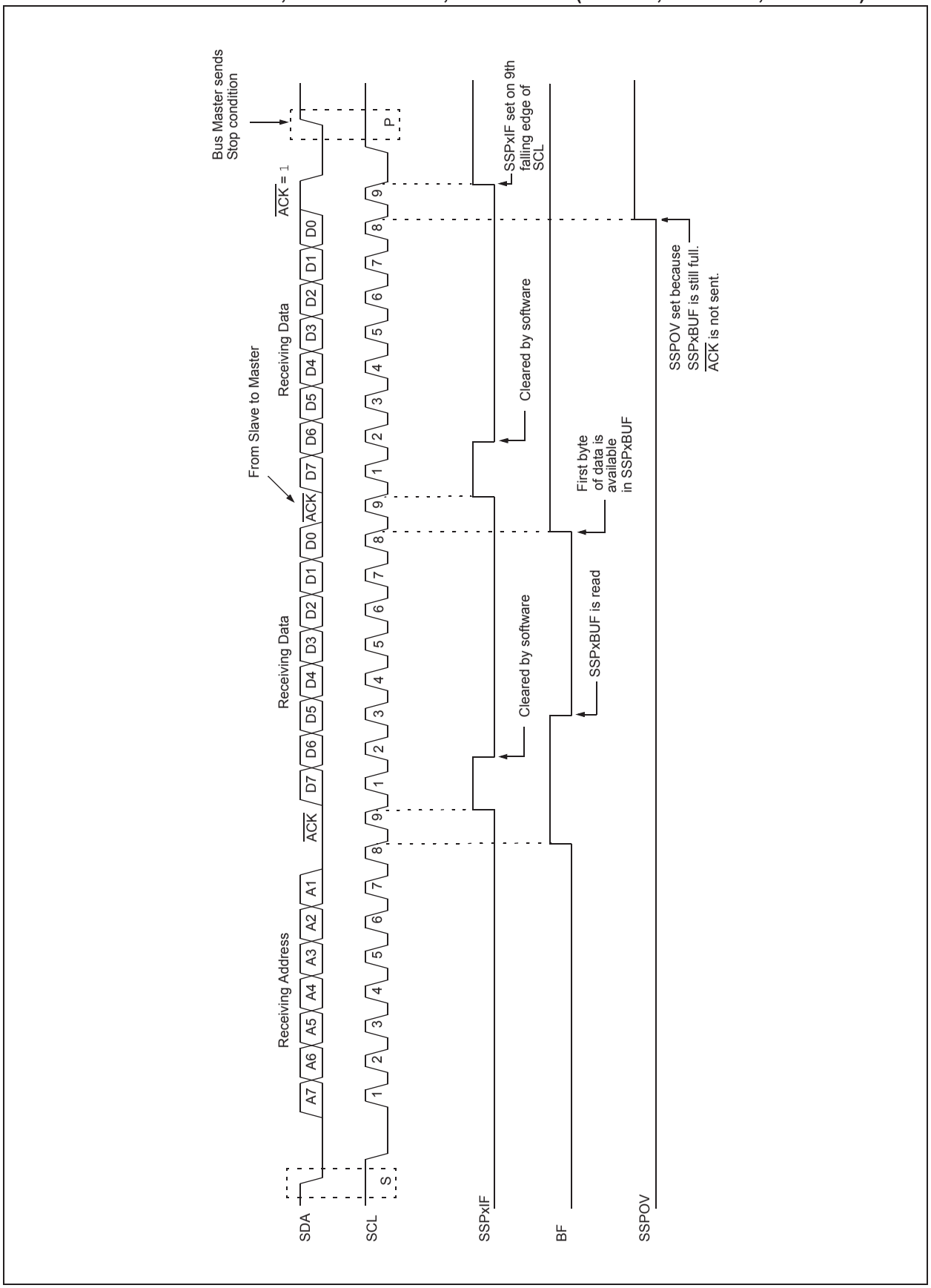
FIGURE 32-14: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)



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32.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

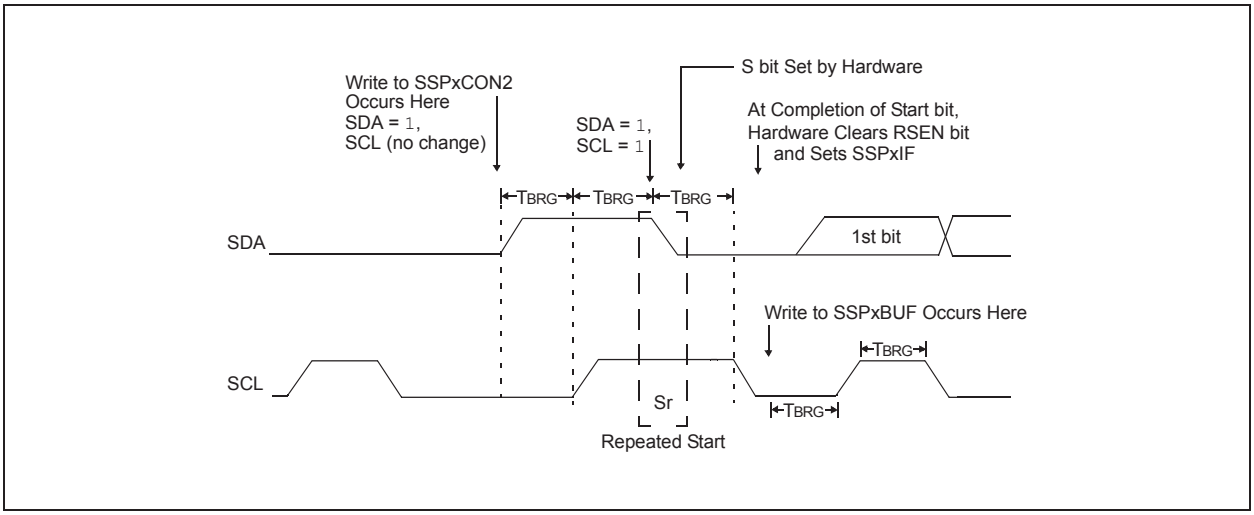
A Repeated Start condition (Figure 32-27) occurs when the RSEN bit of the SSPxCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPxCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPxSTAT register will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

2: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 32-27: REPEATED START CONDITION WAVEFORM



REGISTER 32-2: SSP1CON1: MSSP CONTROL REGISTER 1 (CONTINUED)

bit 4 **CKP:** Clock Polarity Select bit

In SPI mode:
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level

In I^2C Slave mode:
SCL release control.
1 = Enables clock
0 = Holds clock low (clock stretch), used to ensure data setup time

In I^2C Master mode:
Unused in this mode.

bit 3-0 **SSPM<3:0>:** Synchronous Serial Port Mode Select bits

1111 = I^2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled
1110 = I^2C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1101 = Reserved
1100 = Reserved
1011 = I^2C Firmware Controlled Master mode (slave Idle)
1010 = SPI Master mode, clock = FOSC/(4 * (SSP1ADD + 1))**(5)**
1001 = Reserved
1000 = I^2C Master mode, clock = FOSC/(4 * (SSP1ADD + 1))**(4)**
0111 = I^2C Slave mode, 10-bit address
0110 = I^2C Slave mode, 7-bit address
0101 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control is disabled, $\overline{SS}$ can be used as I/O pin
0100 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control is enabled
0011 = SPI Master mode, clock = T2_match/2
0010 = SPI Master mode, clock = FOSC/64
0001 = SPI Master mode, clock = FOSC/16
0000 = SPI Master mode, clock = FOSC/4

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPxBUF register.

2: When enabled, these pins must be properly configured as input or output. Use SSPSSPPS, SSPCLKPPS, SSPDATPPS and RxyPPS to select the pins.

3: When enabled, the SDA and SCL pins must be configured as inputs. Use SSPCLKPPS, SSPDATPPS and RxyPPS to select the pins.

4: SSPxADD values of 0, 1 or 2 are not supported for I^2C mode.

5: SSPxADD value of 0 is not supported; use SSPM<3:0> = 0000 instead.

REGISTER 32-4: SSP1CON3: MSSP CONTROL REGISTER 3

R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACKTIM(3)	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **ACKTIM:** Acknowledge Time Status bit (I^2C slave modes only)(3)
1 = Indicates the I^2C bus is in an Acknowledge sequence, set on eighth falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 6 **PCIE**: Stop Condition Interrupt Enable bit (I^2C slave modes only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled(2)

bit 5 **SCIE**: Start Condition Interrupt Enable bit (I^2C slave modes only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled(2)

bit 4 **BOEN:** Buffer Overwrite Enable bit
In SPI Slave mode:(1)
1 = SSPxBUF updates every time that a new data byte is shifted in, ignoring the BF bit
0 = If new byte is received with BF bit of the SSPxSTAT register already set, the SSPOV bit of the SSPxCON1 register is set and the buffer is not updated
In I^2C Master mode and SPI Master mode:
This bit is ignored.
In I^2C Slave mode:
1 = SSPxBUF is updated and $\overline{ACK}$ is generated for a received address/data byte, ignoring the state of the SSPOV bit only if the BF bit = 0
0 = SSPxBUF is only updated when SSPOV is clear

bit 3 **SDAHT:** SDA Hold Time Selection bit (I^2C mode only)
1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL
0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCL, SDA is sampled low when the module is outputting a high state, the BCL1IF bit of the PIR2 register is set and the bus goes Idle
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the eighth falling edge of SCL for a matching received address byte; CKP bit of the SSPxCON1 register will be cleared and the SCL will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the eighth falling edge of SCL for a received data byte; slave hardware clears the CKP bit of the SSPxCON1 register and SCL is held low
0 = Data holding is disabled

Note 1: For daisy-chained SPI operation; allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSP1BUF.
2: This bit has no effect in Slave modes in which Start and Stop condition detection is explicitly listed as enabled.
3: The ACKTIM status bit is only active when the AHEN bit or DHEN bit is set.

33.1.2.4 Receive Framing Error

Each character in the receive FIFO buffer has a corresponding framing error status bit. A framing error indicates that a Stop bit was not seen at the expected time. The framing error status is accessed via the FERR bit of the RCxSTA register. The FERR bit represents the status of the top unread character in the receive FIFO. Therefore, the FERR bit must be read before reading the RCxREG.

The FERR bit is read-only and only applies to the top unread character in the receive FIFO. A framing error (FERR = 1) does not preclude reception of additional characters. It is not necessary to clear the FERR bit. Reading the next character from the FIFO buffer will advance the FIFO to the next character and the next corresponding framing error.

The FERR bit can be forced clear by clearing the SPEN bit of the RCxSTA register which resets the EUSART. Clearing the CREN bit of the RCxSTA register does not affect the FERR bit. A framing error by itself does not generate an interrupt.

Note:	If all receive characters in the receive FIFO have framing errors, repeated reads of the RCxREG will not clear the FERR bit.

33.1.2.5 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before the FIFO is accessed. When this happens, the OERR bit of the RCxSTA register is set. The characters already in the FIFO buffer can be read, but no additional characters will be received until the error is cleared. The error must be cleared by either clearing the CREN bit of the RCxSTA register or by resetting the EUSART by clearing the SPEN bit of the RCxSTA register.

33.1.2.6 Receiving 9-Bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCxSTA register is set, the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCxSTA register is the ninth and Most Significant data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCxREG.

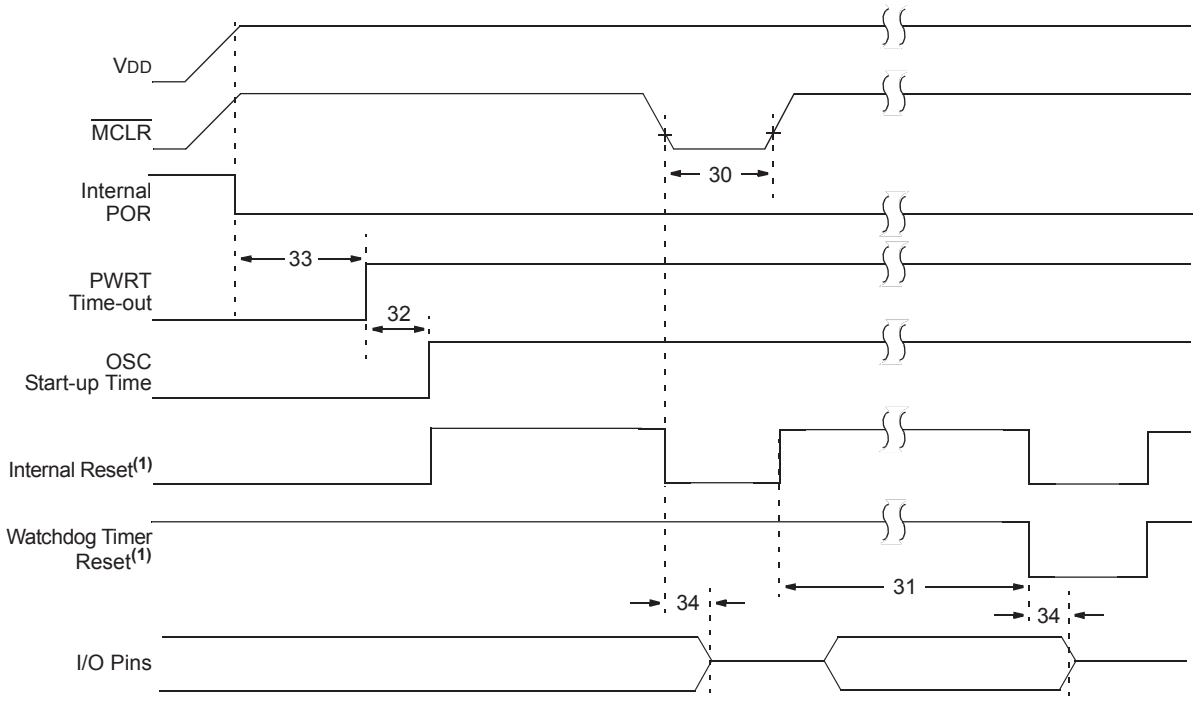
33.1.2.7 Address Detection

A special Address Detection mode is available for use when multiple receivers share the same transmission line, such as in RS-485 systems. Address detection is enabled by setting the ADDEN bit of the RCxSTA register.

Address detection requires 9-bit character reception. When address detection is enabled, only characters with the ninth data bit set will be transferred to the receive FIFO buffer, thereby setting the RCIF interrupt bit. All other characters will be ignored.

Upon receiving an address character, user software determines if the address matches its own. Upon address match, user software must disable address detection by clearing the ADDEN bit before the next Stop bit occurs. When user software detects the end of the message, determined by the message protocol used, software places the receiver back into the Address Detection mode by setting the ADDEN bit.

FIGURE 36-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Asserted low.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

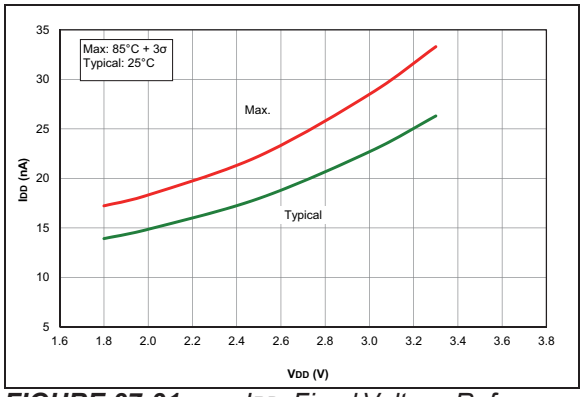


FIGURE 37-31: *IPD, Fixed Voltage Reference (FVR), PIC16LF1764/5/8/9 Only.*

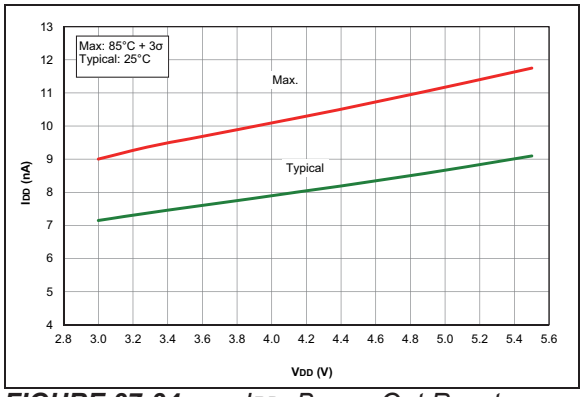


FIGURE 37-34: *IPD, Brown-Out Reset (BOR), BORV = 1, PIC16F1764/5/8/9 Only.*

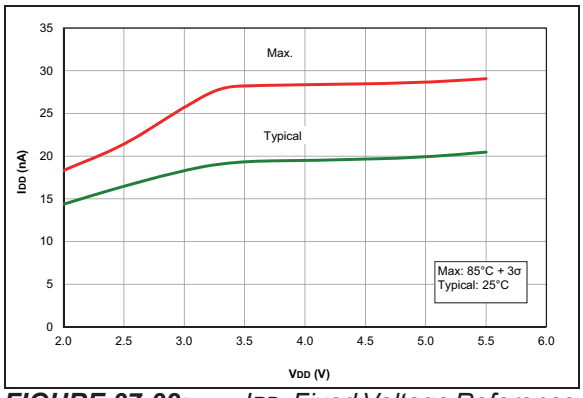


FIGURE 37-32: *IPD, Fixed Voltage Reference (FVR), PIC16F1764/5/8/9 Only.*

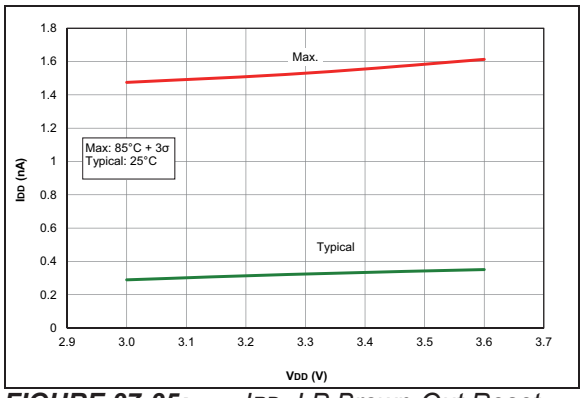


FIGURE 37-35: *IPD, LP Brown-Out Reset (LPBOR = 0), PIC16LF1764/5/8/9 Only.*

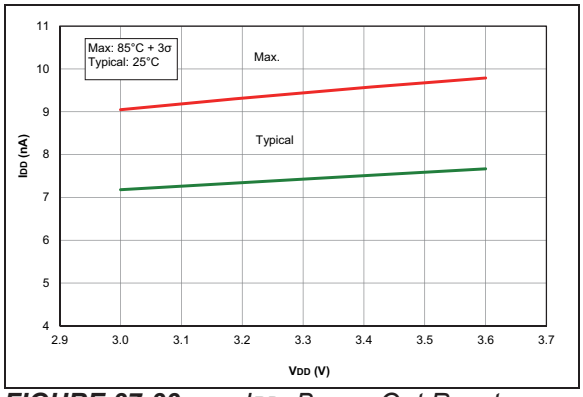


FIGURE 37-33: *IPD, Brown-Out Reset (BOR), BORV = 1, PIC16LF1764/5/8/9 Only.*

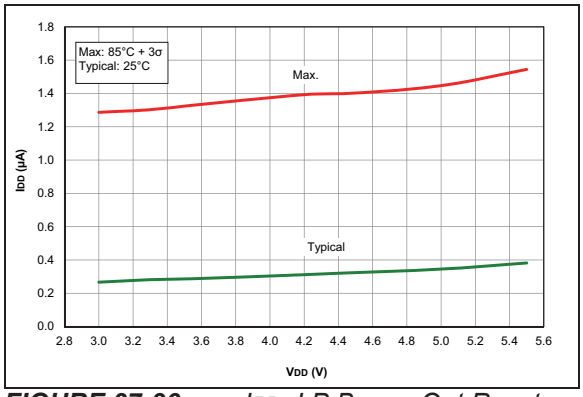


FIGURE 37-36: *IPD, LP Brown-Out Reset (LPBOR = 0), PIC16F1764/5/8/9 Only.*