Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1768-i-ss

2.1 Automatic Interrupt Context Saving

During interrupts, certain registers are automatically saved in shadow registers and restored when returning from the interrupt. This saves stack space and user code. See **Section 7.5 "Automatic Context Saving"** for more information.

2.2 16-Level Stack with Overflow and Underflow

These devices have a hardware stack memory 15 bits wide and 16 words deep. A Stack Overflow or Underflow will set the appropriate bit (STKOVF or STKUNF) in the PCON register, and if enabled, will cause a Software Reset. See **Section 3.5 "Stack"** for more details.

2.3 File Select Registers

There are two 16-bit File Select Registers (FSRs). FSRs can access all file registers and program memory, which allows one Data Pointer for all memory. When an FSRn points to program memory, there is one additional instruction cycle in instructions using INDFn to allow the data to be fetched. General purpose memory can now also be addressed linearly, providing the ability to access contiguous data larger than 80 bytes. There are also new instructions to support the FSRs. See **Section 3.6 "Indirect Addressing"** for more details.

2.4 Instruction Set

There are 49 instructions for the enhanced mid-range CPU to support the features of the CPU. See **Section 35.0 "Instruction Set Summary"** for more details.

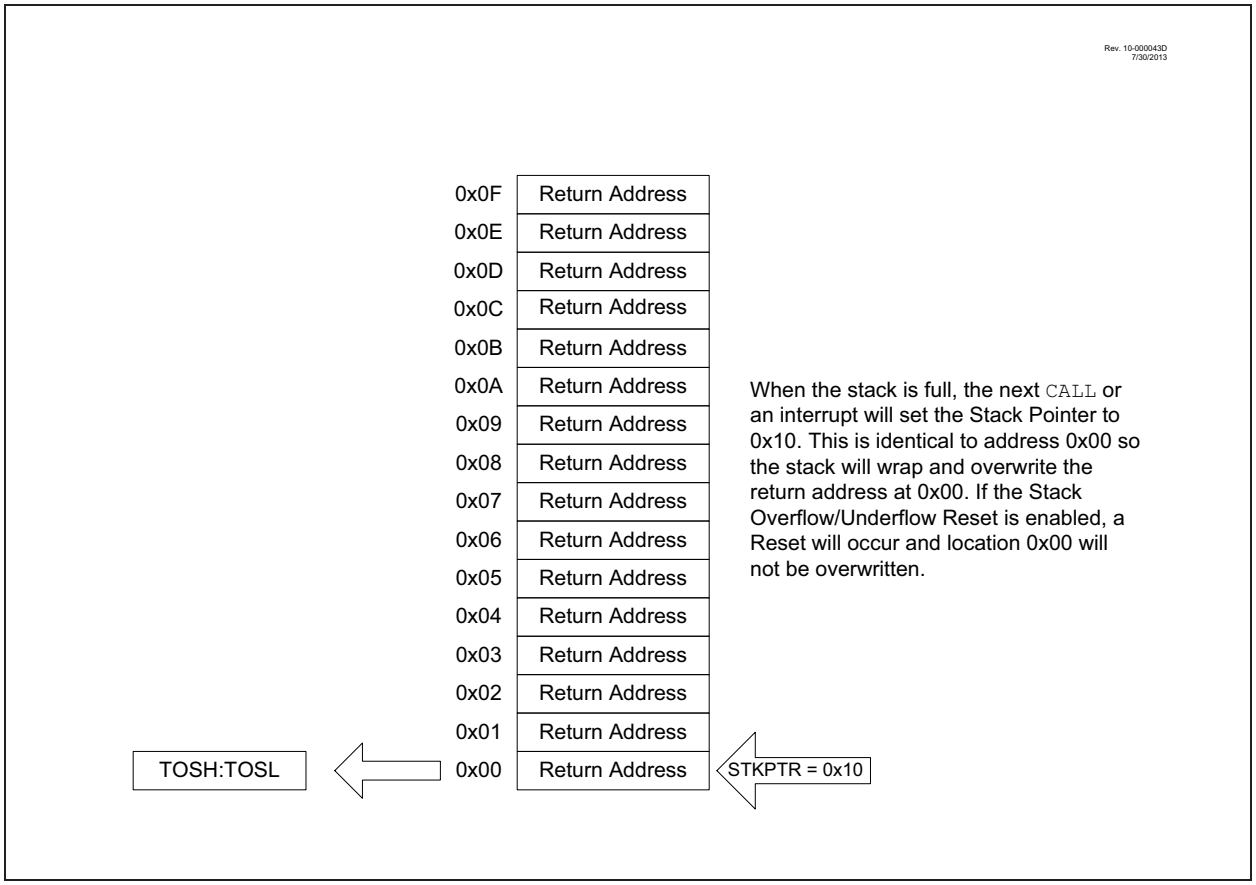
TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 8											
40Ch — 40Dh	—	Unimplemented								—	—
40Eh	HIDRVC	—	—	HIDC<5:4>		—	—	—	—	--00 ----	--00 ----
40Fh — 412h	—	Unimplemented								—	—
413h	T4TMR	Holding Register for the 8-Bit TMR4 Register								0000 0000	0000 0000
413h	T4PR	TMR4 Period Register								1111 1111	1111 1111
415h	T4CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
416h	T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
417h	T4CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
418h	T4RST	—	—	—	—	RSEL<3:0>				---- 0000	---- 0000
419h	—	Unimplemented								—	—
41Ah	T6TMR	Holding Register for the 8-Bit TMR4 Register								0000 0000	0000 0000
41Bh	T6PR	TMR4 Period Register								1111 1111	1111 1111
41Ch	T6CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
41Dh	T6HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
41Eh	T6CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
41Fh	T6RST	—	—	—	—	RSEL<3:0>				---- 0000	---- 0000
Bank 9											
48Ch to 492h	—	Unimplemented								—	—
493h	TMR3L	Holding Register for the Least Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
494h	TMR3H	Holding Register for the Most Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
495h	T3CON	CS<1:0>		CKPS<1:0>		OSCEN	$\overline{\text{SYNC}}$	—	ON	0000 00-0	uuuu uu-u
496h	T3GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	GSS<1:0>		0000 0x00	uuuu uxuu
497h to 499h	—	Unimplemented								—	—
49Ah	TMR5L	Holding Register for the Least Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
49Bh	TMR5H	Holding Register for the Most Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
49Ch	T5CON	CS<1:0>		CKPS<1:0>		OSCEN	$\overline{\text{SYNC}}$	—	ON	0000 00-0	uuuu uu-u
49Dh	T5GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	GSS<1:0>		0000 0x00	uuuu uxuu
49Eh to 49Fh	—	Unimplemented								—	—

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: PIC16(L)F1768/9 only.
3: PIC16(L)F1764/5 only.
4: Unimplemented on PIC16LF1764/5/8/9.

FIGURE 3-7: ACCESSING THE STACK EXAMPLE 4



3.5.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Words is programmed to '1', the device will be reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

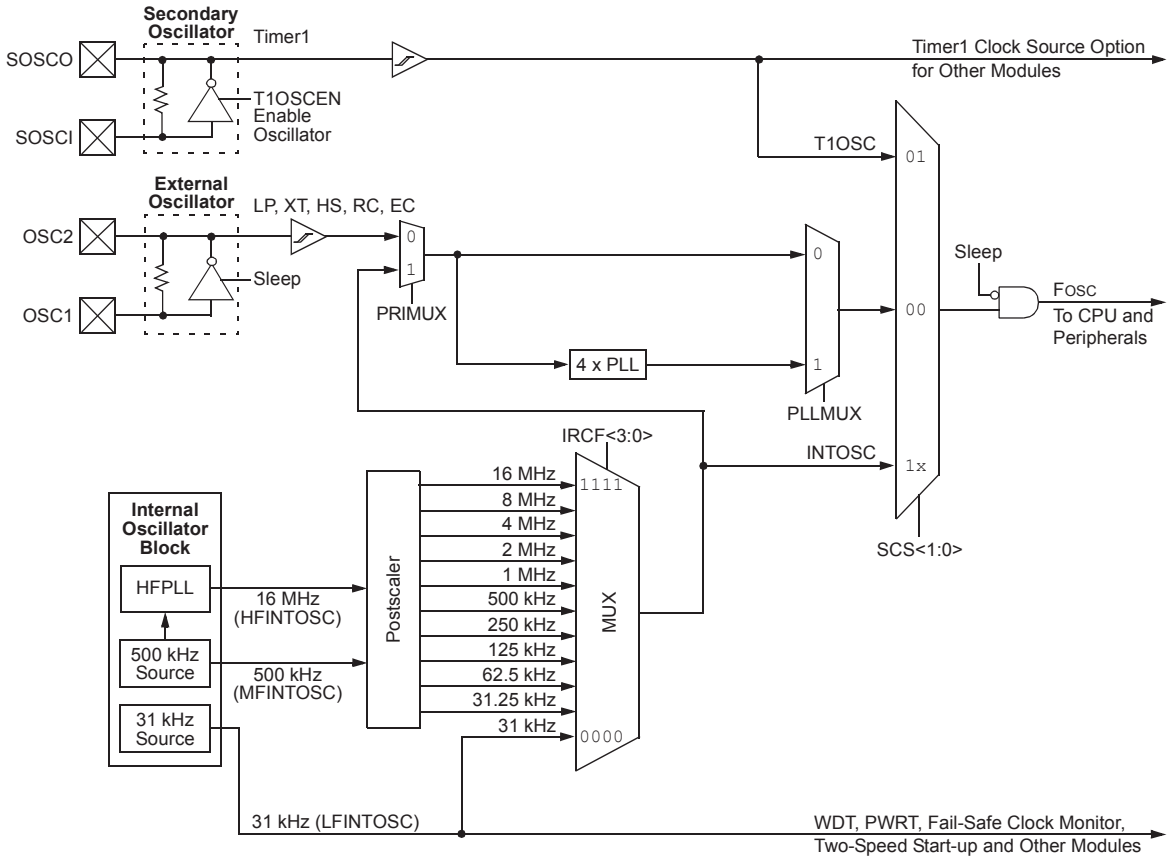
3.6 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSRs). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair, FSRnH and FSRnL.

The FSRn registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- Linear Data Memory
- Program Flash Memory

FIGURE 5-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



Inputs				Outputs	
SCS<1:0>	FOSC<2:0>	PLLEN or SPLLEN	IRCF<3:0>	PRIMUX	PLLMUX
= 00	= 100	0	xxxx	1	0
		1	= 1110	1	1
			≠ 1110	1	0
	≠ 100	0	xxxx	0	0
		1	xxxx	0	1
≠ 00	x	x	xxxx	x	x

6.2.1 BOR IS ALWAYS ON

When the BOREN<1:0> bits of the Configuration Words are programmed to '11', the BOR is always on. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is active during Sleep. The BOR does not delay wake-up from Sleep.

6.2.2 BOR IS OFF IN SLEEP

When the BORENx bits of the Configuration Words are programmed to '10', the BOR is on, except in Sleep. The device start-up will be delayed until the BOR is ready and VDD is higher than the BOR threshold.

BOR protection is not active during Sleep. The device wake-up will be delayed until the BOR is ready.

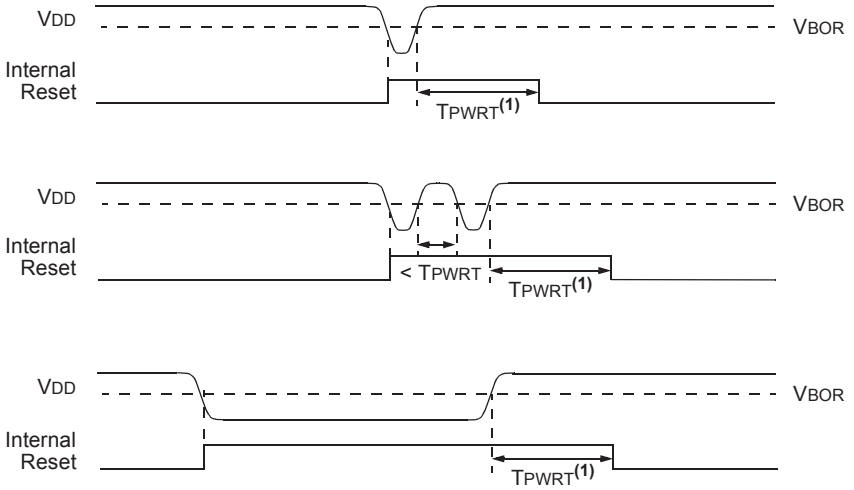
6.2.3 BOR CONTROLLED BY SOFTWARE

When the BORENx bits of the Configuration Words are programmed to '01', the BOR is controlled by the SBOREN bit of the BORCON register. The device start-up is not delayed by the BOR ready condition or the VDD level.

BOR protection begins as soon as the BOR circuit is ready. The status of the BOR circuit is reflected in the BORRDY bit of the BORCON register.

BOR protection is unchanged by Sleep.

FIGURE 6-2: BROWN-OUT SITUATIONS



Note 1: TPWRT delay only if the $\overline{\text{PWRTE}}$ bit is programmed to '0'.

REGISTER 7-7: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PWM6IF(1)	PWM5IF	COG1IF	ZCDIF	COG2IF(1)	CLC3IF	CLC2IF	CLC1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **PWM6IF:** PWM6 Interrupt Flag bit(1)
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 6 **PWM5IF:** PWM5 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 5 **COG1IF:** COG1 Auto-Shutdown Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 4 **ZCDIF:** Zero-Cross Detection Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 3 **COG2IF:** COG2 Auto-Shutdown Interrupt Flag bit(1)
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 2 **CLC3IF:** CLC3 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 1 **CLC2IF:** CLC2 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 0 **CLC1IF:** CLC1 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

Note 1: PIC16(L)F1768/9 only.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 10-5: PMCON1: PROGRAM MEMORY CONTROL 1 REGISTER

U-1	R/W-0/0	R/W-0/0	R/W/HC-0/0	R/W/HC-x/q(2)	R/W-0/0	R/S/HC-0/0	R/S/HC-0/0
—(1)	CFGS	LWLO(3)	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
S = Settable Only bit	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Hardware Clearable bit

bit 7 **Unimplemented:** Read as '1'

bit 6 **CFGS:** Configuration Select bit
- 1 = Accesses Configuration, User ID and Device ID registers
- 0 = Accesses Flash program memory

bit 5 **LWLO:** Load Write Latches Only bit(3)
- 1 = Only the addressed program memory write latch is loaded/updated on the next WR command
- 0 = The addressed program memory write latch is loaded/updated and a write of all program memory write latches will be initiated on the next WR command

bit 4 **FREE:** Program Flash Erase Enable bit
- 1 = Performs an erase operation on the next WR command (hardware cleared upon completion)
- 0 = Performs a write operation on the next WR command

bit 3 **WRERR:** Program/Erase Error Flag bit(2)
- 1 = Condition indicates an improper program or erase sequence attempt, or termination (bit is set automatically on any set attempt (writes '1') of the WR bit)
- 0 = The program or erase operation completed normally

bit 2 **WREN:** Program/Erase Enable bit
- 1 = Allows program/erase cycles
- 0 = Inhibits programming/erasing of program Flash

bit 1 **WR:** Write Control bit
- 1 = Initiates a Flash program/erase operation
  The operation is self-timed and the bit is cleared by hardware once operation is complete.
  The WR bit can only be set (not cleared) in software.
- 0 = Program/erase operation to the Flash is complete and inactive

bit 0 **RD:** Read Control bit
- 1 = Initiates a program Flash read
  Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software.
- 0 = Does not initiate a program Flash read

Note 1: Unimplemented bit, read as '1'.
2: The WRERR bit is automatically set by hardware when a program memory write or erase operation is started (WR = 1).
3: The LWLO bit is ignored during a program memory erase operation (FREE = 1).

REGISTER 13-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS = Hardware Settable bit

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **IOCAF<5:0>:** Interrupt-On-Change PORTA Flag bits

1 = An enabled change was detected on the associated pin
Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.

0 = No change was detected or the user cleared the detected change

REGISTER 13-4: IOCBP: INTERRUPT-ON-CHANGE PORTB POSITIVE EDGE REGISTER(1)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
IOCBP<7:4>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **IOCBP<7:4>:** Interrupt-On-Change PORTB Positive Edge Enable bits

1 = Interrupt-On-Change is enabled on the pin for a positive going edge; IOCBFx bit and IOCIF flag will be set upon edge detection

0 = Interrupt-On-Change is disabled for the associated pin

bit 3-0 **Unimplemented:** Read as ‘0’

Note 1: PIC16(L)F1768/9 only.

FIGURE 14-1: VOLTAGE REFERENCE BLOCK DIAGRAM

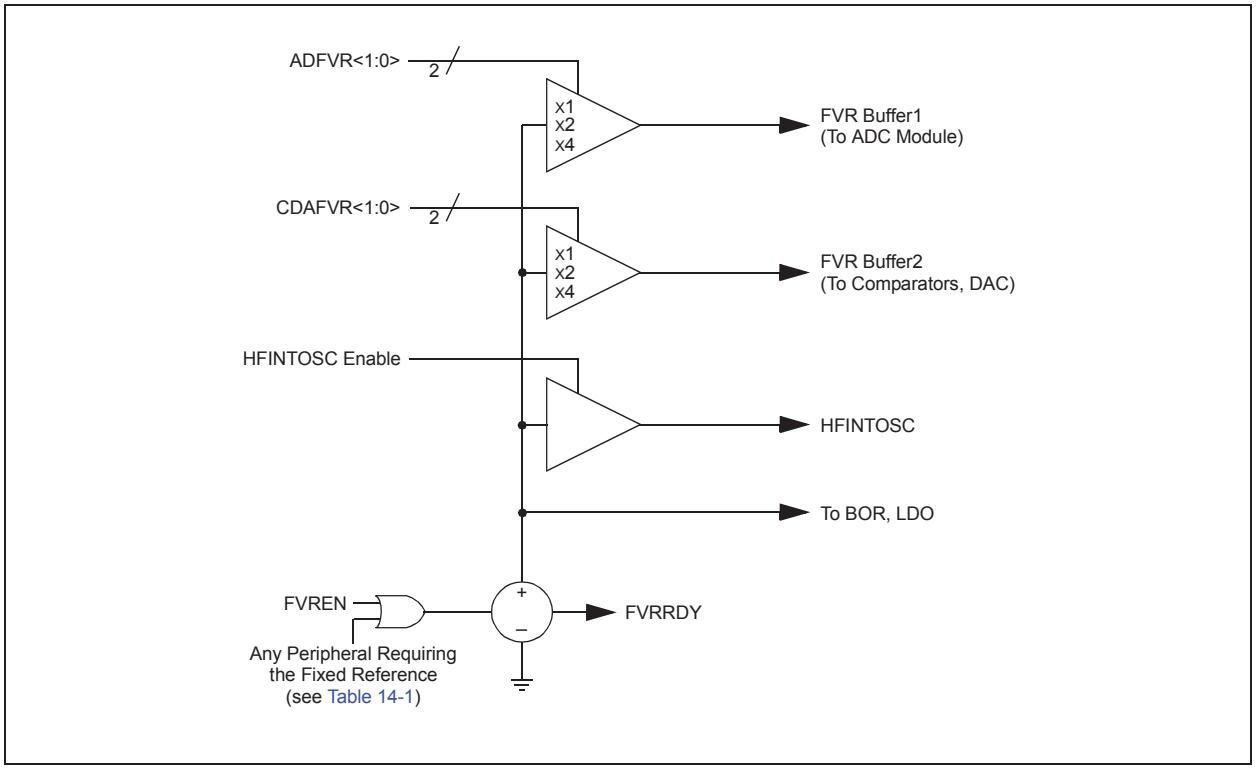


TABLE 14-1: PERIPHERALS REQUIRING THE FIXED VOLTAGE REFERENCE (FVR)

Peripheral	Conditions	Description
HFINTOSC	FOSC<2:0> = 100 and IRCF<3:0> ≠ 000x	INTOSC is active and device is not in Sleep
BOR	BOREN<1:0> = 11	BOR is always enabled
	BOREN<1:0> = 10 and BORFS = 1	BOR is disabled in Sleep mode, BOR fast start is enabled
	BOREN<1:0> = 01 and BORFS = 1	BOR under software control, BOR fast start is enabled
LDO	All PIC16F1764/5/8/9 devices when VREGPM = 1 and not in Sleep	The device runs off of the ULP regulator when in Sleep mode

21.0 TIMER0 MODULE

The Timer0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter register (TMR0)
- 8-bit prescaler (independent of Watchdog Timer)
- Programmable internal or external clock source
- Programmable external clock edge selection
- Interrupt-on-overflow
- TMR0 can be used to gate Timer1

Figure 21-1 is a block diagram of the Timer0 module.

21.1 Timer0 Operation

The Timer0 module can be used as either an 8-bit timer or an 8-bit counter.

21.1.1 8-BIT TIMER MODE

The Timer0 module will increment every instruction cycle if used without a prescaler. 8-Bit Timer mode is selected by clearing the TMR0CS bit of the OPTION_REG register.

When TMR0 is written, the increment is inhibited for two instruction cycles immediately following the write.

Note:	The value written to the TMR0 register can be adjusted, in order to account for the two instruction cycle delay when TMR0 is written.

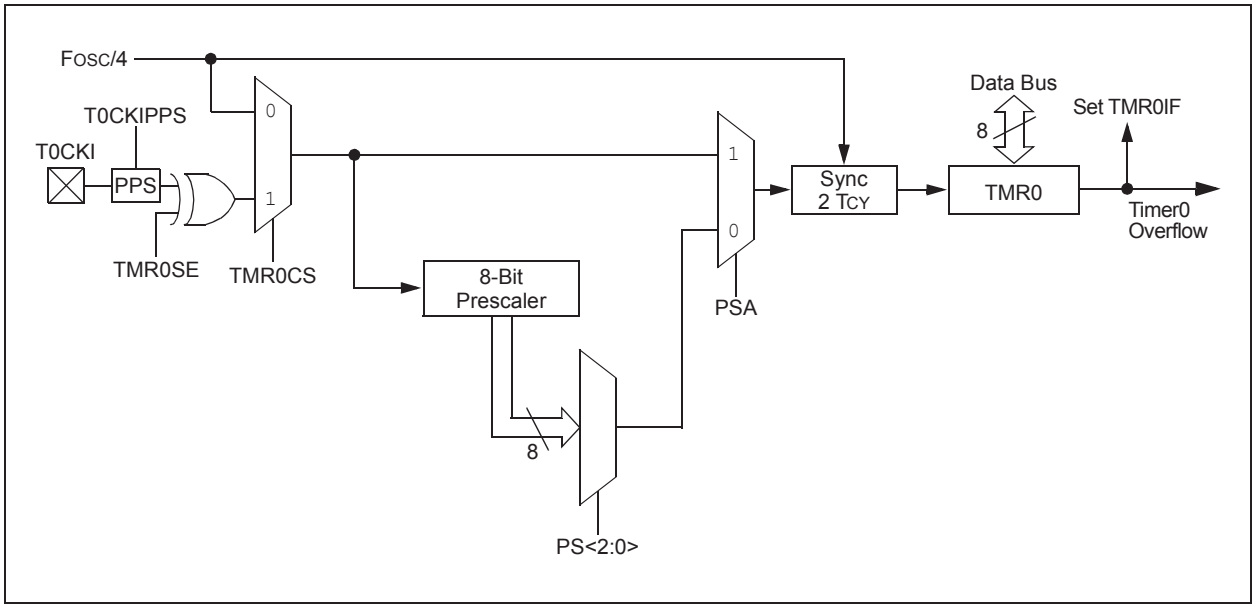
21.1.2 8-BIT COUNTER MODE

In 8-Bit Counter mode, the Timer0 module will increment on every rising or falling edge of the T0CKI pin.

8-Bit Counter mode using the T0CKI pin is selected by setting the TMR0CS bit in the OPTION_REG register to '1'.

The rising or falling transition of the incrementing edge for either input source is determined by the TMR0SE bit in the OPTION_REG register.

FIGURE 21-1: BLOCK DIAGRAM OF TIMER0



REGISTER 26-11: PWMxPRH: PWMx PERIOD COUNT HIGH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PR<15:8>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **PR<15:8>**: PWMx Period High bits
Upper eight bits of PWMx period count.

REGISTER 26-12: PWMxPRL: PWMx PERIOD COUNT LOW REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
PR<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **PR<7:0>**: PWMx Period Low bits
Lower eight bits of PWMx period count.

FIGURE 27-15: AUTO-SHUTDOWN WAVEFORM – CCP1 AS RISING AND FALLING EVENT INPUT SOURCE

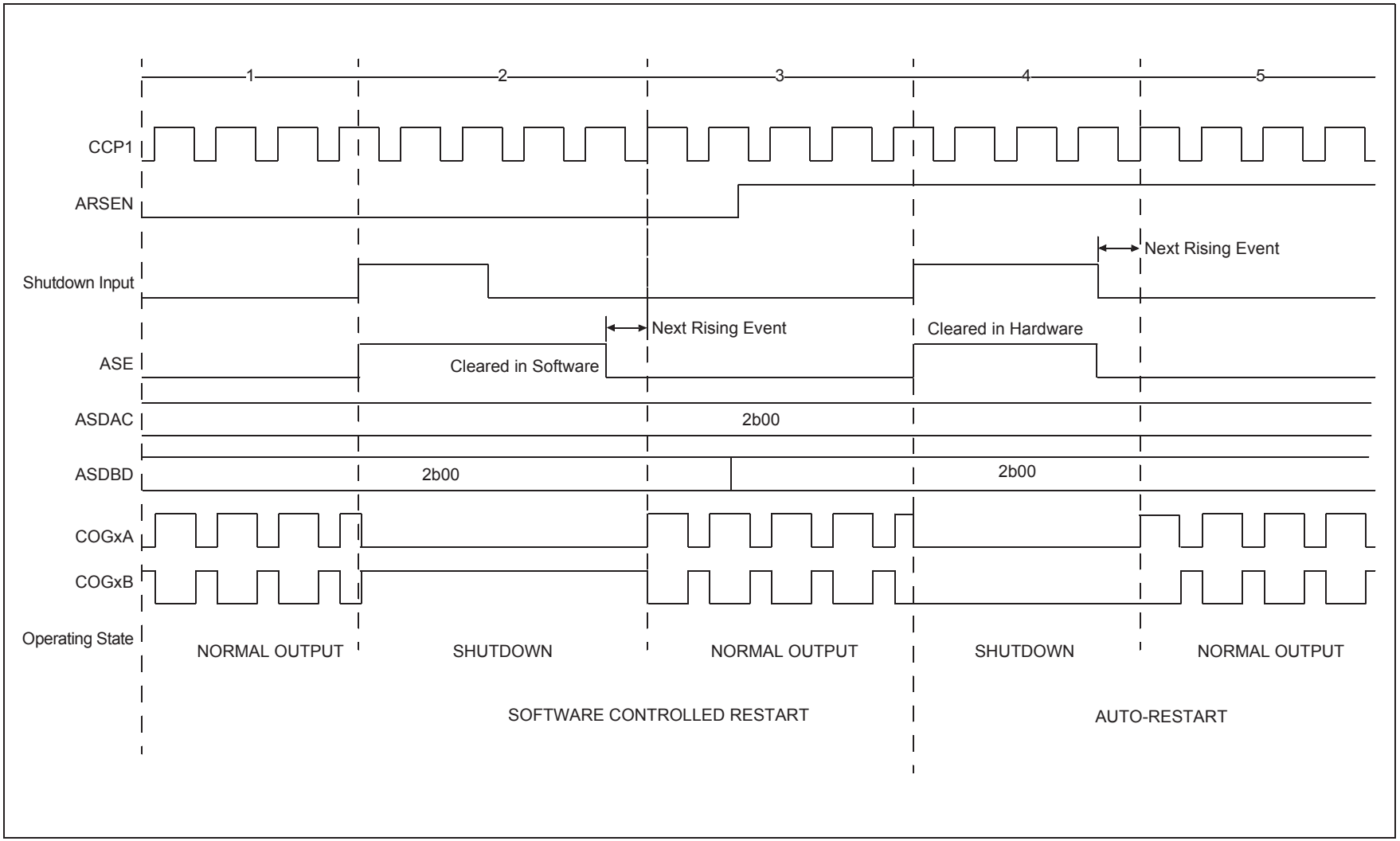


FIGURE 32-15: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)

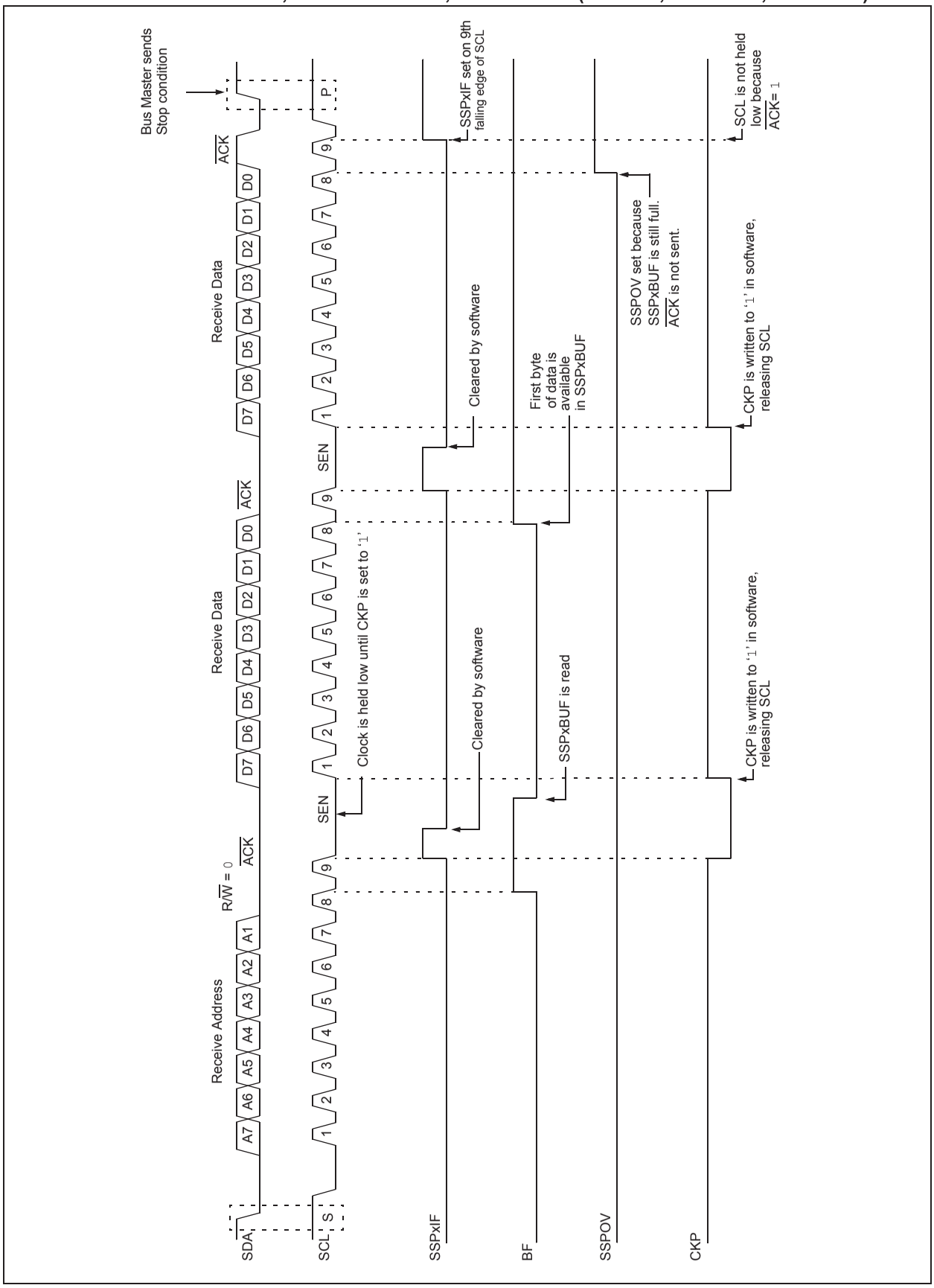
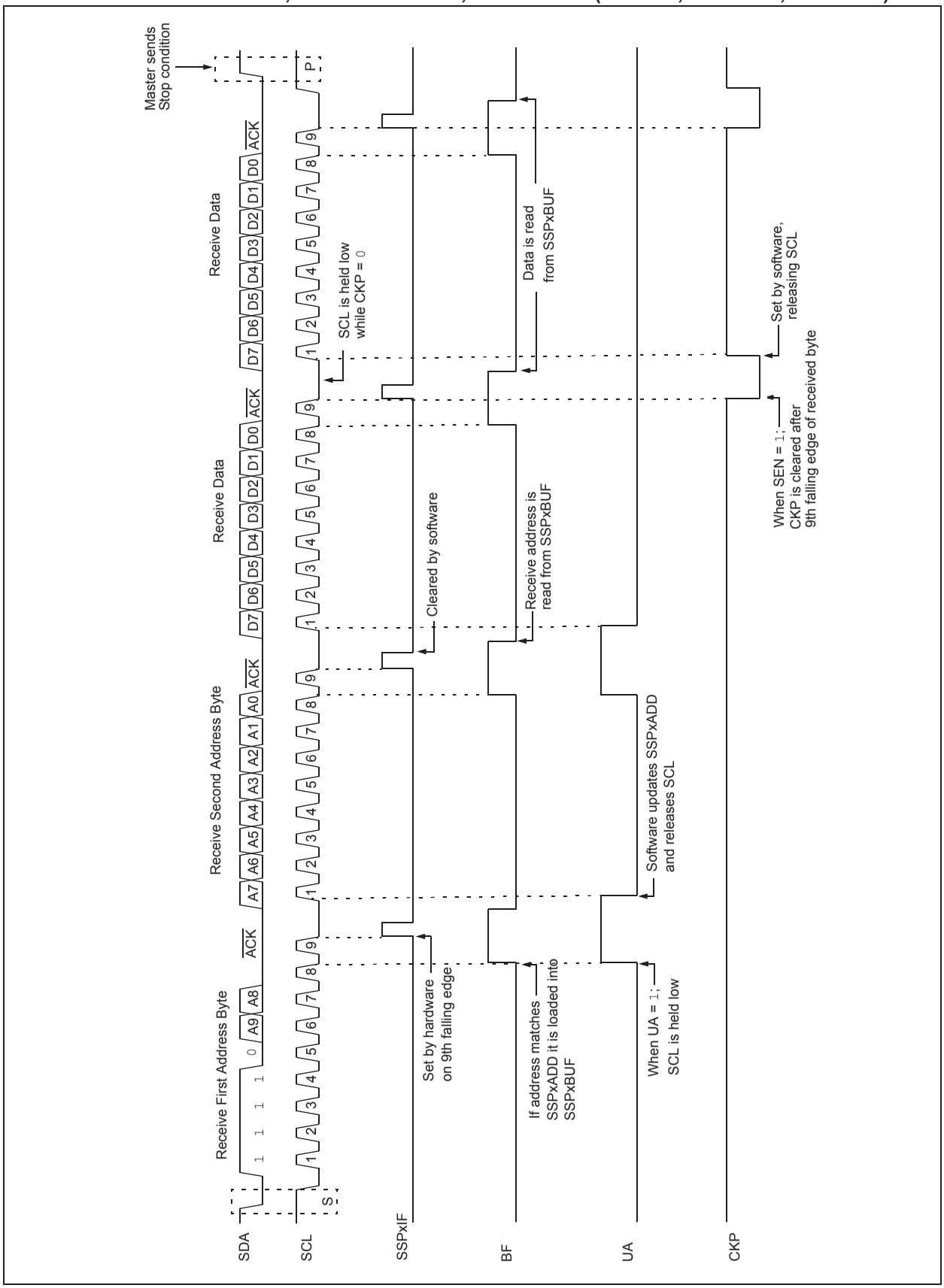


FIGURE 32-20: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)



32.6.13.2 Bus Collision During a Repeated Start Condition

During a Repeated Start condition, a bus collision occurs if:

a) A low level is sampled on SDA when SCL goes from low level to high level (Case 1).

b) SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1' (Case 2).

When the user releases SDA and the pin is allowed to float high, the BRG is loaded with SSPxADD and counts down to zero. The SCL pin is then deasserted and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 32-36). If SDA is sampled high, the BRG is reloaded and begins counting. If SDA goes from high-to-low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high-to-low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated Start condition, see Figure 32-37.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated Start condition is complete.

FIGURE 32-36: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

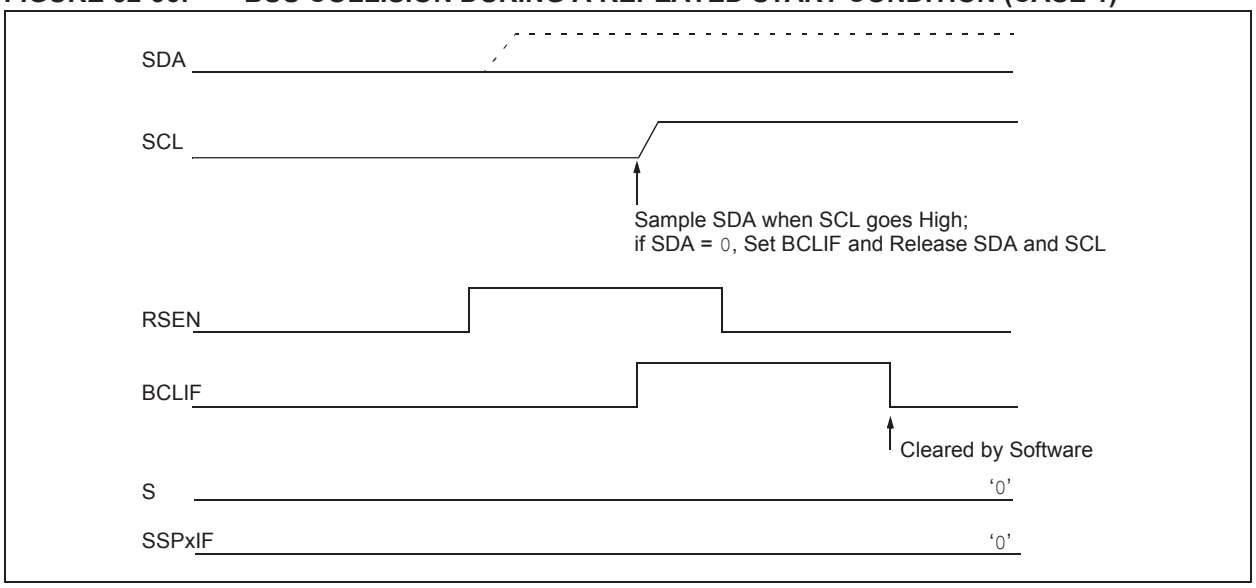
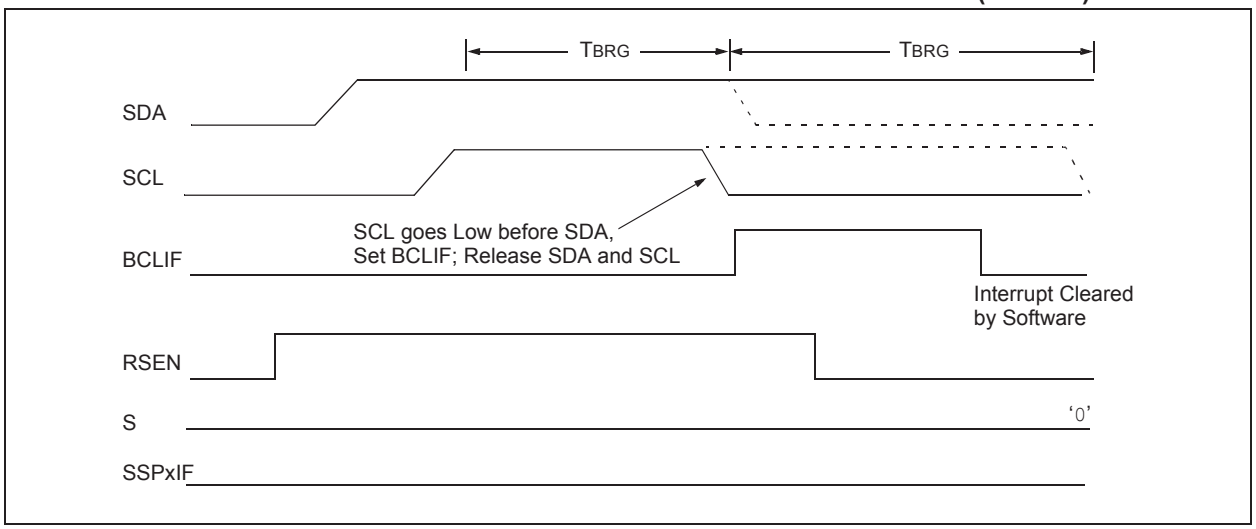


FIGURE 32-37: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



MOVIW **Move INDFn to W**

Syntax: [*label*] MOVIW ++FSRn
[*label*] MOVIW --FSRn
[*label*] MOVIW FSRn++
[*label*] MOVIW FSRn--
[*label*] MOVIW k[FSRn]

Operands: n ∈ [0,1]
mm ∈ [00,01, 10, 11]
-32 ≤ k ≤ 31

Operation: INDFn → W
Effective address is determined by
- FSRn + 1 (preincrement)
- FSRn – 1 (predecrement)
- FSRn + k (relative offset)

After the Move, the FSRn value will be either:
- FSRn + 1 (all increments)
- FSRn – 1 (all decrements)
- Unchanged

Status Affected: Z

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers (INDFn). Before/after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h-FFFFh. Incrementing/decrementing it beyond these bounds will cause it to wrap around.

MOVLB **Move literal to BSR**

Syntax: [*label*] MOVLB k

Operands: 0 ≤ k ≤ 31

Operation: k → BSR

Status Affected: None

Description: The 5-bit literal ‘k’ is loaded into the Bank Select Register (BSR).

MOVLP **Move literal to PCLATH**

Syntax: [*label*] MOVLP k

Operands: 0 ≤ k ≤ 127

Operation: k → PCLATH

Status Affected: None

Description: The 7-bit literal ‘k’ is loaded into the PCLATH register.

MOVLW **Move literal to W**

Syntax: [*label*] MOVLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W)

Status Affected: None

Description: The 8-bit literal ‘k’ is loaded into W register. The “don’t cares” will assemble as ‘0’s.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: 0 ≤ f ≤ 127

Operation: (W) → (f)

Status Affected: None

Description: Move data from W register to register ‘f’.

Words: 1

Cycles: 1

Example:
```
MOVWF   OPTION_REG
```
Before Instruction
OPTION_REG = 0xFF
W = 0x4F
After Instruction
OPTION_REG = 0x4F
W = 0x4F

36.0 ELECTRICAL SPECIFICATIONS

36.1 Absolute Maximum Ratings(†)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on pins with respect to V_{SS}
- on V_{DD} pin
  - PIC16F1764/5/8/9 ..... -0.3V to +6.5V
  - PIC16LF1764/5/8/9 ..... -0.3V to +4.0V
- on $\overline{MCLR}$ pin ..... -0.3V to +9.0V
- on all other pins ..... -0.3V to (V_{DD} + 0.3V)

Maximum current
- on V_{SS} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 250 mA
  - +85°C ≤ T_A ≤ +125°C ..... 85 mA
- on V_{DD} pin(1)
  - -40°C ≤ T_A ≤ +85°C ..... 250 mA
  - +85°C ≤ T_A ≤ +125°C ..... 85 mA
- Sunk by any standard I/O pin ..... 50 mA
- Sourced by any standard I/O pin ..... 50 mA
- Sunk by any high-current I/O pin ..... 100 mA
- Sourced by any high-current I/O pin ..... 100 mA
- Sourced by any op amp output pin ..... 100 mA

Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) ..... ±20 mA
Total power dissipation(2) ..... 800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 36-6: Thermal Characteristics to calculate device specifications.

2: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

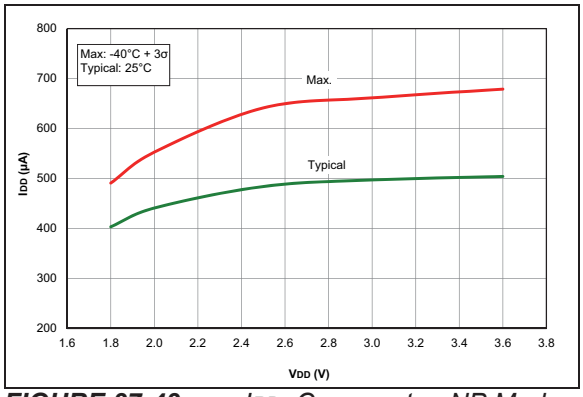


FIGURE 37-43: *IPD, Comparator, NP Mode (CxSP = 1), PIC16LF1764/5/8/9 Only.*

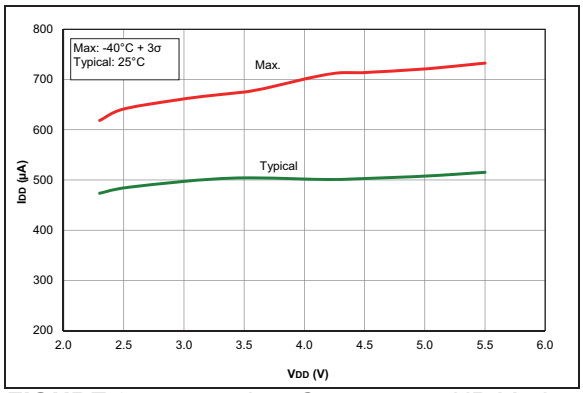


FIGURE 37-44: *IPD, Comparator, NP Mode (CxSP = 1), PIC16F1764/5/8/9 Only.*

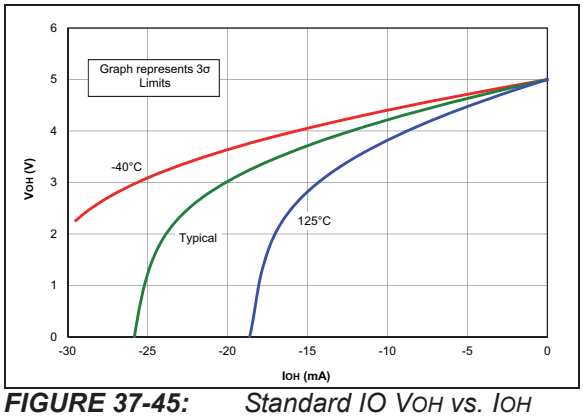


FIGURE 37-45: *Standard IO VOH vs. IOH Over Temperature, VDD = 5.0V, PIC16F1764/5/8/9 Only.*

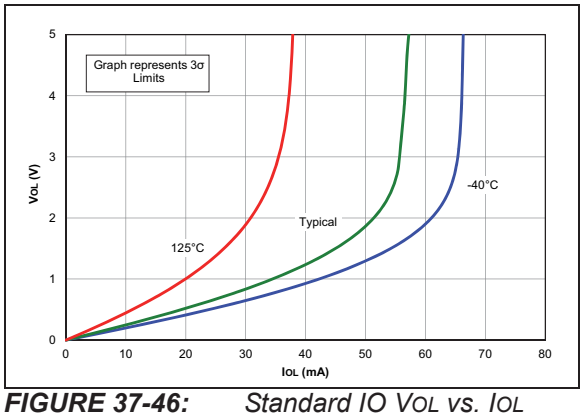


FIGURE 37-46: *Standard IO VOL vs. IOL Over Temperature, VDD = 5.0V, PIC16F1764/5/8/9 Only.*

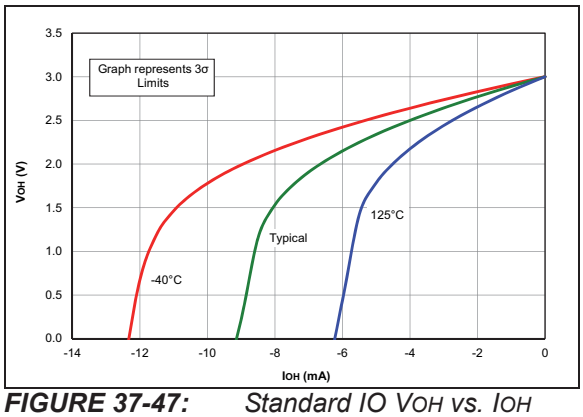


FIGURE 37-47: *Standard IO VOH vs. IOH Over Temperature, VDD = 3.0V.*

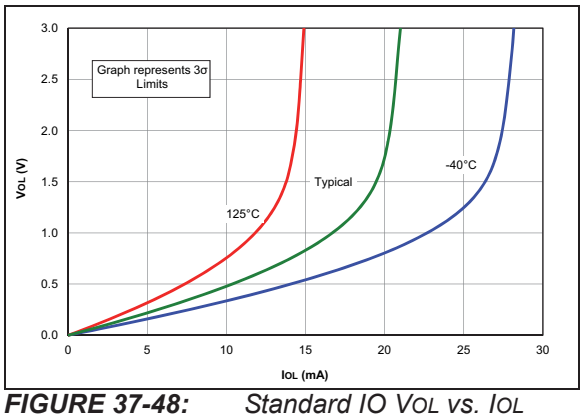


FIGURE 37-48: *Standard IO VOL vs. IOL Over Temperature, VDD = 3.0V.*

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

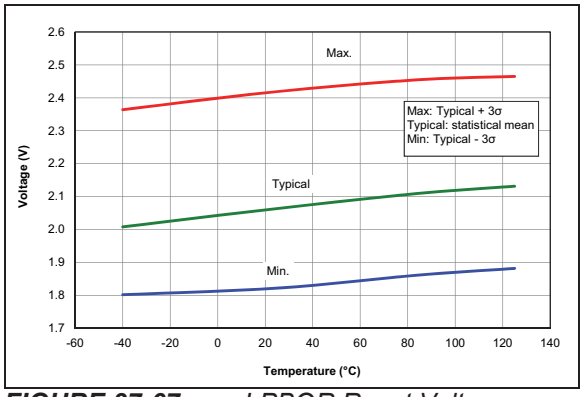


FIGURE 37-67: *LPBOR Reset Voltage.*

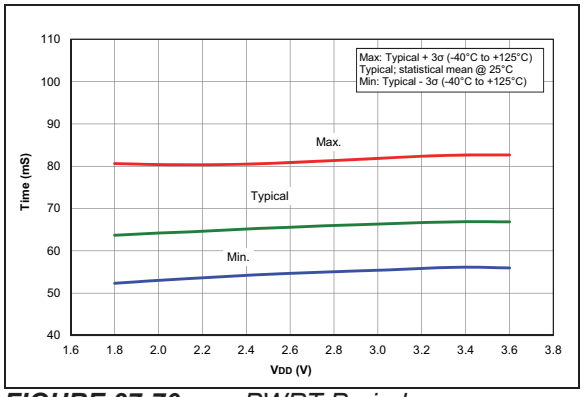


FIGURE 37-70: *PWRT Period, PIC16LF1764/5/8/9 Only.*

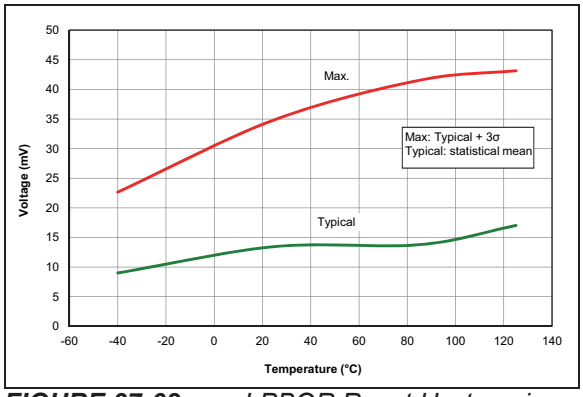


FIGURE 37-68: *LPBOR Reset Hysteresis.*

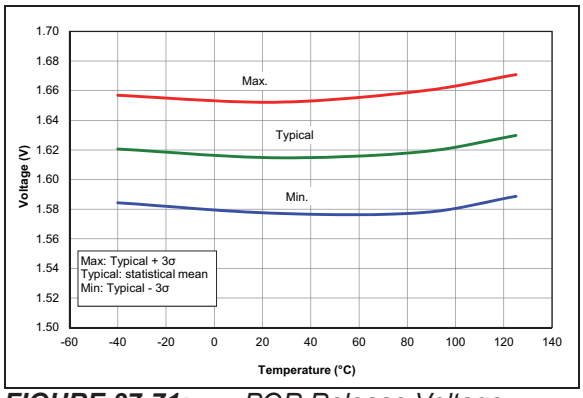


FIGURE 37-71: *POR Release Voltage.*

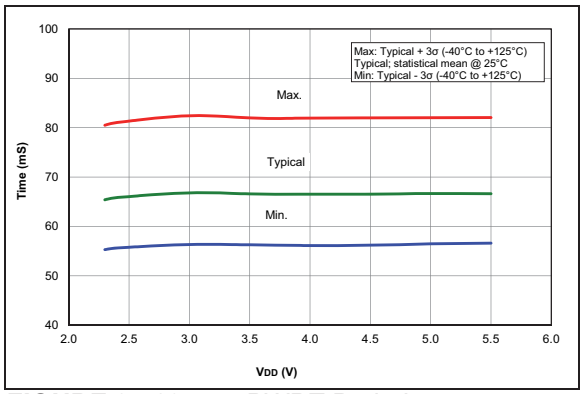


FIGURE 37-69: *PWRT Period, PIC16F1764/5/8/9 Only.*

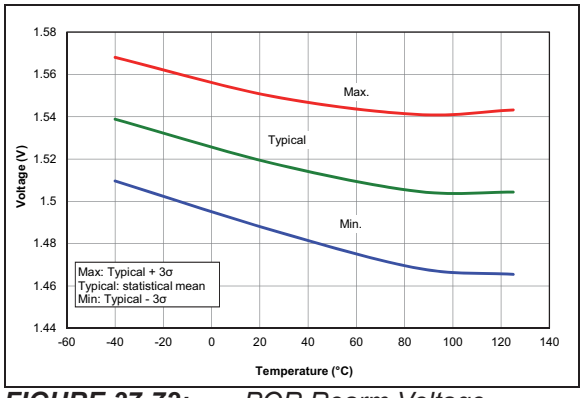
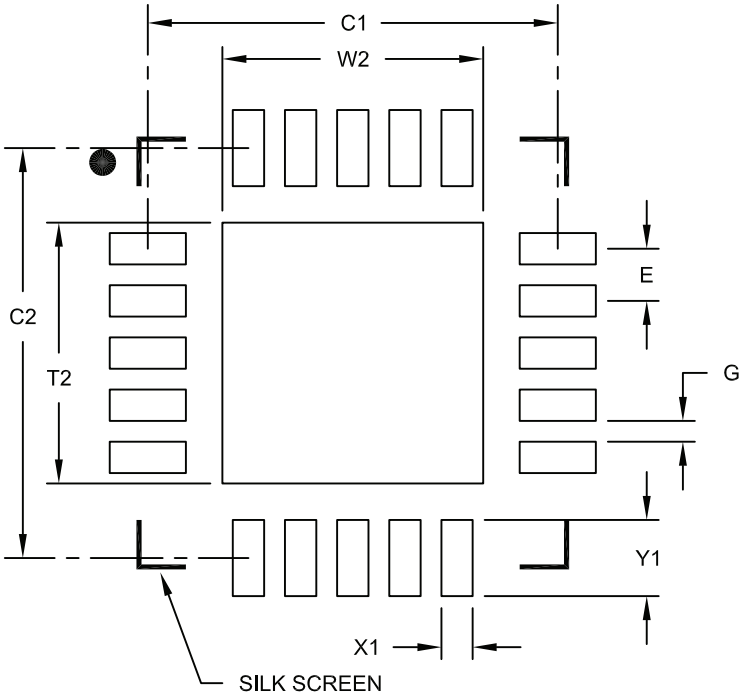


FIGURE 37-72: *POR Rearm Voltage, NP Mode (VREGPM = 0), PIC16F1764/5/8/9 Only.*

20-Lead Plastic Quad Flat, No Lead Package (ML) - 4x4 mm Body [QFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.50
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		3.93	
Contact Pad Spacing	C2		3.93	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.73
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2126A