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Applications of "Embedded - Microcontrollers"

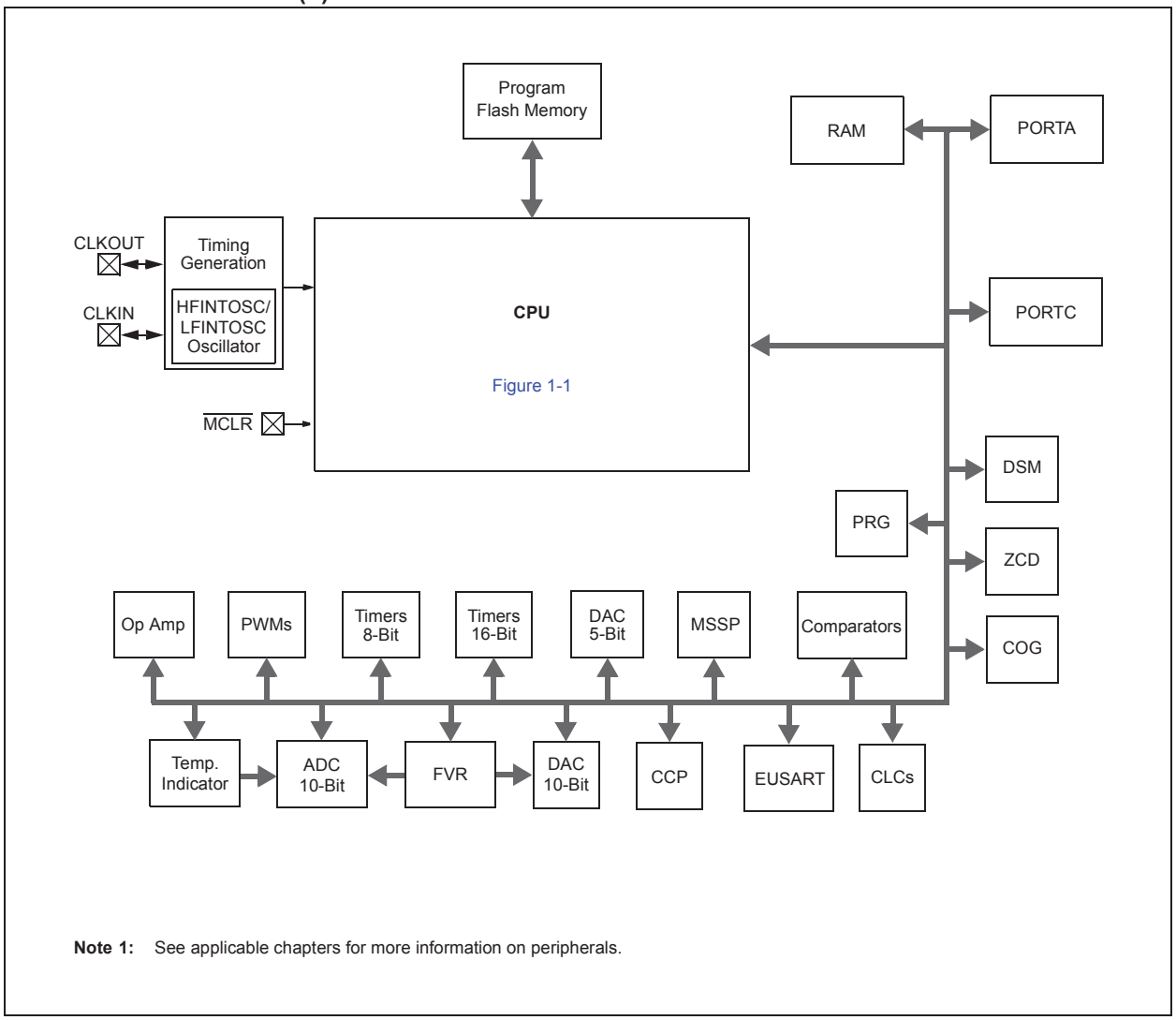
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1768t-i-so

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1768/9) (CONTINUED)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Programmable Ramp Generator	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RC3	7	4	AN7	—	—	OPA2OUT OPA1IN1- OPA1IN1+	C1IN3- C2IN3- C3IN3- C4IN3-	—	PRG2IN0 PRG1IN1	T5G(1)	—	CCP2(1)	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RC4	6	3	—	—	—	—	—	—	PRG1R(1) PRG2R(1)	T3G(1)	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	Y	—
RC5	5	2	—	—	—	—	—	—	PRG1F(1) PRG2F(1)	T3CKI(1)	—	CCP1(1)	—	—	—	—	—	IOC	Y	Y	—
RC6	8	5	AN8	—	—	OPA2IN0-	—	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	IOC	Y	—	—
RC7	9	6	AN9	—	—	OPA2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
OUT(2)	—	—	—	—	—	—	C1OUT	—	—	—	PWM3	CCP1	COG1A	CLC1OUT	MD1OUT	DT(3)	SDO	—	—	—	—
	—	—	—	—	—	—	C2OUT	—	—	—	PWM4	CCP2	COG1B	CLC2OUT	MD2OUT	TX	SDA(3)	—	—	—	—
	—	—	—	—	—	—	C3OUT	—	—	—	PWM5	—	COG1C	CLC3OUT	—	CK	SCK	—	—	—	—
	—	—	—	—	—	—	C4OUT	—	—	—	PWM6	—	COG1D	—	—	—	SCL(3)	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2A	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2B	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2C	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2D	—	—	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection register. See Table 12-1.
2: All pin outputs default to PORT latch data. Any input capable pin can be selected as a digital peripheral output with the PPS Output Selection registers. See Table 12-2.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: Input only.

FIGURE 1-1: PIC16(L)F1764/5 BLOCK DIAGRAM



Note 1: See applicable chapters for more information on peripherals.

TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 31											
F8Ch to FE3h	—	Unimplemented								—	—
FE4h	STATUS_SHAD	—	—	—	—	—	Z	DC	C	---- -xxx	---- -uuu
FE5h	WREG_SHAD	Working Register Shadow								xxxx xxxx	uuuu uuuu
FE6h	BSR_SHAD	—	—	—	Bank Select Register Shadow					---x xxxx	---u uuuu
FE7h	PCLATH_SHAD	—	Program Counter Latch High Register Shadow							-xxx xxxx	-uuu uuuu
FE8h	FSR0L_SHAD	Indirect Data Memory Address 0 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FE9h	FSR0H_SHAD	Indirect Data Memory Address 0 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FEAh	FSR1L_SHAD	Indirect Data Memory Address 1 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FEBh	FSR1H_SHAD	Indirect Data Memory Address 1 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FECh	—	Unimplemented								—	—
FEDh	STKPTR	—	—	—	Current Stack Pointer					---1 1111	---1 1111
FEEh	TOSL	Top of Stack Low byte								xxxx xxxx	uuuu uuuu
FEFh	TOSH	—	Top of Stack High Byte							-xxx xxxx	-uuu uuuu

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1768/9 only.

3: PIC16(L)F1764/5 only.

4: Unimplemented on PIC16LF1764/5/8/9.

REGISTER 7-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **TMR1GIF:** Timer1 Gate Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 6 **ADIF:** Analog-to-Digital Converter (ADC) Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **RCIF:** EUSART Receive Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **TXIF:** EUSART Transmit Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **SSP1IF: Master** Synchronous Serial Port (MSSP) Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **TMR2IF:** Timer2 to T2PR Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 10-6: PMCON2: PROGRAM MEMORY CONTROL 2 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
Program Memory Control Register 2							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
S = Bit can only be set	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **Program Memory Control 2:** Flash Memory Unlock Pattern bits

To unlock writes, 55h must be written first, followed by AAh, before setting the WR bit of the PMCON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes.

TABLE 10-3: SUMMARY OF REGISTERS ASSOCIATED WITH FLASH PROGRAM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
PMCON1	—(1)	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	132
PMCON2	Program Memory Control Register 2								133
PMADRL	PMADRL<7:0>								131
PMADRH	—(1)	PMADRH<6:0>							131
PMDATL	PMDATL<7:0>								130
PMDATH	—	—	PMDATH<5:0>						130

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory.

Note 1: Unimplemented, read as '1'.

TABLE 10-4: SUMMARY OF CONFIGURATION WORD WITH FLASH PROGRAM MEMORY

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	63
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>			
CONFIG2	13:8	—	—	LVP	$\overline{\text{DEBUG}}$	$\overline{\text{LPBOR}}$	BORV	STVREN	PLLEN	65
	7:0	$\overline{\text{ZCD}}$	—	—	—	—	PPS1WAY	WRT<1:0>		

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Flash program memory.

11.1.3 OPEN-DRAIN CONTROL

The ODCONA register (Register 11-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONA bit is set, the corresponding port output becomes an open-drain driver, capable of sinking current only. When an ODCONA bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

11.1.4 SLEW RATE CONTROL

The SLRCONA register (Register 11-7) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONA bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONA bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

11.1.5 INPUT THRESHOLD CONTROL

The INLVLA register (Register 11-8) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an Interrupt-On-Change occurs, if that feature is enabled. See Table 36-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

11.1.6 ANALOG CONTROL

The ANSELA register (Register 11-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRISx clear and ANSELx set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing Read-Modify-Write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSELA bits must be initialized to '0' by user software.

EXAMPLE 11-1: INITIALIZING PORTA

```
; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL  PORTA        ;
CLRF     PORTA        ;Init PORTA
BANKSEL  LATA         ;Data Latch
CLRF     LATA         ;
BANKSEL  ANSELA       ;
CLRF     ANSELA       ;digital I/O
BANKSEL  TRISA        ;
MOVLW    B'00111000'  ;Set RA<5:3> as inputs
MOVWF    TRISA        ;and set RA<2:0> as
                      ;outputs
```

11.1.7 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the Peripheral Pin Select (PPS) logic. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as the ADC and comparator inputs, are not shown in the Peripheral Pin Select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELA register. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 11-5: WPUA: WEAK PULL-UP PORTA REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	WPUA<5:0>(1,2)					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **WPUA<5:0>**: Weak Pull-up PORTA Register bits(1,2)
1 = Pull-up is enabled
0 = Pull-up is disabled

Note 1: The global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 11-6: ODCONA: PORTA OPEN-DRAIN CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	ODA<5:4>		—	ODA<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **ODA<5:4>:** PORTA Open-Drain Enable bits
For RA<5:4> Pins:
1 = Port pins operate as open-drain drive (sink current only)
0 = Port pins operate as standard push-pull drive (source and sink current)

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **ODA<2:0>:** PORTA Open-Drain Enable bits
For RA<2:0> Pins:
1 = Port pins operate as open-drain drive (sink current only)
0 = Port pins operate as standard push-pull drive (source and sink current)

TABLE 12-1: PPS INPUT REGISTER RESET VALUES

Peripheral	xxxPPS Register (Register 12-1)	Default Pin Selection		Reset Value (xxxPPS<4:0>)	
		PIC16(L)F1768/9	PIC16(L)F1764/5	PIC16(L)F1768/9	PIC16(L)F1764/5
Interrupt-On-Change	INTPPS	RA2	RA2	00010	00010
Timer0 Clock	T0CKIPPS	RA2	RA2	00010	00010
Timer1 Clock	T1CKIPPS	RA5	RA5	00101	00101
Timer1 Gate	T1GPPS	RA4	RA4	00100	00100
Timer2 Clock	T2INPPS	RA5	RA5	0101	0101
Timer3 Clock	T3CKIPPS	RC5	RC5	10101	10101
Timer3 Gate	T3GPPS	RC4	RC4	10100	10100
Timer4 Clock	T4INPPS	RC1	RC1	10001	10001
Timer5 Clock	T5CKIPPS	RC0	RC0	10000	10000
Timer5 Gate	T5GPPS	RC3	RC3	10011	10011
Timer6 Clock	T6INPPS	RA3	RA3	00011	00011
CCP1	CCP1PPS	RC5	RC5	10101	10101
CCP2	CCP2PPS(1)	RC3	—	10011	—
COG1	COG1INPPS	RA2	RA2	00010	00010
COG2	COG2INPPS(1)	RA2	—	00010	—
SPI and I^2C Clock	SSPCLKPPS	RB6	RC0	01110	10000
SPI and I^2C Data	SSPDATPPS	RB4	RC1	01100	10001
SPI Slave Select	SSPSSPPS	RC6	RC3	10110	10011
EUSART RX	RXPPS	RB5	RC5	01101	10101
EUSART CK	CKPPS	RB7	RC4	01111	10100
All CLCs	CLCIN0PPS	RC3	RC3	10011	10011
All CLCs	CLCIN1PPS	RC4	RC4	10100	10100
All CLCs	CLCIN2PPS	RC1	RC1	10001	10001
All CLCs	CLCIN3PPS	RA5	RA5	00101	00101
PRG1 Set Rising	PRG1RPPS	RC4	RC4	10100	10100
PRG1 Set Falling	PRG1FPPS	RC5	RC5	10101	10101
PRG2 Set Rising	PRG2RPPS(1)	RC4	—	10100	—
PRG2 Set Falling	PRG2FPPS(1)	RC5	—	10101	—
DSM1 High Carrier	MD1CHPPS	RA3	RA3	00011	00011
DSM1 Low Carrier	MD1CLPPS	RA4	RA4	00100	00100
DSM1 Modulation	MD1MODPPS	RA5	RA5	00101	00101
DSM2 High Carrier	MD2CHPPS(1)	RA3	—	00011	—
DSM2 Low Carrier	MD2CLPPS(1)	RA4	—	00100	—
DSM2 Modulation	MD2MODPPS(1)	RA5	—	00101	—

Example: CCP1PPS = 0x13 selects RC3 as the CCP1 input.

Note 1: PIC16(L)F1768/9 only.

18.7 Register Definitions: DAC Control

Long bit name prefixes for the 10-bit DAC peripherals are shown in Table 18-2. Refer to **Section 1.1 "Register and Bit Naming Conventions"** for more information.

TABLE 18-2: BIT NAME PREFIXES

Peripheral	Bit Name Prefix
DAC1	DAC1
DAC2(1)	DAC2

Note 1: PIC16(L)F1768/9 devices only.

REGISTER 18-1: DACxCON0: DACx CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0
EN	FM	OE1	—	PSS<1:0>		—	NSS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **EN:** DACx Enable bit
- 1 = DACx is enabled
- 0 = DACx is disabled

bit 6 **FM:** DACx Reference Format bit
- 1 = DACx reference selection is left justified
- 0 = DACx reference selection is right justified

bit 5 **OE1:** DACx Voltage Output Enable bit
- 1 = DACx voltage level is also an output on the DACxOUT1 pin
- 0 = DACx voltage level is disconnected from the DACxOUT1 pin

bit 4 **Unimplemented:** Read as '0'

bit 3-2 **PSS<1:0>:** DACx Positive Source Select bits
- 11 = Reserved; do not use.
- 10 = FVR_buffer2
- 01 = V_{REF+} pin
- 00 = V_{DD}

bit 1 **Unimplemented:** Read as '0'

bit 0 **NSS:** DACx Negative Source Select bit
- 1 = V_{REF-} pin
- 0 = V_{SS}

24.4 CCP/PWM Clock Selection

The PIC16(L)F1764/5/8/9 allows each individual CCP and PWM module to select the timer source that controls the module. Each module has an independent selection.

As there are up to three 8-bit timers with auto-reload (Timer2/4/6), the PWM mode on the CCP and PWM modules can use any of these timers.

The CCPTMRS register is used to select which timer is used.

24.4.1 USING THE TMR2/4/6 WITH THE CCP MODULE

This device has a new version of the TMR2 module that has many new modes, which allow for greater customization and control of the PWM signals than older parts. Refer to **Section 23.6 "Operation Examples"** for examples of PWM signal generation using the different modes of Timer2. The CCP operation requires that the timer used as the PWM time base has the FOSC/4 clock source selected.

24.4.2 PWM PERIOD

The PWM period is specified by the T2PR/T4PR/T6PR register of Timer2/4/6. The PWM period can be calculated using the formula of Equation 24-1.

EQUATION 24-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

Note 1: TOSC = 1/FOSC.

When TMR2/4/6 is equal to its respective T2PR/T4PR/T6PR register, the following three events occur on the next increment cycle:

- TMR2/4/6 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from the CCPRxH:CCPRxL pair into the internal 10-bit latch.

Note: The Timer postscaler (see Figure 24-1) is not used in the determination of the PWM frequency.

24.4.3 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to two registers: the CCPRxH:CCPRxL register pair. Where the particular bits go is determined by the FMT bit of the CCPxCON register. If FMT = 0, the two Most Significant bits of the duty cycle value should be written to bits<1:0> of the CCPRxH register and the remaining eight bits to the CCPRxL register. If FMT = 1, the Least Significant two bits of the duty cycle should be written to bits<7:6> of the CCPRxL register and the Most Significant eight bits to the CCPRxH register. This is illustrated in Figure 24-4. These bits can be written at any time. The duty cycle value is not latched into the internal latch until after the period completes (i.e., a match between T2PR/T4PR/T6PR and TMR2/4/6 registers occurs).

Equation 24-2 is used to calculate the PWM pulse width. Equation 24-3 is used to calculate the PWM duty cycle ratio.

EQUATION 24-2: PULSE WIDTH

$$Pulse\ Width = CCPRxH:CCPRxL \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

EQUATION 24-3: DUTY CYCLE RATIO

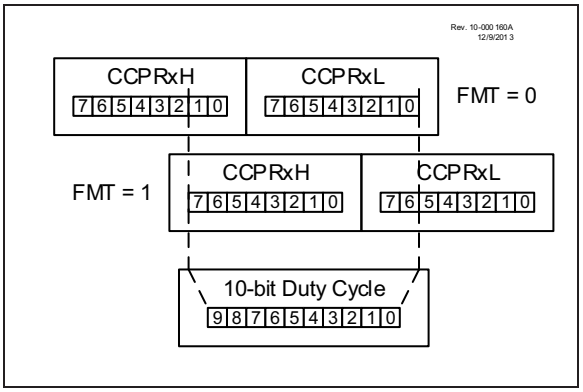
$$Duty\ Cycle\ Ratio = \frac{(CCPRxH:CCPRxL)}{4(PRx + 1)}$$

The PWM Duty Cycle registers are double-buffered for glitchless PWM operation.

The 8-bit timer TMR2/4/6 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2/4/6 prescaler is set to 1:1.

When the 10-bit time base matches the internal buffer register, then the CCPx pin is cleared (see Figure 24-3).

FIGURE 24-4: CCPx DUTY CYCLE ALIGNMENT



REGISTER 24-2: CCPTMRS: PWM TIMER SELECTION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
P4TSEL<1:0>(1)		P3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

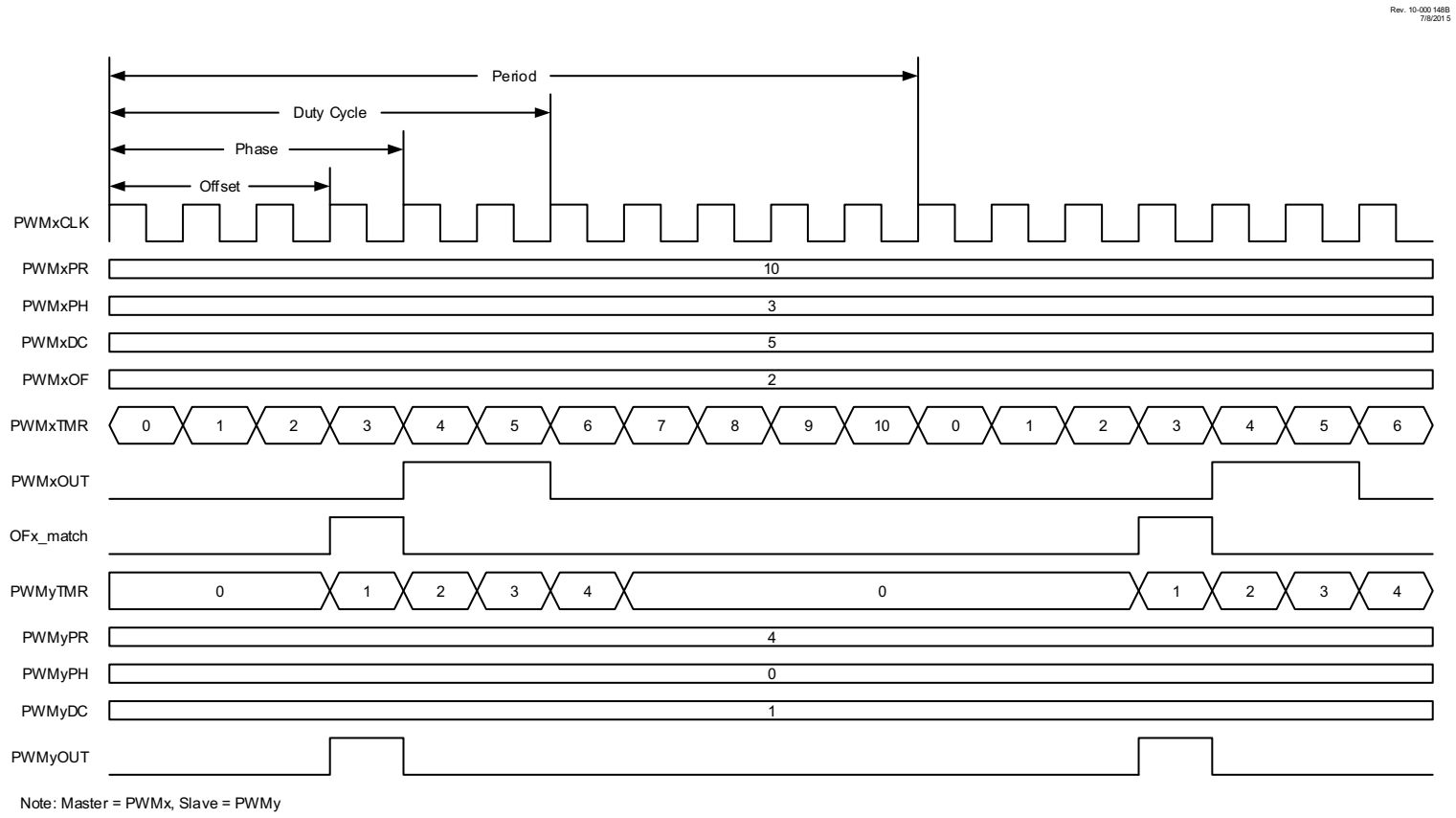
bit 7-6 **P4TSEL<1:0>:** PWM4 Timer Selection bits(1)
- 11 = Reserved
- 10 = PWM4 is based off Timer6 in PWM mode
- 01 = PWM4 is based off Timer4 in PWM mode
- 00 = PWM4 is based off Timer2 in PWM mode

bit 5-4 **P3TSEL<1:0>:** PWM3 Timer Selection bits
- 11 = Reserved
- 10 = PWM3 is based off Timer6 in PWM mode
- 01 = PWM3 is based off Timer4 in PWM mode
- 00 = PWM3 is based off Timer2 in PWM mode

bit 3-2 **C2TSEL<1:0>:** CCP2 (PWM2) Timer Selection bits
- 11 = Reserved
- 10 = CCP2 is based off Timer6 in PWM mode
- 01 = CCP2 is based off Timer4 in PWM mode
- 00 = CCP2 is based off Timer2 in PWM mode

bit 1-0 **C1TSEL<1:0>:** CCP1 (PWM1) Timer Selection bits
- 11 = Reserved
- 10 = CCP1 is based off Timer6 in PWM mode
- 01 = CCP1 is based off Timer4 in PWM mode
- 00 = CCP1 is based off Timer2 in PWM mode

FIGURE 26-10: ONE-SHOT SLAVE RUN MODE WITH SYNC START TIMING DIAGRAM



REGISTER 26-3: PWMxINTF: PWMx INTERRUPT REQUEST REGISTER

U-0	U-0	U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	—	—	OFIF(1)	PHIF(1)	DCIF(1)	PRIF(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	HS = Hardware Settable bit
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OFIF**: Offset Interrupt Flag bit(1)
- 1 = Offset match event occurred
- 0 = Offset match event did not occur

bit 2 **PHIF:** Phase Interrupt Flag bit(1)
- 1 = Phase match event occurred
- 0 = Phase match event did not occur

bit 1 **DCIF:** Duty Cycle Interrupt Flag bit(1)
- 1 = Duty cycle match event occurred
- 0 = Duty cycle match event did not occur

bit 0 **PRIF:** Period Interrupt Flag bit(1)
- 1 = Period match event occurred
- 0 = Period match event did not occur

Note 1: Bit is forced clear by hardware while module is disabled (EN = 0).

FIGURE 27-12: FULL-BRIDGE FORWARD MODE COG OPERATION WITH CCP1

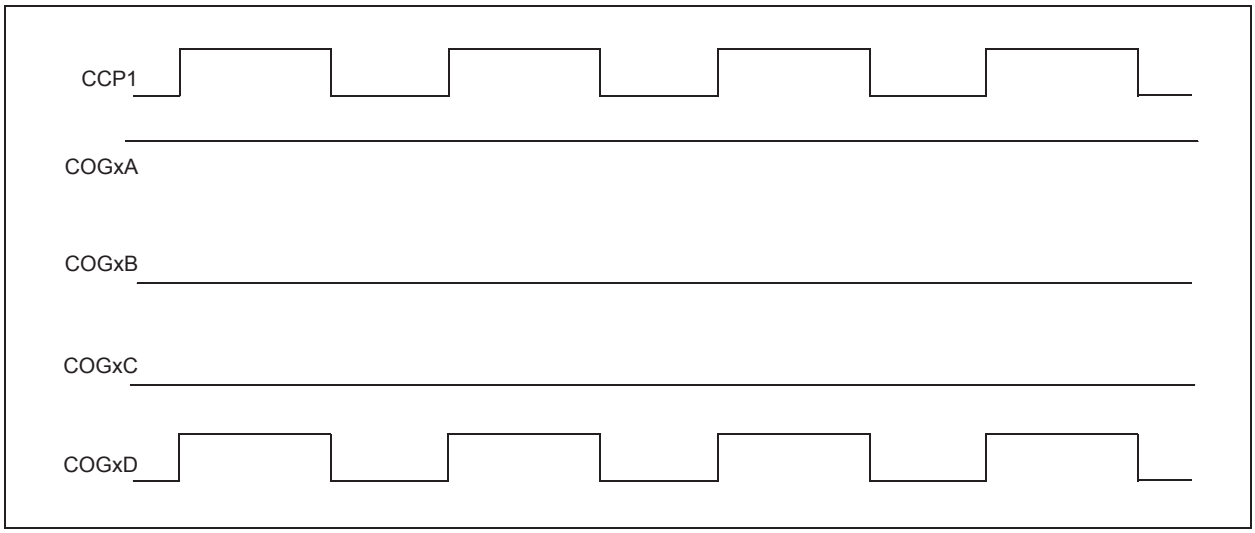
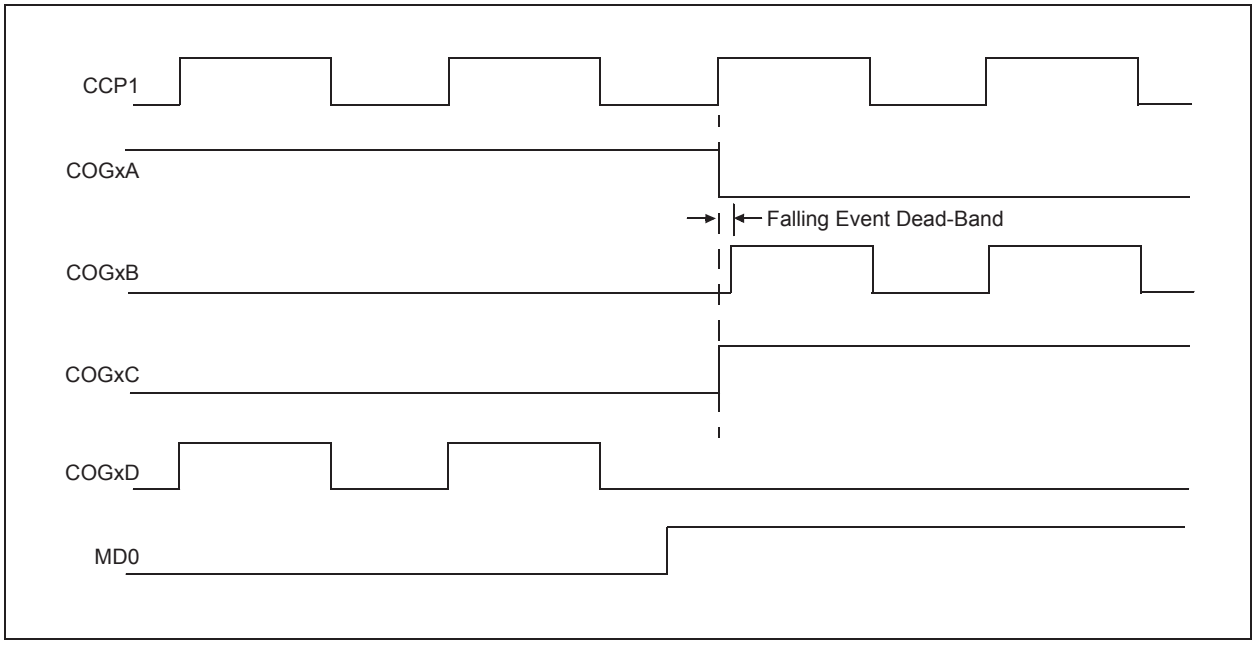


FIGURE 27-13: FULL-BRIDGE MODE COG OPERATION WITH CCP1 AND DIRECTION CHANGE



27.5.2 RISING EVENT

The rising event starts the PWM output active duty cycle period. The rising event is the low-to-high transition of the rising_event output. When the rising event phase delay and dead-band time values are zero, the primary output starts immediately. Otherwise, the primary output is delayed. The rising event source causes all the following actions:

- Start rising event phase delay counter (if enabled)
- Clear complementary output after phase delay
- Start falling event input blanking (if enabled)
- Start dead-band delay (if enabled)
- Set primary output after dead-band delay expires

27.5.3 FALLING EVENT

The falling event terminates the PWM output active duty cycle period. The falling event is the high-to-low transition of the falling_event output. When the falling event phase delay and dead-band time values are zero, the complementary output starts immediately. Otherwise, the complementary output is delayed. The falling event source causes all the following actions:

- Start falling event phase delay counter (if enabled)
- Clear primary output
- Start rising event input blanking (if enabled)
- Start falling event dead-band delay (if enabled)
- Set complementary output after dead-band delay expires

27.6 Output Control

Upon disabling, or immediately after enabling the COG module, the primary COG outputs are inactive and complementary COG outputs are active.

27.6.1 OUTPUT ENABLES

There are no output enable controls in the COG module. Instead, each device pin has an individual output selection control called the PPS register. All four COG outputs are available for selection in the PPS register of every pin.

When a COG output is enabled by PPS selection, the output on the pin has several possibilities which depend on the mode, steering control, EN bit and shutdown state, as shown in Table 27-1 and Table 27-2.

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TABLE 27-1: PIN OUTPUT STATES MD<2:0> = 00x

EN Bit	STR Bit	Shutdown	Output
x	0	Inactive	Static Steering Data
x	1	Active	Shutdown Override
0	1	Inactive	Inactive State
1	1	Inactive	Active PWM Signal

TABLE 27-2: PIN OUTPUT STATES MD<2:0> > 001

EN Bit	STR Bit	Shutdown	Output
x	x	Inactive	Inactive State
x	x	Active	Shutdown Override
1	x	Inactive	Active PWM Signal

27.6.2 POLARITY CONTROL

The polarity of each COG output can be selected independently. When the output polarity bit is set, the corresponding output is active-low. Clearing the output polarity bit configures the corresponding output as active-high. However, polarity affects the outputs in only one of the four Shutdown Override modes. See **Section 27.10 "Auto-Shutdown Control"** for more details.

Output polarity is selected with the POLA through POLD bits of the COGxCON1 register (Register 27-2).

27.7 Dead-Band Control

The dead-band control provides for non-overlapping PWM output signals to prevent shoot-through current in the external power switches. Dead-band time affects the output only in the Half-Bridge mode and when changing direction in the Full-Bridge mode.

The COG contains two dead-band timers. One dead-band timer is used for rising event dead-band control. The other is used for falling event dead-band control. Timer modes are selectable as either:

- Asynchronous delay chain
- Synchronous counter

The Dead-Band Timer mode is selected for the rising event and falling event dead-band times, with the respective RDBS and FDBS bits of the COGxCON1 register (Register 27-2).

In Half-Bridge mode, the rising event dead-band time delays all selected primary outputs from going active for the selected dead-band time after the rising event. COGxA and COGxC are the primary outputs in Half-Bridge mode.

In Half-Bridge mode, the falling event dead-band time delays all selected complementary outputs from going active for the selected dead-band time after the falling event. COGxB and COGxD are the complementary outputs in Half-Bridge mode.

In Full-Bridge mode, the dead-band delay occurs only during direction changes. The modulated output is delayed for the falling event dead-band time after a direction change from forward to reverse. The modulated output is delayed for the rising event dead-band time after a direction change from reverse to forward.

TABLE 30-5: SUMMARY OF REGISTERS ASSOCIATED WITH THE PRG MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
PRG1CON0	EN	—	FEDG	REDG	MODE<1:0>		OS	GO	360
PRG1CON1	—	—	—	—	—	RDY	FPOL	RPOL	361
PRG1CON2	—	—	—	ISET<4:0>					363
PRG1INS	—	—	—	—	INS<3:0>				361
PRG1RPPS	—	—	—	PRG1RPPS<4:0>					364
PRG1FPPS	—	—	—	PRG1FPPS<4:0>					364
PRG1RTSS	—	—	—	—	RTSS<3:0>				154, 156
PRG1FTSS	—	—	—	—	FTSS<3:0>				154, 156
PRG2CON0(1)	EN	—	FEDG	REDG	MODE<1:0>		OS	GO	360
PRG2CON1(1)	—	—	—	—	—	RDY	FPOL	RPOL	361
PRG2CON2(1)	—	—	—	ISET<4:0>					363
PRG2INS(1)	—	—	—	—	INS<3:0>				361
PRG2RPPS(1)	—	—	—	PRG2RPPS<4:0>					364
PRG2FPPS(1)	—	—	—	PRG2FPPS<4:0>					364
PRG2RTSS(1)	—	—	—	—	RTSS<3:0>				154, 156
PRG2FTSS(1)	—	—	—	—	FTSS<3:0>				154, 156
PORTC	RC<7:6>(1)		RC<5:0>						147
TRISC	TRISC<7:6>(1)		TRISC<5:4>		TRISC<3:2>		TRISC<1:0>		147
ANSELC	ANSC<7:6>(1)		—	—	ANSC<3:2>		ANSC<1:0>		148
WPUC	WPUC<7:6>(1)		WPUC<5:4>		WPUC<3:2>		WPUC<1:0>		149

Legend: — = unimplemented, read as '0'. Shaded cells are unused by the PRG module.

Note 1: PIC16(L)F1768/9 only.

REGISTER 32-3: SSP1CON2: MSSP CONTROL REGISTER 2(1)

R/W-0/0	R-0/0	R/W-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/S/HS-0/0	R/W/HS-0/0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	HS = Hardware Settable bit	S = Settable bit
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'	
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets	

bit 7 **GCEN:** General Call Enable bit (in I^2C Slave mode only)
1 = Enables interrupt when a general call address (0x00 or 00h) is received in the SSPSR
0 = General call address disabled

bit 6 **ACKSTAT:** Acknowledge Status bit (in I^2C mode only)
1 = Acknowledge was not received
0 = Acknowledge was received

bit 5 **ACKDT:** Acknowledge Data bit (in I^2C mode only)
In Receive mode:
Value transmitted when the user initiates an Acknowledge sequence at the end of a receive.
1 = Not Acknowledge
0 = Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit (in I^2C Master mode only)
In Master Receive mode:
1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit; automatically cleared by hardware
0 = Acknowledge sequence is Idle

bit 3 **RCEN:** Receive Enable bit (in I^2C Master mode only)
1 = Enables Receive mode for I^2C
0 = Receive is Idle

bit 2 **PEN:** Stop Condition Enable bit (in I^2C Master mode only)
SCKMSSP Release Control:
1 = Initiates Stop condition on SDA and SCL pins; automatically cleared by hardware
0 = Stop condition is Idle

bit 1 **RSEN:** Repeated Start Condition Enable bit (in I^2C Master mode only)
1 = Initiates Repeated Start condition on SDA and SCL pins; automatically cleared by hardware
0 = Repeated Start condition is Idle

bit 0 **SEN:** Start Condition Enable/Stretch Enable bit
In Master mode:
1 = Initiates Start condition on SDA and SCL pins; automatically cleared by hardware
0 = Start condition is Idle
In Slave mode:
1 = Clock stretching is enabled for both slave transmit and slave receive (stretch enabled)
0 = Clock stretching is disabled

Note 1: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I^2C module is not in Idle mode, this bit may not be set (no spooling) and the SSPxBUF may not be written (or writes to the SSPxBUF are disabled).

36.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} – Operating Supply Voltage(1)

PIC16LF1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +1.8V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +3.6V

PIC16F1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +2.3V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +5.5V

T_A – Operating Ambient Temperature Range

Industrial Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +85°C

Extended Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

TABLE 36-3: POWER-DOWN CURRENTS (I_{PD})(1,2)

PIC16LF1764/5/8/9		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC16F1764/5/8/9		Low-Power Sleep Mode, VREGPM = 1						
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V_{DD}	Note
D023	Base I_{PD}	—	0.05	1.0	8.0	µA	1.8	WDT, BOR, FVR and SOSC disabled, all peripherals inactive
		—	0.08	2.0	9.0	µA	3.0	
D023	Base I_{PD}	—	0.3	3	11	µA	2.3	WDT, BOR, FVR and SOSC disabled, all peripherals inactive, Low-Power Sleep mode
		—	0.4	4	12	µA	3.0	
		—	0.5	6	15	µA	5.0	
D023A	Base I_{PD}	—	9.8	16	18	µA	2.3	WDT, BOR, FVR and SOSC disabled, all peripherals inactive, Normal Power Sleep mode, VREGPM = 0
		—	10.3	18	20	µA	3.0	
		—	11.5	21	26	µA	5.0	
D024		—	0.5	6	14	µA	1.8	WDT current
		—	0.8	7	17	µA	3.0	
D024		—	0.8	6	15	µA	2.3	WDT current
		—	0.9	7	20	µA	3.0	
		—	1.0	8	22	µA	5.0	
D025		—	15	28	30	µA	1.8	FVR current
		—	24	35	38	µA	3.0	
D025		—	18	33	35	µA	2.3	FVR current
		—	24	35	37	µA	3.0	
		—	26	37	39	µA	5.0	
D026		—	7.5	25	28	µA	3.0	BOR current
D026		—	10	25	28	µA	3.0	BOR current
		—	12	28	31	µA	5.0	
D027		—	0.5	4	10	µA	3.0	LPBOR current
D027		—	0.8	6	14	µA	3.0	LPBOR current
		—	1	8	17	µA	5.0	
D028		—	0.5	5	9	µA	1.8	SOSC current
		—	0.8	8.5	12	µA	3.0	
D028		—	1.1	6	10	µA	2.3	SOSC current
		—	1.3	8.5	20	µA	3.0	
		—	1.4	10	25	µA	5.0	
D029		—	0.05	2	9	µA	1.8	ADC current, no conversion in progress **(Note 3)**
		—	0.08	3	10	µA	3.0	
D029		—	0.3	4	12	µA	2.3	ADC current, no conversion in progress **(Note 3)**
		—	0.4	5	13	µA	3.0	
		—	0.5	7	16	µA	5.0	

* These parameters are characterized but not tested.

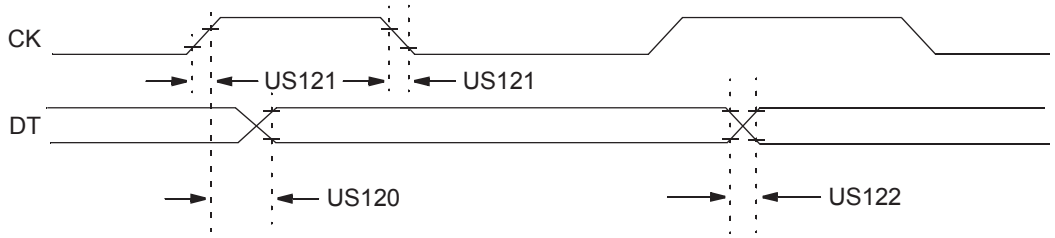
† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: ADC clock source is FRC.

FIGURE 36-15: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

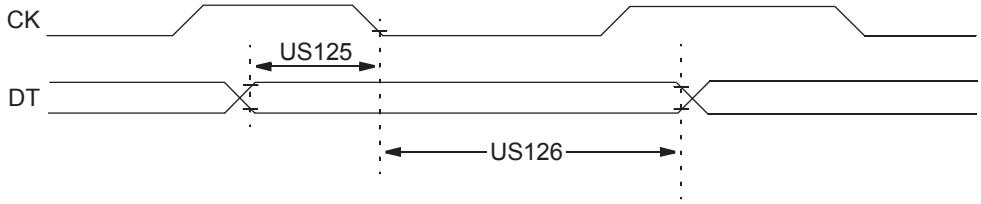


Note: Refer to Figure 36-4 for load conditions.

TABLE 36-23: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US120	TCKH2DTV	SYNC XMIT (Master and Slave) Clock High to Data-out Valid	—	80	ns	3.0V ≤ VDD ≤ 5.5V
			—	100	ns	1.8V ≤ VDD ≤ 5.5V
US121	TCKRF	Clock Out Rise Time and Fall Time (Master mode)	—	45	ns	3.0V ≤ VDD ≤ 5.5V
			—	50	ns	1.8V ≤ VDD ≤ 5.5V
US122	TDTRF	Data-out Rise Time and Fall Time	—	45	ns	3.0V ≤ VDD ≤ 5.5V
			—	50	ns	1.8V ≤ VDD ≤ 5.5V

FIGURE 36-16: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



Note: Refer to Figure 36-4 for load conditions.

TABLE 36-24: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-Setup before CK ↓ (DT hold time)	10	—	ns	
US126	TCKL2DTL	Data-hold after CK ↓ (DT hold time)	15	—	ns	