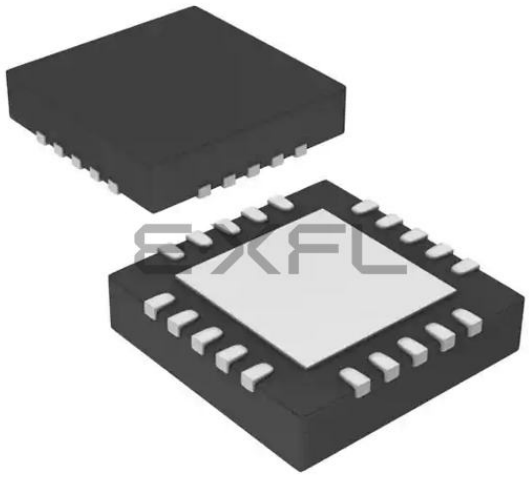

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1769-e-ml

TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 2											
10Ch	LATA	—	—	LATA<5:4>		—	LATA<2:0>			--xx -xxx	--uu -uuu
10Dh	LATB(2)	LATB<7:4>				—	—	—	—	xxxx ----	uuuu ----
10Eh	LATC	LATC<7:6>(2)		LATC<5:0>						xxxx xxxx	uuuu uuuu
10Fh	CMOUT	—	—	—	—	MC4OUT(2)	MC3OUT(2)	MC2OUT	MC1OUT	---- 0000	---- 0000
110h	CM1CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	00-0 0100	00-0 0100
111h	CM1CON1	—	—	—	—	—	—	INTP	INTN	---- --00	---- --00
112h	CM1NSEL	—	—	—	—	—	NCH<2:0>			---- -000	---- -000
113h	CM1PSEL	—	—	—	—	—	PCH<2:0>			---- -000	---- -000
114h	CM2CON0	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	00-0 0100	00-0 0100
115h	CM2CON1	—	—	—	—	—	—	INTP	INTN	---- --00	---- --00
116h	CM2NSEL	—	—	—	—	—	NCH<2:0>			---- -000	---- -000
117h	CM2PSEL	—	—	—	—	—	PCH<2:0>			---- -000	---- -000
118h	CM3CON0(2)	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	00-0 0100	00-0 0100
119h	CM3CON1(2)	—	—	—	—	—	—	INTP	INTN	---- --00	---- --00
11Ah	CM3NSEL(2)	—	—	—	—	—	NCH<2:0>			---- -000	---- -000
11Bh	CM3PSEL(2)	—	—	—	—	—	PCH<2:0>			---- -000	---- -000
11Ch	CM4CON0(2)	ON	OUT	—	POL	ZLF	Reserved	HYS	SYNC	00-0 0100	00-0 0100
11Dh	CM4CON1(2)	—	—	—	—	—	—	INTP	INTN	---- --00	---- --00
11Eh	CM4NSEL(2)	—	—	—	—	—	NCH<2:0>			---- -000	---- -000
11Fh	CM4PSEL(2)	—	—	—	—	—	PCH<2:0>			---- -000	---- -000
Bank 3											
18Ch	ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			---1 -111	---1 -111
18Dh	ANSELB(2)	ANSB<7:4>				—	—	—	—	1111 ----	1111 ----
18Eh	ANSELC	ANSC<7:6>(2)		—	—	ANSC<3:0>				11-- 1111	11-- 1111
18Fh	—	Unimplemented								—	—
190h	—	Unimplemented								—	—
191h	PMADRL	Program Memory Address Register Low Byte								0000 0000	0000 0000
192h	PMADRH	—(1)	Program Memory Address Register High Byte							1000 0000	1000 0000
193h	PMDATL	Program Memory Read Data Register Low Byte								xxxx xxxx	uuuu uuuu
194h	PMDATH	—	—	Program Memory Read Data Register High Byte						--xx xxxx	--uu uuuu
195h	PMCON1	—(1)	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	1000 x000	1000 q000
196h	PMCON2	Program Memory Control Register 2								0000 0000	0000 0000
197h	VREGCON(4)	—	—	—	—	—	—	VREGPM	Reserved	---- --01	---- --01
198h	—	Unimplemented								—	—
199h	RC1REG	EUSART Receive Data Register								0000 0000	0000 0000
19Ah	TX1REG	EUSART Transmit Data Register								0000 0000	0000 0000
19Bh	SP1BRGL	SP1BRG<7:0>								0000 0000	0000 0000
19Ch	SP1BRGH	SP1BRG<15:8>								0000 0000	0000 0000
19Dh	RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 0000	0000 0000
19Eh	TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	0000 0010
19Fh	BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	01-0 0-00

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1768/9 only.

3: PIC16(L)F1764/5 only.

4: Unimplemented on PIC16LF1764/5/8/9.

REGISTER 4-4: REVID: REVISION ID REGISTER

R	R	R	R	R	R
REV<13:8>					
bit 13					bit 8

R	R	R	R	R	R	R	R
REV<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	'1' = Bit is set	'0' = Bit is cleared

bit 13-0 **REV<13:0>**: Revision ID bits

5.4 Two-Speed Clock Start-up Mode

Two-Speed Clock Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the Internal Oscillator Block, INTOSC, as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

Note:	Executing a `SLEEP` instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCSTAT register to remain clear.

5.4.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Words) = `1`; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS<1:0> (of the OSCCON register) = `00`.
- FOSC<2:0> bits in the Configuration Words configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

TABLE 5-1: OSCILLATOR SWITCHING DELAYS

Switch From	Switch To	Frequency	Oscillator Delay
Sleep	LFINTOSC MFINTOSC HFINTOSC(1)	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-up Delay (TWARM)(2)
Sleep	EC, RC(1)	DC- 32 MHz	2 cycles
LFINTOSC	EC, RC(1)	DC-32 MHz	1 Cycle of Each
Sleep	Secondary Oscillator LP, XT, HS(1)	32 kHz-20 MHz	1024 Clock Cycles (OST)
Any Clock Source	MFINTOSC HFINTOSC(1)	31.25 kHz-500 kHz 31.25 kHz-16 MHz	2 μs (approx.)
Any Clock Source	LFINTOSC	31 kHz	1 Cycle of Each
Any Clock Source	Secondary Oscillator	32 kHz	1024 Clock Cycles (OST)
PLL Inactive	PLL Active	16-32 MHz	2 ms (approx.)

Note 1: PLL is inactive.

2: See Table 36-8.

FIGURE 18-1: DAC JUSTIFICATION

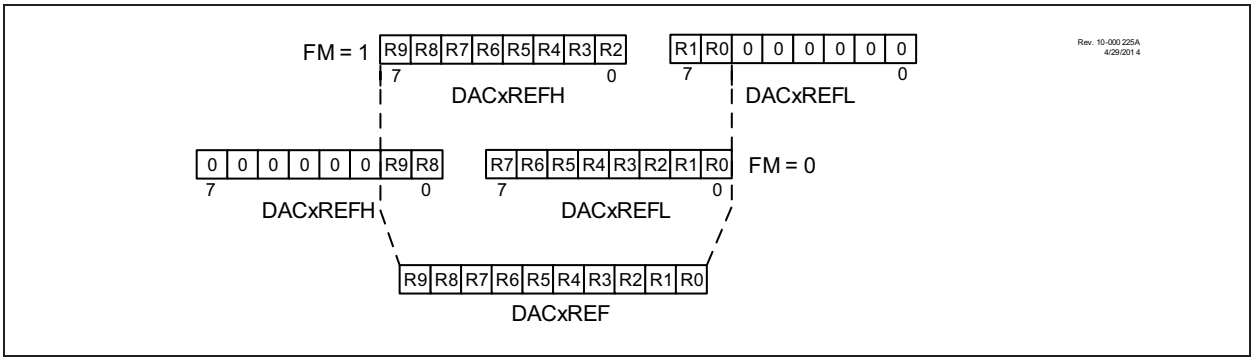
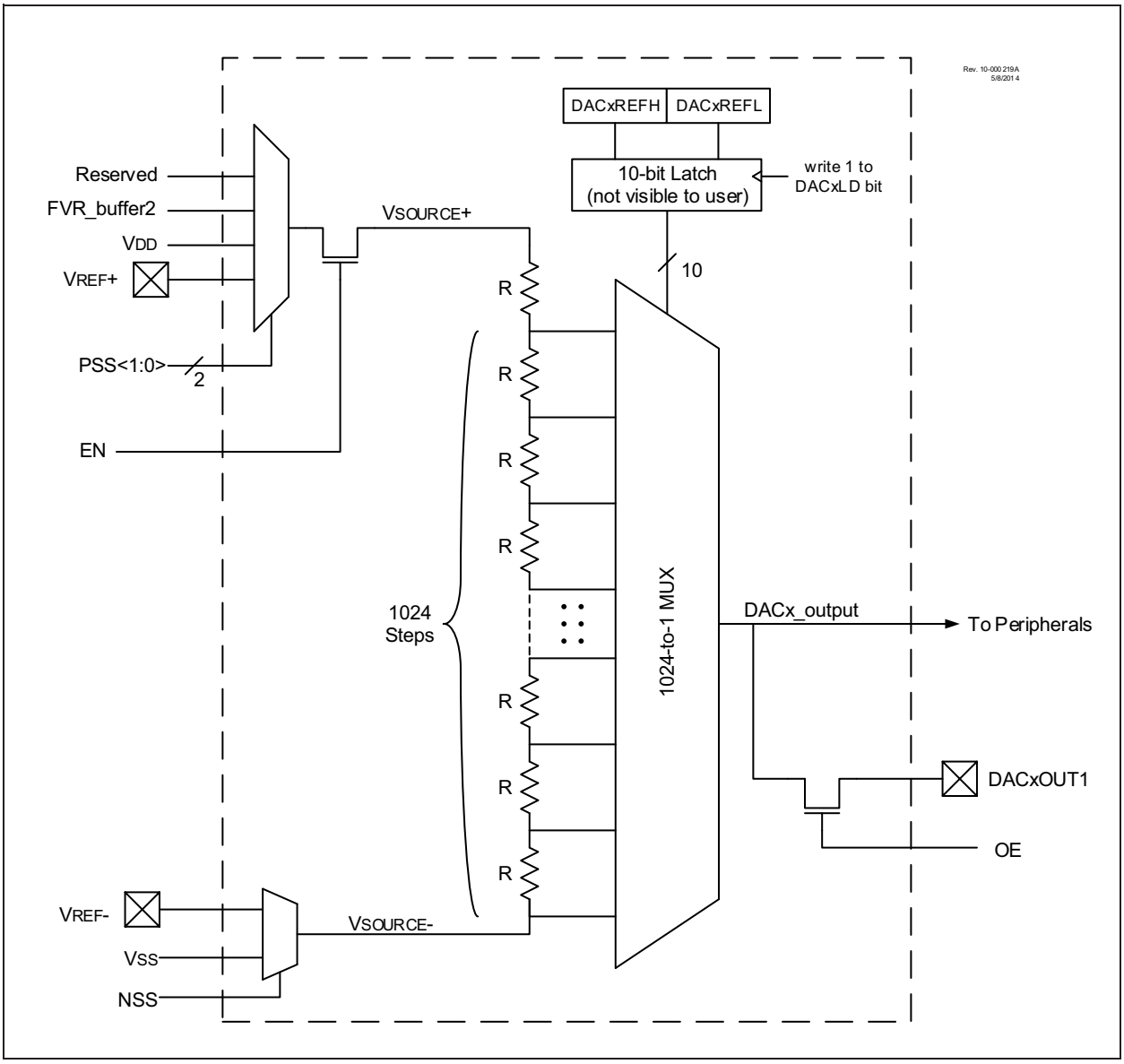


FIGURE 18-2: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM



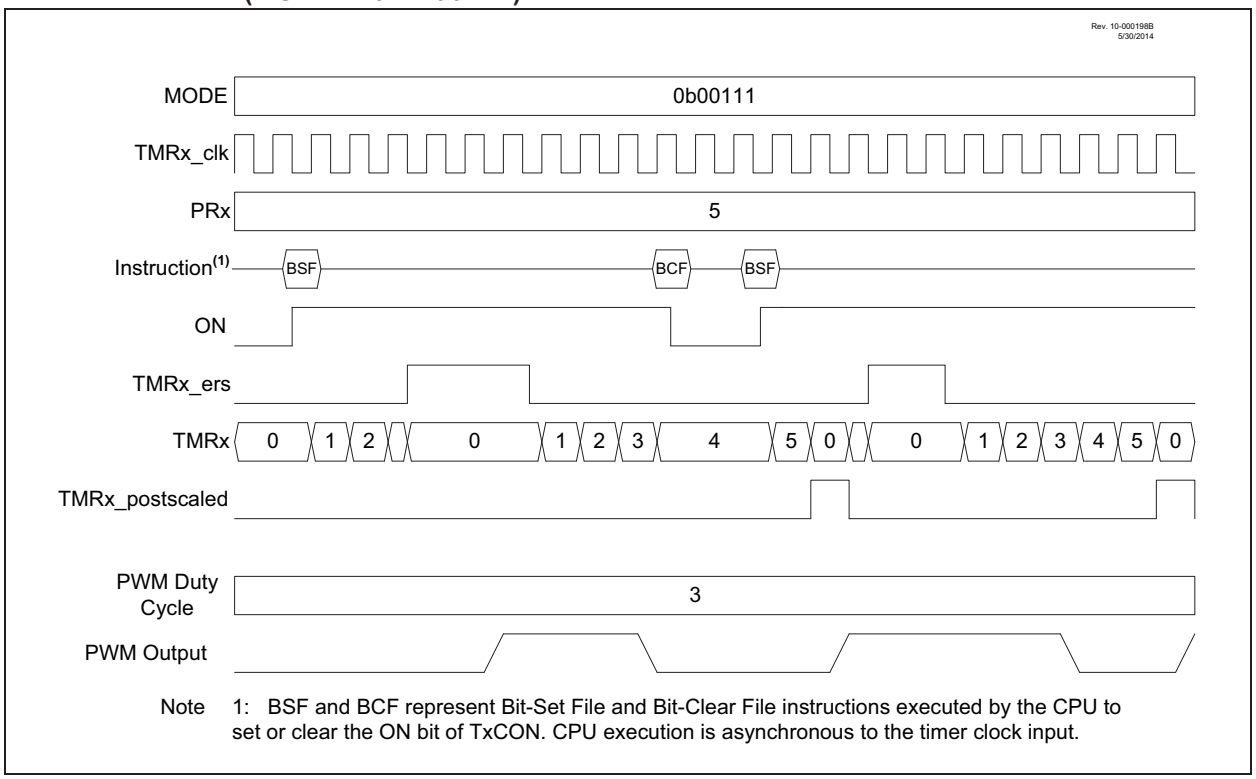
23.6.4 LEVEL-TRIGGERED HARDWARE LIMIT MODE

In the Level-Triggered Hardware Limit Timer modes, the counter is reset by high or low levels of the external signal, TMRx_ers, as shown in Figure 23-7. Selecting MODE<4:0> = 00110 will cause the timer to reset on a low-level external signal. Selecting MODE<4:0> = 00111 will cause the timer to reset on a high-level external signal. In the example, the counter is reset while TMRx_ers = 1. ON is controlled by BSF and BCF instructions. When ON = 0, the external signal is ignored.

When the CCP uses the timer as the PWM time base, then the PWM output will be set high when the timer starts counting and then set low only when the timer count matches the CCPRx value. The timer is reset when either the timer count matches the PRx value or two clock periods after the external Reset signal goes true and stays true.

The timer starts counting, and the PWM output is set high, on either the clock following the PRx match or two clocks after the external Reset signal relinquishes the Reset. The PWM output will remain high until the timer counts up to match the CCPRx pulse-width value. If the external Reset signal goes true while the PWM output is high then the PWM output will remain high until the Reset signal is released allowing the timer to count up to match the CCPRx value.

FIGURE 23-7: LEVEL-TRIGGERED HARDWARE LIMIT MODE TIMING DIAGRAM (MODE<4:0> = 00111)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

24.4 CCP/PWM Clock Selection

The PIC16(L)F1764/5/8/9 allows each individual CCP and PWM module to select the timer source that controls the module. Each module has an independent selection.

As there are up to three 8-bit timers with auto-reload (Timer2/4/6), the PWM mode on the CCP and PWM modules can use any of these timers.

The CCPTMRS register is used to select which timer is used.

24.4.1 USING THE TMR2/4/6 WITH THE CCP MODULE

This device has a new version of the TMR2 module that has many new modes, which allow for greater customization and control of the PWM signals than older parts. Refer to **Section 23.6 "Operation Examples"** for examples of PWM signal generation using the different modes of Timer2. The CCP operation requires that the timer used as the PWM time base has the FOSC/4 clock source selected.

24.4.2 PWM PERIOD

The PWM period is specified by the T2PR/T4PR/T6PR register of Timer2/4/6. The PWM period can be calculated using the formula of Equation 24-1.

EQUATION 24-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \bullet 4 \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

Note 1: TOSC = 1/FOSC.

When TMR2/4/6 is equal to its respective T2PR/T4PR/T6PR register, the following three events occur on the next increment cycle:

- TMR2/4/6 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from the CCPRxH:CCPRxL pair into the internal 10-bit latch.

Note: The Timer postscaler (see Figure 24-1) is not used in the determination of the PWM frequency.

24.4.3 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to two registers: the CCPRxH:CCPRxL register pair. Where the particular bits go is determined by the FMT bit of the CCPxCON register. If FMT = 0, the two Most Significant bits of the duty cycle value should be written to bits<1:0> of the CCPRxH register and the remaining eight bits to the CCPRxL register. If FMT = 1, the Least Significant two bits of the duty cycle should be written to bits<7:6> of the CCPRxL register and the Most Significant eight bits to the CCPRxH register. This is illustrated in Figure 24-4. These bits can be written at any time. The duty cycle value is not latched into the internal latch until after the period completes (i.e., a match between T2PR/T4PR/T6PR and TMR2/4/6 registers occurs).

Equation 24-2 is used to calculate the PWM pulse width. Equation 24-3 is used to calculate the PWM duty cycle ratio.

EQUATION 24-2: PULSE WIDTH

$$Pulse\ Width = CCPRxH:CCPRxL \bullet TOSC \bullet (TMR2\ Prescale\ Value)$$

EQUATION 24-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxH:CCPRxL)}{4(PRx + 1)}$$

The PWM Duty Cycle registers are double-buffered for glitchless PWM operation.

The 8-bit timer TMR2/4/6 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2/4/6 prescaler is set to 1:1.

When the 10-bit time base matches the internal buffer register, then the CCPx pin is cleared (see Figure 24-3).

FIGURE 24-4: CCPx DUTY CYCLE ALIGNMENT

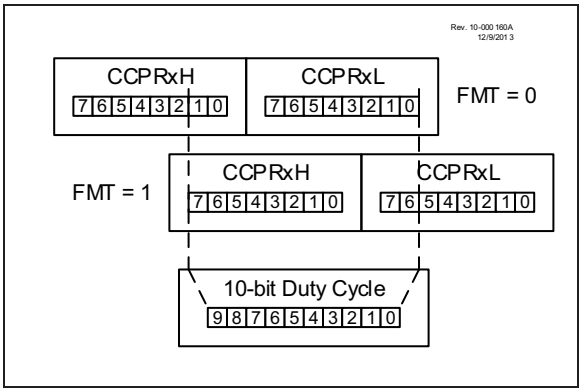
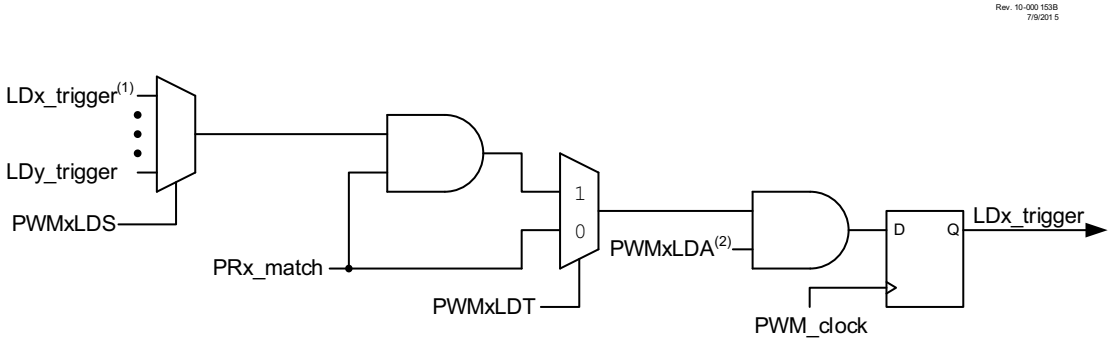


FIGURE 26-2: LOAD TRIGGER BLOCK DIAGRAM



Note 1. The input corresponding to a PWM module's own load trigger is reserved.
2. PWMxLDA is cleared by hardware upon LDx_trigger.

26.1 Fundamental Operation

The PWM module produces a 16-bit resolution Pulse-Width Modulated output.

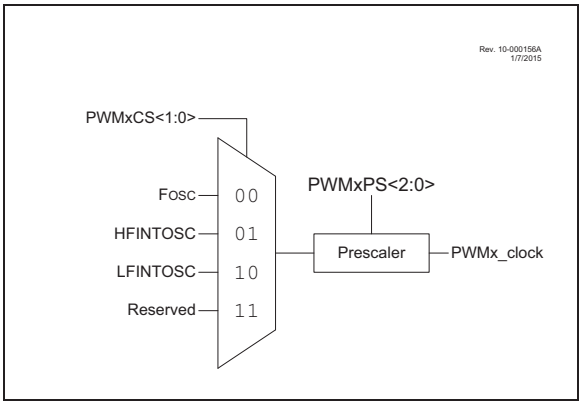
Each PWM module has an independent timer driven by a selection of clock sources determined by the PWMxCLKCON register (Register 26-4). The timer value is compared to Event Count registers to generate the various events of a the PWM waveform, such as the period and duty cycle. For a block diagram describing the clock sources, refer to Figure 26-3.

Each PWM module can be enabled individually using the EN bit of the PWMxCON register, or several PWM modules can be enabled simultaneously using the MPWMxEN bits of the PWMEN register.

The current state of the PWM output can be read using the OUT bit of the PWMxCON register. In some modes, this bit can be set and cleared by software, giving additional software control over the PWM waveform. This bit is synchronized to FOSC/4 and therefore, does not change in real time with respect to the PWM_clock.

Note:	If PWM_clock > FOSC/4, the OUT bit may not accurately represent the output state of the PWM.

FIGURE 26-3: PWMx CLOCK SOURCE BLOCK DIAGRAM



26.1.1 PWMx PIN CONFIGURATION

This device uses the PPS control circuitry to route peripherals to any device I/O pin. Select the desired pin, or pins, for PWM output with the device pin, using the RxyPPS control register (Register 12-2).

All PWM outputs are multiplexed with the PORT data latch, so the pins must also be configured as outputs by clearing the associated PORT TRISx bits.

The slew rate feature may be configured to optimize the rate to be used in conjunction with the PWM _outputs. High-speed output switching is attained by clearing the associated PORT SLRCONx bits.

The PWM outputs can be configured to be open-drain outputs by setting the associated PORT ODCONx bits.

26.1.2 PWMx Output Polarity

The output polarity is inverted by setting the POL bit of the PWMxCON register. The polarity control affects the PWM output even when the module is not enabled.

TABLE 26-2: SUMMARY OF REGISTERS ASSOCIATED WITH PWMx

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		84
PWMEN	—	—	MPWM6EN(1)	MPWM5EN	—	—	—	—	291
PWMLD	—	—	MPWM6LD(1)	MPWM5LD	—	—	—	—	291
PWMOUT	—	—	MPWM6OUT(1)	MPWM5OUT	—	—	—	—	291
PWM5PHL	PH<7:0>								286
PWM5PHH	PH<15:8>								286
PWM5DCL	DC<7:0>								287
PWM5DCH	DC<15:8>								287
PWM5PRH	PR<15:8>								288
PWM5PRL	PR<7:0>								288
PWM5OFH	OF<15:8>								289
PWM5OFL	OF<7:0>								289
PWM5TMRH	TMR<15:8>								290
PWM5TMRL	TMR<7:0>								290
PWM5CON	EN	—	OUT	POL	MODE<1:0>		—	—	280
PWM5INTE	—	—	—	—	OFIE	PHIE	DCIE	PRIE	281
PWM5INTF	—	—	—	—	OFIF	PHIF	DCIF	PRIF	282
PWM5CLKCON	—	PS<2:0>			—	—	CS<1:0>		283
PWM5LDCON	LDA	LDT(1)	—	—	—	—	—	LDS(1)	284
PWM5OFCON	—	OFM<1:0>(1)		OFO	—	—	—	OFS(1)	285
PWM6PHL(1)	PH<7:0>								286
PWM6PHH(1)	PH<15:8>								286
PWM6DCL(1)	DC<7:0>								287
PWM6DCH(1)	DC<15:8>								287
PWM6PRL(1)	PR<7:0>								288
PWM6PRH(1)	PR<15:8>								288
PWM6OFL(1)	OF<7:0>								289
PWM6OFH(1)	OF<15:8>								289
PWM6TMRL(1)	TMR<7:0>								290
PWM6TMRH(1)	TMR<15:8>								290
PWM6CON(1)	EN	—	OUT	POL	MODE<1:0>		—	—	280
PWM6INTE(1)	—	—	—	—	OFIE	PHIE	DCIE	PRIE	281
PWM6INTF(1)	—	—	—	—	OFIF	PHIF	DCIF	PRIF	282
PWM6CLKCON(1)	—	PS<2:0>			—	—	CS<1:0>		283
PWM6LDCON(1)	LDA	LDT(1)	—	—	—	—	—	LDS(1)	284
PWM6OFCON(1)	—	OFM<1:0>(1)		OFO	—	—	—	OFS(1)	285

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PWM.

Note 1: PIC16(L)F1768/9 only

TABLE 26-3: SUMMARY OF CONFIGURATION WORDS WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	63
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

FIGURE 27-12: FULL-BRIDGE FORWARD MODE COG OPERATION WITH CCP1

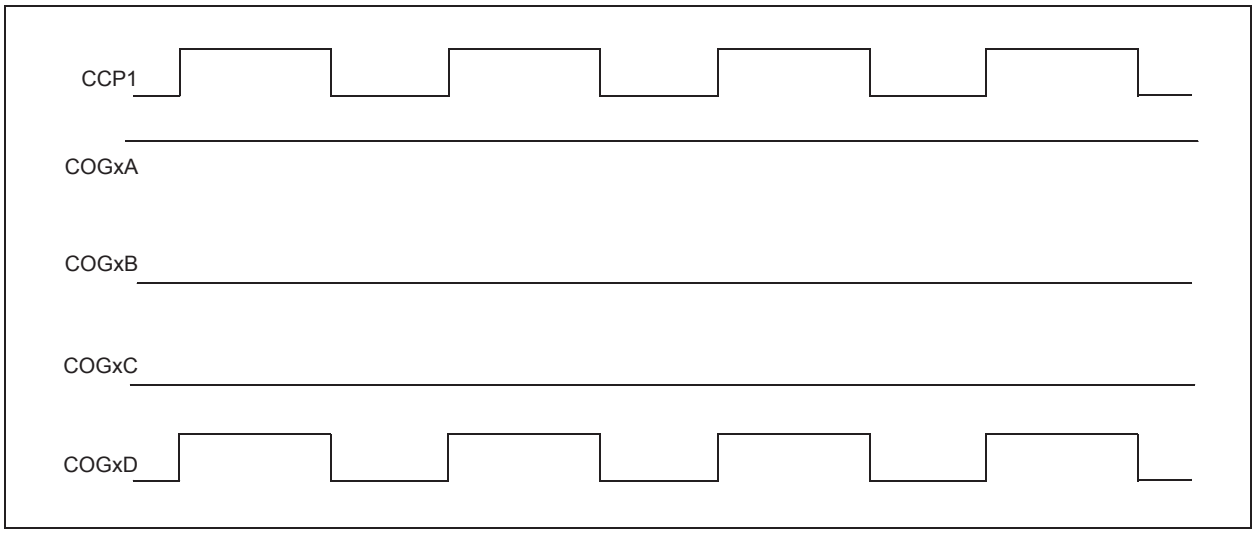
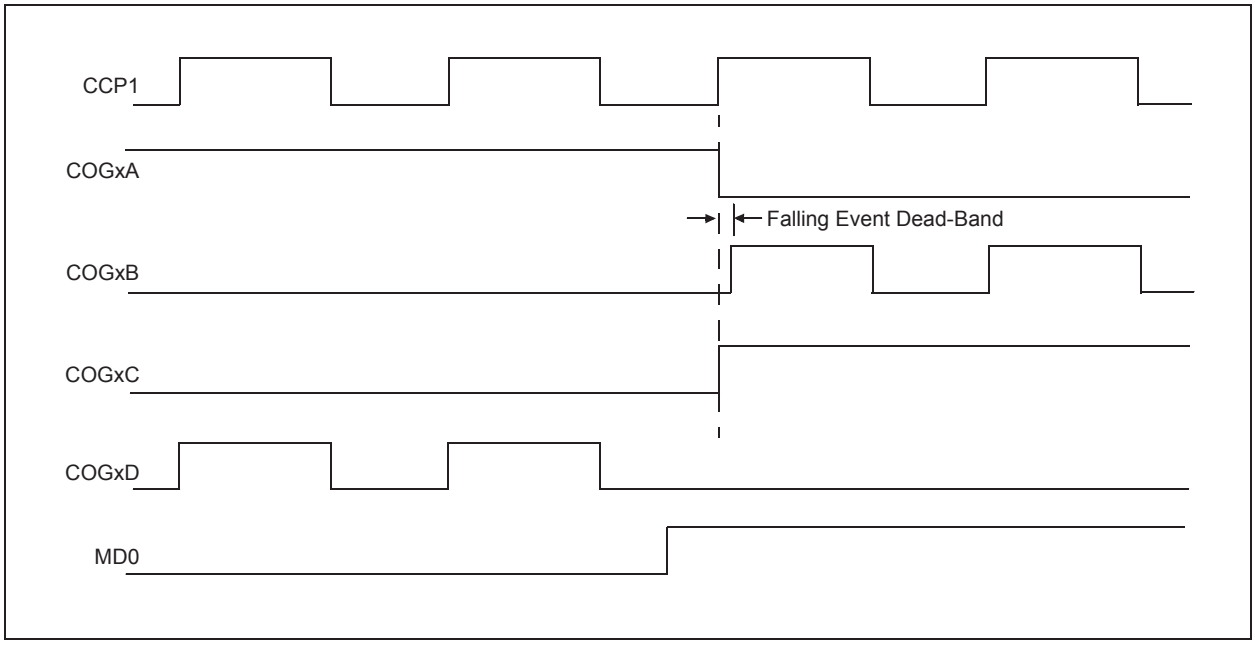


FIGURE 27-13: FULL-BRIDGE MODE COG OPERATION WITH CCP1 AND DIRECTION CHANGE



27.4 Clock Sources

The COG_clock is used as the reference clock to the various timers in the peripheral. Timers that use the COG_clock include:

- Rising and falling dead-band time
- Rising and falling blanking time
- Rising and falling event phase delay

Clock sources available for selection include:

- 16 MHz HFINTOSC (active during Sleep)
- Instruction clock (FOSC/4)
- System clock (FOSC)

The clock source is selected with the CS<1:0> bits of the COGxCON0 register (Register 27-1).

27.5 Selectable Event Sources

The COG uses any combination of independently selectable event sources to generate the complementary waveform. Sources fall into two categories:

- Rising event sources
- Falling event sources

The rising event sources are selected by setting bits in the COGxRIS0 and COGxRIS1 registers (Register 27-3 and Register 27-4). The falling event sources are selected by setting bits in the COGxFIS0 and COGxF1 registers (Register 27-7 and Register 27-8). All selected sources are OR'd together to generate the corresponding event signal. Refer to Figure 27-7.

27.5.1 EDGE vs. LEVEL SENSING

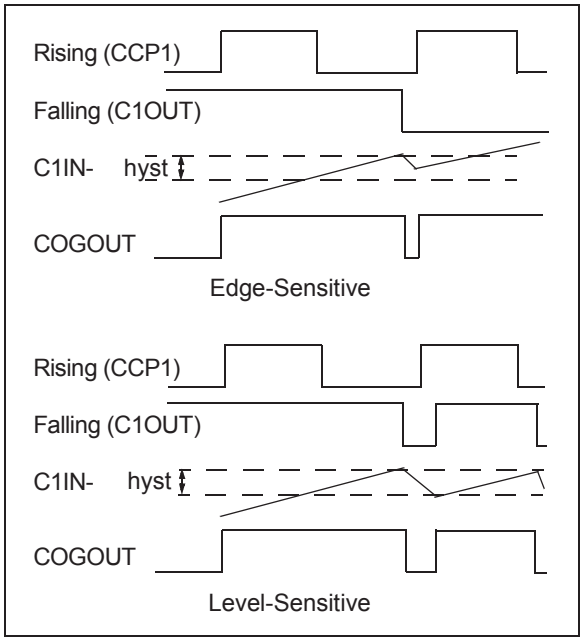
Event input detection may be selected as level or edge-sensitive. The Detection mode is individually selectable for every source. Rising Source Detection modes are selected with the COGxRSIM0 and COGxRSIM1 registers (Register 27-5 and Register 27-6). Falling Source Detection modes are selected with the COGxFSIM0 and COGxFSIM1 registers (Register 27-9 and Register 27-10). A set bit selects edge detection for the corresponding event source. A cleared bit selects level detection.

In general, events that are driven from a periodic source should be edge-detected and events that are derived from voltage thresholds at the target circuit should be level-sensitive. Consider the following two examples:

1. The first example is an application in which the period is determined by a 50% duty cycle clock on the rising event input and the COG output duty cycle is determined by a voltage level fed back through a comparator on the falling event input. If the clock input is level-sensitive, duty cycles less than 50% will exhibit erratic operation because the level-sensitive clock will suppress the comparator feedback.

2. The second example is similar to the first except that the duty cycle is close to 100%. The feedback comparator high-to-low transition trips the COG drive off, but almost immediately the period source turns the drive back on. If the off cycle is short enough, the comparator input may not reach the low side of the hysteresis band precluding an output change. The comparator output stays low and without a high-to-low transition to trigger the edge sense, the drive of the COG output will be stuck in a constant drive-on condition. See Figure 27-14.

FIGURE 27-14: EDGE vs. LEVEL SENSE



REGISTER 27-5: COGxRSIM0: COGx RISING EVENT SOURCE INPUT MODE REGISTER 0 (CONTINUED)

bit 1 **RSIM1:** COGx Rising Event Input Source 1 Mode bit

RIS1 = 1:

1 = Comparator 1 low-to-high transition will cause a rising event after rising event phase delay
0 = Comparator 1 high level will cause an immediate rising event

RIS1 = 0:

Comparator 1 has no effect on rising event.

bit 0 **RSIM0:** COGx Rising Event Input Source 0 Mode bit

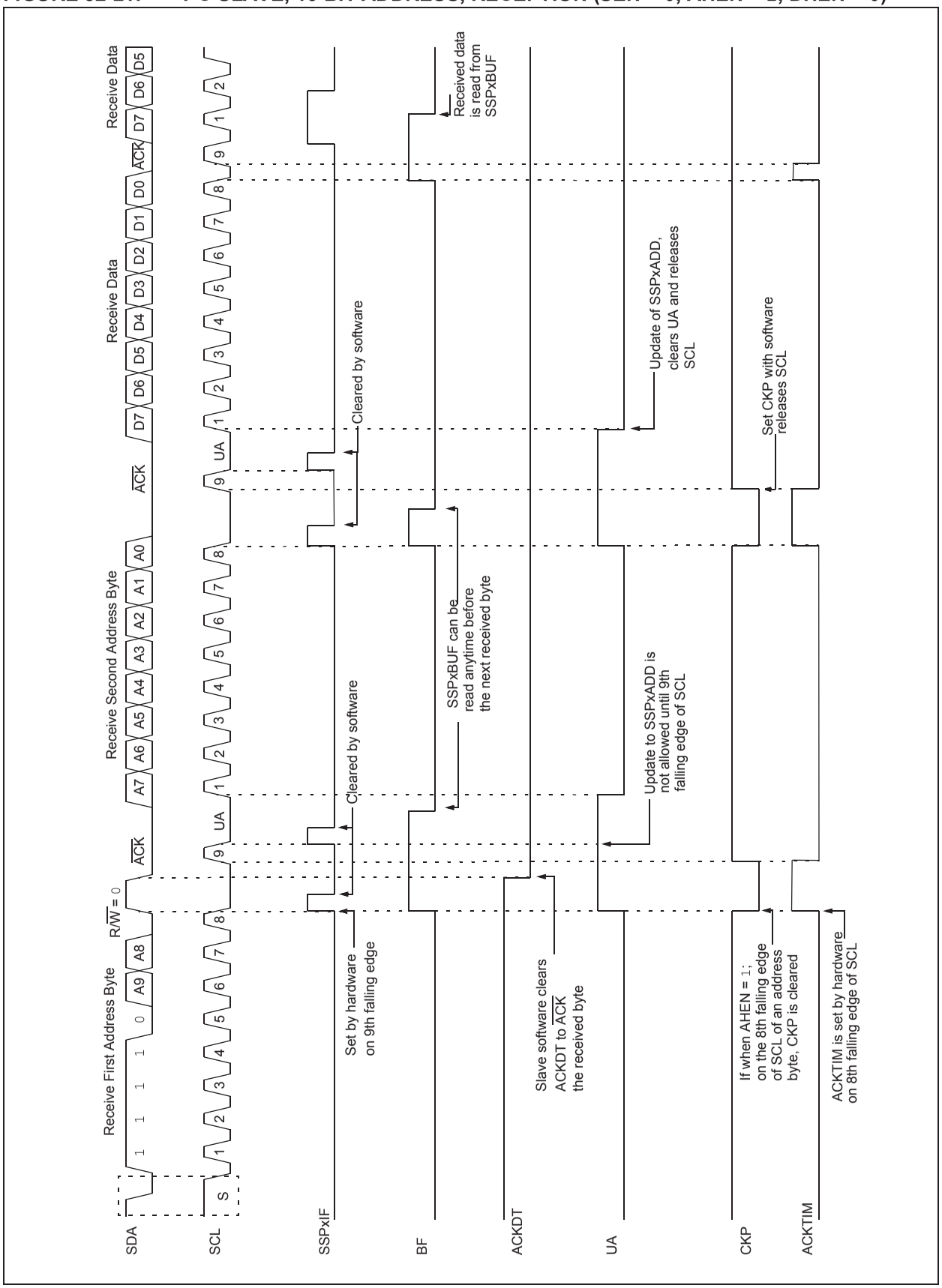
RIS0 = 1:

1 = Pin selected with COGxINPPS register low-to-high transition will cause a rising event after rising event phase delay
0 = Pin selected with COGxINPPS register high level will cause an immediate rising event

RIS0 = 0:

Pin selected with COGxINPPS register has no effect on rising event.

FIGURE 32-21: I²C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 1, DHEN = 0)



32.8 Register Definitions: MSSP Control

REGISTER 32-1: SSP1STAT: MSSP STATUS REGISTER

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **SMP:** SPI Data Input Sample bit

SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time

SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode.

In I^2C Master or Slave mode:
1 = Slew rate control is disabled for Standard Speed mode (100 kHz and 1 MHz)
0 = Slew rate control is enabled for High-Speed mode (400 kHz)

bit 6 **CKE:** SPI Clock Edge Select bit (SPI mode only)

In SPI Master or Slave mode:
1 = Transmit occurs on transition from active to Idle clock state
0 = Transmit occurs on transition from Idle to active clock state

In I^2C mode only:
1 = Enables input logic so that thresholds are compliant with SMBus specification
0 = Disables SMBus specific inputs

bit 5 **D/$\overline{A}$:** Data/$\overline{Address}$ bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P:** Stop bit (I^2C mode only; this bit is cleared when the MSSP module is disabled, SSPEN is cleared)
1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset)
0 = Stop bit was not detected last

bit 3 **S:** Start bit (I^2C mode only; this bit is cleared when the MSSP module is disabled, SSPEN is cleared)
1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset)
0 = Start bit was not detected last

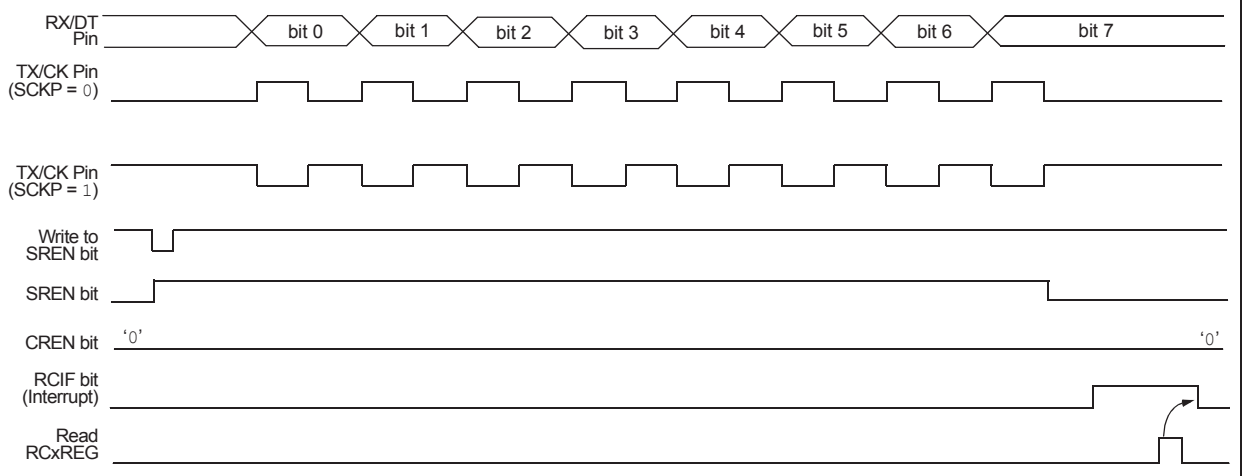
bit 2 **R/$\overline{W}$:** Read/$\overline{Write}$ bit information (I^2C mode only)
This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or not $\overline{ACK}$ bit.

In I^2C Slave mode:
1 = Read
0 = Write

In I^2C Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
ORing this bit with SEN, RSEN, PEN, RCEN or ACKEN will indicate if the MSSP is in Idle mode.

bit 1 **UA:** Update Address bit (10-bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPxADD register
0 = Address does not need to be updated

FIGURE 33-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

TABLE 33-8: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELB(1)	ANSB<7:4>				—	—	—	—	143
ANSELC	ANSC<7:6>(1)		—	—	ANSC<3:0>				148
BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	442
CKPPS	—	—	—	CKPPS<4:0>					154, 156
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	102
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	105
RC1REG	EUSART Receive Data Register								436*
RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	441
RXPPS	—	—	—	RXPPS<4:0>					154, 156
RxyPPS	—	—	—	RxyPPS<4:0>					154
SP1BRGL	BRG<7:0>								443*
SP1BRGH	BRG<15:8>								443*
TRISA	—	—	TRISA<5:4>		—(2)	TRISA<2:0>			136
TRISB(1)	TRISB<7:4>				—	—	—	—	142
TRISC	TRISC<7:6>(1)		TRISC<5:0>						147
TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	440

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous master reception.

* Page provides register information.

Note 1: PIC16(L)F1768/9 only.

2: Unimplemented, read as '1'.

TABLE 36-4: I/O PORTS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
	V_{IL}	**Input Low Voltage**					
		I/O Ports:					
D034		with TTL Buffer	—	—	0.8	V	$4.5V \le V_{DD} \le 5.5V$
D034A			—	—	$0.15\ V_{DD}$	V	$1.8V \le V_{DD} \le 4.5V$
D035		with Schmitt Trigger Buffer	—	—	$0.2\ V_{DD}$	V	$2.0V \le V_{DD} \le 5.5V$
		with I^2C Levels	—	—	$0.3\ V_{DD}$	V	
		with SMBus Levels	—	—	0.8	V	$2.7V \le V_{DD} \le 5.5V$
D036		$\overline{MCLR}$, OSC1 (EXTRC mode)	—	—	$0.2\ V_{DD}$	V	**(Note 1)**
D036A		OSC1 (HS mode)	—	—	$0.3\ V_{DD}$	V	
	V_{IH}	**Input High Voltage**					
		I/O Ports:					
D040		with TTL Buffer	2.0	—	—	V	$4.5V \le V_{DD} \le 5.5V$
D040A			$0.25\ V_{DD} + 0.8$	—	—	V	$1.8V \le V_{DD} \le 4.5V$
D041		with Schmitt Trigger Buffer	$0.8\ V_{DD}$	—	—	V	$2.0V \le V_{DD} \le 5.5V$
		with I^2C Levels	$0.7\ V_{DD}$	—	—	V	
		with SMBus Levels	2.1	—	—	V	$2.7V \le V_{DD} \le 5.5V$
D042		$\overline{MCLR}$	$0.8\ V_{DD}$	—	—	V	
D043A		OSC1 (HS mode)	$0.7\ V_{DD}$	—	—	V	
D043B		OSC1 (EXTRC oscillator)	$0.9\ V_{DD}$	—	—	V	$V_{DD} > 2.0V$ **(Note 1)**
	I_{IL}	**Input Leakage Current(2)**					
D060		I/O Ports	—	± 5	± 125	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, +85°C
			—	± 5	± 1000	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, +125°C
D061		$\overline{MCLR}$(3)	—	± 50	± 200	nA	$V_{SS} \le V_{PIN} \le V_{DD}$, Pin at high-impedance, +85°C
	I_{PUR}	**Weak Pull-up Current**					
D070*			25	100	200	µA	V_{DD} = 3.3V, $V_{PIN} = V_{SS}$
			25	140	300	µA	V_{DD} = 5.0V, $V_{PIN} = V_{SS}$
	V_{OL}	**Output Low Voltage(4)**					
D080		Standard I/O ports	—	—	0.6	V	I_{OL} = 8mA, V_{DD} = 5V I_{OL} = 6mA, V_{DD} = 3.3V I_{OL} = 1.8mA, V_{DD} = 1.8V
D080A		High Drive I/O ports	—	—	0.6	V	I_{OH} = 10mA, V_{DD} = 2.3V, HIDCx = 1
			—	0.6	—	V	I_{OH} = 32mA, V_{DD} = 3.0V, HIDCx = 1
			—	0.6	—	V	I_{OH} = 51mA, V_{DD} = 5.0V, HIDCx = 1

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in EXTRC mode.

2: Negative current is defined as current sourced by the pin.

3: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

4: Including OSC2 in CLKOUT mode.

TABLE 36-6: THERMAL CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)					
Param No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	70.0	°C/W	14-pin PDIP package
			95.3	°C/W	14-pin SOIC package
			100.0	°C/W	14-pin TSSOP package
			51.5	°C/W	16-pin QFN 4x4 mm package
			62.2	°C/W	20-pin PDIP package
			87.3	°C/W	20-pin SSOP
			77.7	°C/W	20-pin SOIC package
			43.0	°C/W	20-pin QFN 4x4 mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	32.75	°C/W	14-pin PDIP package
			31.0	°C/W	14-pin SOIC package
			24.4	°C/W	14-pin TSSOP package
			5.4	°C/W	16-pin QFN 4x4 mm package
			27.5	°C/W	20-pin PDIP package
			31.1	°C/W	20-pin SSOP
			23.1	°C/W	20-pin SOIC package
			5.3	°C/W	20-pin QFN 4x4 mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ (1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \Sigma (I_{OL} * V_{OL}) + \Sigma (I_{OH} * (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = P_{DMAX} (T_J - T_A)/\theta_{JA}$ (2)

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.

2: T_A = Ambient Temperature, T_J = Junction Temperature.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

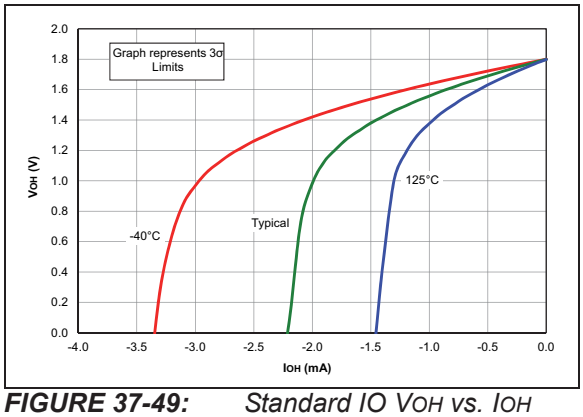


FIGURE 37-49: *Standard IO VOH vs. IOH Over Temperature, VDD = 1.8V, PIC16LF1764/5/8/9 Only.*

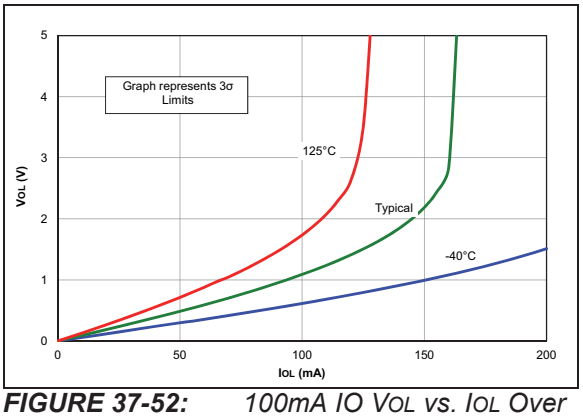


FIGURE 37-52: *100mA IO VOL vs. IOL Over Temperature, VDD = 5.5V, PIC16F1764/5/8/9 Only.*

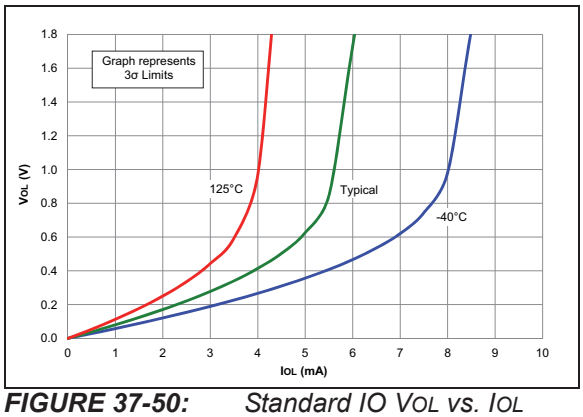


FIGURE 37-50: *Standard IO VOL vs. IOL Over Temperature, VDD = 1.8V, PIC16LF1764/5/8/9 Only.*

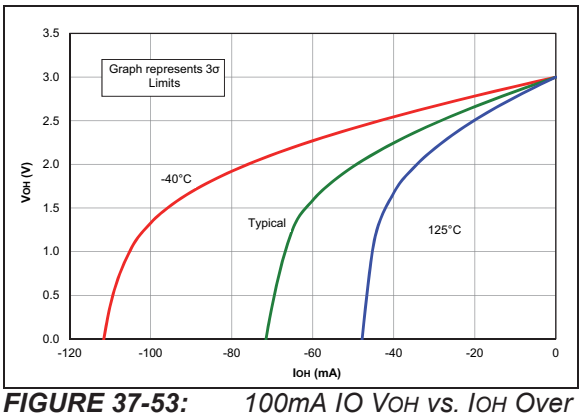


FIGURE 37-53: *100mA IO VOH vs. IOH Over Temperature, VDD = 3.0V.*

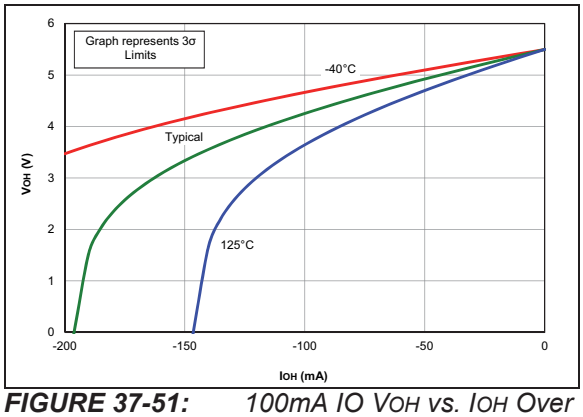


FIGURE 37-51: *100mA IO VOH vs. IOH Over Temperature, VDD = 5.5V, PIC16F1764/5/8/9 Only.*

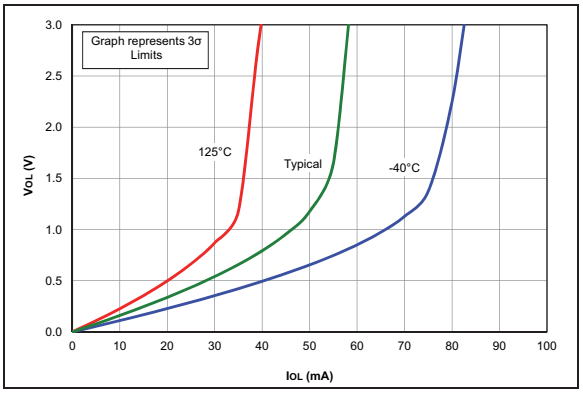
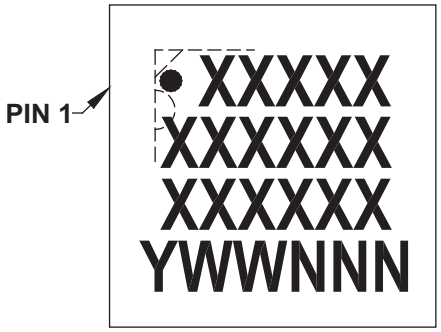


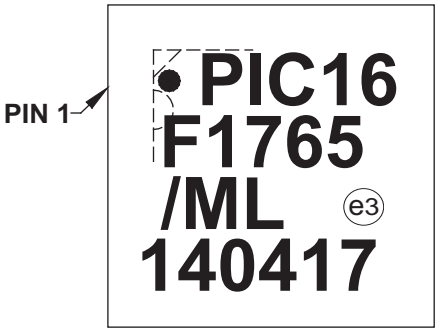
FIGURE 37-54: *VOL vs. IOL Over Temperature, VDD = 3.0V.*

Package Marking Information (Continued)

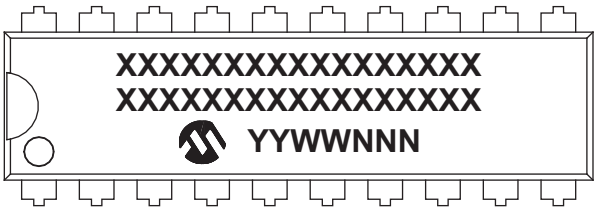
16-Lead QFN (4x4x0.9 mm)



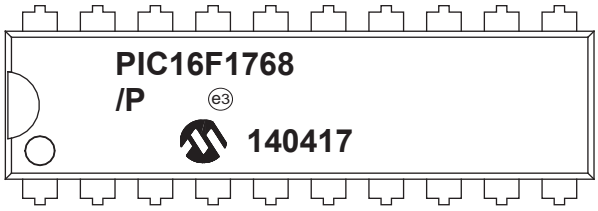
Example



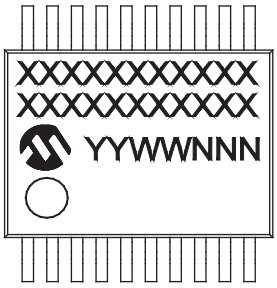
20-Lead PDIP (300 mil)



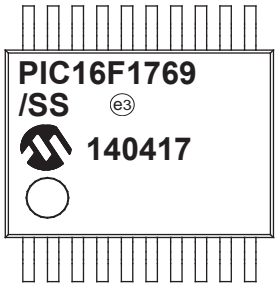
Example



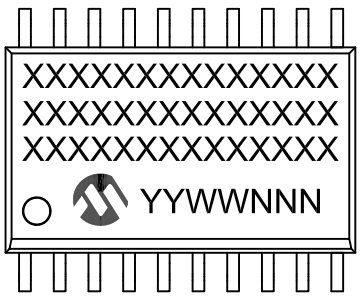
20-Lead SSOP (5.30 mm)



Example



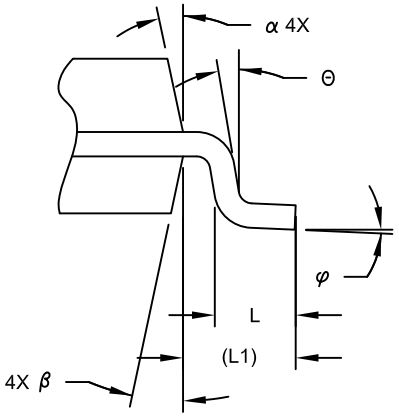
20-Lead SOIC (7.50 mm)



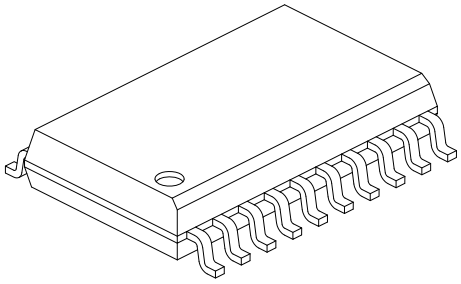
Example

20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E		10.30 BSC	
Molded Package Width	E1		7.50 BSC	
Overall Length	D		12.80 BSC	
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1		1.40 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-094C Sheet 2 of 2

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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