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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1769-e-so

TABLE 4: 20-PIN ALLOCATION TABLE (PIC16(L)F1768/9) (CONTINUED)

I/O	20-Pin PDIP/SOIC/SSOP	20-Pin QFN	ADC	Reference	DAC	Op Amp	Comparator	Zero Cross	Programmable Ramp Generator	Timers	PWM	CCP	COG	CLC	Modulator	EUSART	MSSP	Interrupts	Pull-ups	Hi Current	Basic
RC3	7	4	AN7	—	—	OPA2OUT OPA1IN1- OPA1IN1+	C1IN3- C2IN3- C3IN3- C4IN3-	—	PRG2IN0 PRG1IN1	T5G(1)	—	CCP2(1)	—	CLCIN0(1)	—	—	—	IOC	Y	—	—
RC4	6	3	—	—	—	—	—	—	PRG1R(1) PRG2R(1)	T3G(1)	—	—	—	CLCIN1(1)	—	—	—	IOC	Y	Y	—
RC5	5	2	—	—	—	—	—	—	PRG1F(1) PRG2F(1)	T3CKI(1)	—	CCP1(1)	—	—	—	—	—	IOC	Y	Y	—
RC6	8	5	AN8	—	—	OPA2IN0-	—	—	—	—	—	—	—	—	—	—	$\overline{SS}$(1)	IOC	Y	—	—
RC7	9	6	AN9	—	—	OPA2IN0+	—	—	—	—	—	—	—	—	—	—	—	IOC	Y	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—		
OUT(2)	—	—	—	—	—	—	C1OUT	—	—	—	PWM3	CCP1	COG1A	CLC1OUT	MD1OUT	DT(3)	SDO	—	—	—	—
	—	—	—	—	—	—	C2OUT	—	—	—	PWM4	CCP2	COG1B	CLC2OUT	MD2OUT	TX	SDA(3)	—	—	—	—
	—	—	—	—	—	—	C3OUT	—	—	—	PWM5	—	COG1C	CLC3OUT	—	CK	SCK	—	—	—	—
	—	—	—	—	—	—	C4OUT	—	—	—	PWM6	—	COG1D	—	—	—	SCL(3)	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2A	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2B	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2C	—	—	—	—	—	—	—	—
	—	—	—	—	—	—	—	—	—	—	—	—	COG2D	—	—	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS Input Selection register. See Table 12-1.
2: All pin outputs default to PORT latch data. Any input capable pin can be selected as a digital peripheral output with the PPS Output Selection registers. See Table 12-2.
3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.
4: Input only.

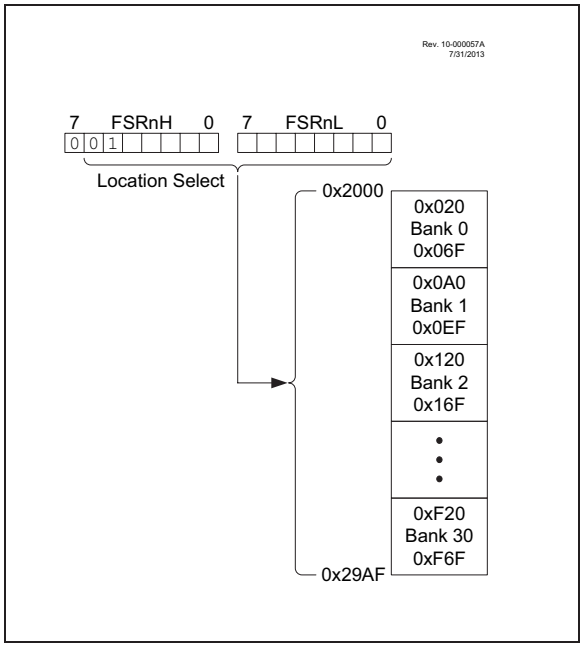
3.6.2 LINEAR DATA MEMORY

The linear data memory is the region from FSRn address, 0x2000, to FSRn address, 0x29AF. This region is a virtual region that points back to the 80-byte blocks of GPR memory in all the banks.

Unimplemented memory reads as 0x00. Use of the linear data memory region allows buffers to be larger than 80 bytes because incrementing the FSRn beyond one bank will go directly to the GPR memory of the next bank.

The 16 bytes of common memory are not included in the linear data memory region.

FIGURE 3-10: LINEAR DATA MEMORY MAP



3.6.3 PROGRAM FLASH MEMORY

To make constant data access easier, the entire Program Flash Memory is mapped to the upper half of the FSRn address space. When the MSB of FSRnH is set, the lower 15 bits are the address in program memory which will be accessed through INDFn. Only the lower eight bits of each memory location are accessible via INDFn. Writing to the Program Flash Memory cannot be accomplished via the FSRn/INDFn interface. All instructions that access Program Flash Memory via the FSRn/INDFn interface will require one additional instruction cycle to complete.

FIGURE 3-11: PROGRAM FLASH MEMORY MAP

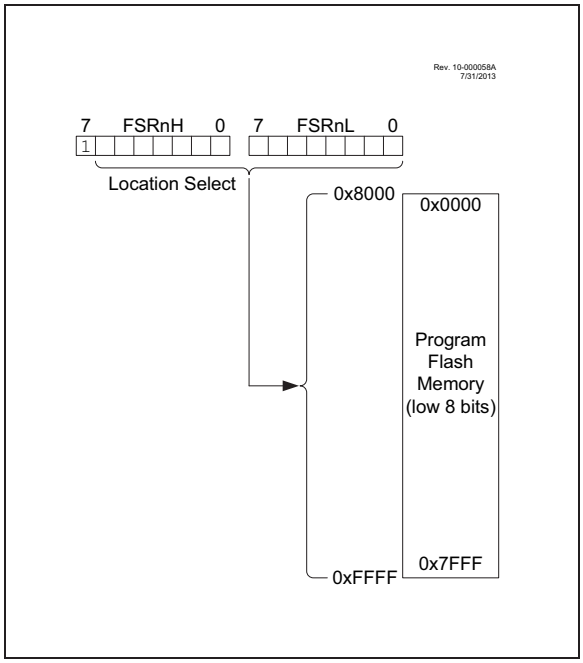


TABLE 6-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	90
PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	94
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	27
WDTCON	—	—	WDTPS<4:0>					SWDTEN	115

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

REGISTER 7-5: PIR1: PERIPHERAL INTERRUPT REQUEST REGISTER 1

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **TMR1GIF:** Timer1 Gate Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 6 **ADIF:** Analog-to-Digital Converter (ADC) Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 5 **RCIF:** EUSART Receive Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 4 **TXIF:** EUSART Transmit Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 3 **SSP1IF: Master** Synchronous Serial Port (MSSP) Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 1 **TMR2IF:** Timer2 to T2PR Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

bit 0 **TMR1IF:** Timer1 Overflow Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

10.0 FLASH PROGRAM MEMORY CONTROL

The Flash program memory is readable and writable during normal operation over the full VDD range. Program memory is indirectly addressed using Special Function Registers (SFRs). The SFRs used to access program memory are:

- PMCON1
- PMCON2
- PMDATL
- PMDATH
- PMADRL
- PMADRH

When accessing the program memory, the PMDATH:PMDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the PMADRH:PMADRL register pair forms a 2-byte word that holds the 15-bit address of the program memory location being read.

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the operating voltage range of the device.

The Flash program memory can be protected in two ways: by code protection ($\overline{CP}$ bit in the Configuration Words) and write protection (WRT<1:0> bits in the Configuration Words).

Code protection ($\overline{CP}$ = 0) disables access, reading and writing to the Flash program memory via external device programmers. Code protection does not affect the self-write and erase functionality. Code protection can only be reset by a device programmer performing a bulk erase to the device, clearing all Flash program memory, Configuration bits and User IDs.(1)

Write protection prohibits self-write and erase to a portion or all of the Flash program memory, as defined by the WRT<1:0> bits. Write protection does not affect a device programmer's ability to read, write or erase the device.

Note 1:	Code protection of the entire Flash program memory array is enabled by clearing the $\overline{CP}$ bit of the Configuration Words.

10.1 PMADRL and PMADRH Registers

The PMADRH:PMADRL register pair can address up to a maximum of 32K words of program memory. When selecting a program address value, the MSB of the address is written to the PMADRH register and the LSB is written to the PMADRL register.

10.1.1 PMCON1 AND PMCON2 REGISTERS

PMCON1 is the control register for Flash program memory accesses.

Control bits, RD and WR, initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared by hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

The PMCON2 register is a write-only register. Attempting to read the PMCON2 register will return all '0's.

To enable writes to the program memory, a specific pattern (the unlock sequence), must be written to the PMCON2 register. The required unlock sequence prevents inadvertent writes to the program memory write latches and Flash program memory.

10.2 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum size that can be erased by user software.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the PMDATH:PMDATL register pair.

Note:	If the user wants to modify only a portion of a previously programmed row, then the contents of the entire row must be read and saved in RAM prior to the erase. Then, new data and retained data can be written into the write latches to reprogram the row of Flash program memory. However, any unprogrammed locations can be written without first erasing the row. In this case, it is not necessary to save and rewrite the other previously programmed locations.

See Table 10-1 for erase row size and the number of write latches for Flash program memory.

11.1.3 OPEN-DRAIN CONTROL

The ODCONA register (Register 11-6) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONA bit is set, the corresponding port output becomes an open-drain driver, capable of sinking current only. When an ODCONA bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

11.1.4 SLEW RATE CONTROL

The SLRCONA register (Register 11-7) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONA bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONA bit is cleared, the corresponding port pin drive slews at the maximum rate possible.

11.1.5 INPUT THRESHOLD CONTROL

The INLVLA register (Register 11-8) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an Interrupt-On-Change occurs, if that feature is enabled. See Table 36-4 for more information on threshold levels.

Note:	Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

11.1.6 ANALOG CONTROL

The ANSELA register (Register 11-4) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRISx clear and ANSELx set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing Read-Modify-Write instructions on the affected port.

Note:	The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSELA bits must be initialized to '0' by user software.

EXAMPLE 11-1: INITIALIZING PORTA

```
; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL  PORTA        ;
CLRF     PORTA        ;Init PORTA
BANKSEL  LATA         ;Data Latch
CLRF     LATA         ;
BANKSEL  ANSELA       ;
CLRF     ANSELA       ;digital I/O
BANKSEL  TRISA        ;
MOVLW    B'00111000'  ;Set RA<5:3> as inputs
MOVWF    TRISA        ;and set RA<2:0> as
                      ;outputs
```

11.1.7 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions.

Each pin defaults to the PORT latch data after Reset. Other functions are selected with the Peripheral Pin Select (PPS) logic. See **Section 12.0 "Peripheral Pin Select (PPS) Module"** for more information.

Analog input functions, such as the ADC and comparator inputs, are not shown in the Peripheral Pin Select lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELA register. Digital output functions may continue to control the pin when it is in Analog mode.

REGISTER 13-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF<5:0>					
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	HS = Hardware Settable bit

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **IOCAF<5:0>:** Interrupt-On-Change PORTA Flag bits

1 = An enabled change was detected on the associated pin
Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.

0 = No change was detected or the user cleared the detected change

REGISTER 13-4: IOCBP: INTERRUPT-ON-CHANGE PORTB POSITIVE EDGE REGISTER(1)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
IOCBP<7:4>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as ‘0’
‘1’ = Bit is set	‘0’ = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **IOCBP<7:4>:** Interrupt-On-Change PORTB Positive Edge Enable bits

1 = Interrupt-On-Change is enabled on the pin for a positive going edge; IOCBFx bit and IOCIF flag will be set upon edge detection

0 = Interrupt-On-Change is disabled for the associated pin

bit 3-0 **Unimplemented:** Read as ‘0’

Note 1: PIC16(L)F1768/9 only.

15.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 16.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

15.4 ADC Acquisition Time

To ensure accurate temperature measurements, the user must wait at least 200 μs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μs between sequential conversions of the temperature indicator output.

TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVR<1:0>		ADFVR<1:0>		169

Legend: Shaded cells are unused by the temperature indicator module.

REGISTER 16-3: ADCON2: ADC CONTROL REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0
TRIGSEL<4:0>(1)					—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

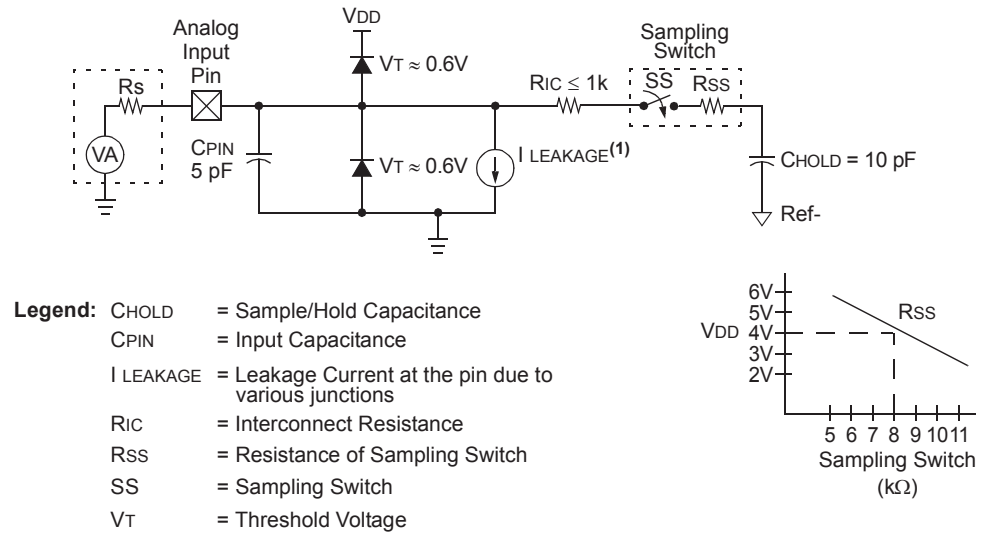
bit 7-3 **TRIGSEL<4:0>:** Auto-Conversion Trigger Selection bits(1)

11111 = Reserved
•
•
•
11011 = Reserved
11010 = PWM6 – OF6_match(2)
11001 = PWM6 – PH6_match(2)
11000 = PWM6 – PR6_match(2)
10111 = PWM6 – DC6_match(2)
10110 = PWM5 – OF5_match
10101 = PWM5 – PH5_match
10100 = PWM5 – PR5_match
10011 = PWM5 – DC5_match
10010 = PWM4 – PWM4OUT(2)
10001 = PWM3 – PWM3OUT
10000 = CCP2 – CCP2_trigger(2)
01111 = CCP1 – CCP1_trigger
01110 = CLC3 – LC3_out
01101 = CLC2 – LC2_out
01100 = CLC1 – LC1_out
01011 = Comparator C4 – sync_C4OUT(2)
01010 = Comparator C3 – sync_C3OUT(2)
01001 = Comparator C2 – sync_C2OUT
01000 = Comparator C1 – sync_C1OUT
00111 = Timer6 – T6_postscaled
00110 = Timer5 – T5_overflow
00101 = Timer4 – T4_postscaled
00100 = Timer3 – T3_overflow
00011 = Timer2 – T2_postscaled
00010 = Timer1 – T1_overflow
00001 = Timer0 – T0_overflow
00000 = No auto-conversion trigger selected

bit 3-0 **Unimplemented:** Read as '0'

Note 1: This is a rising edge-sensitive input for all sources.
2: PIC16(L)F1768/9 only; reserved otherwise.

FIGURE 16-4: ANALOG INPUT MODEL

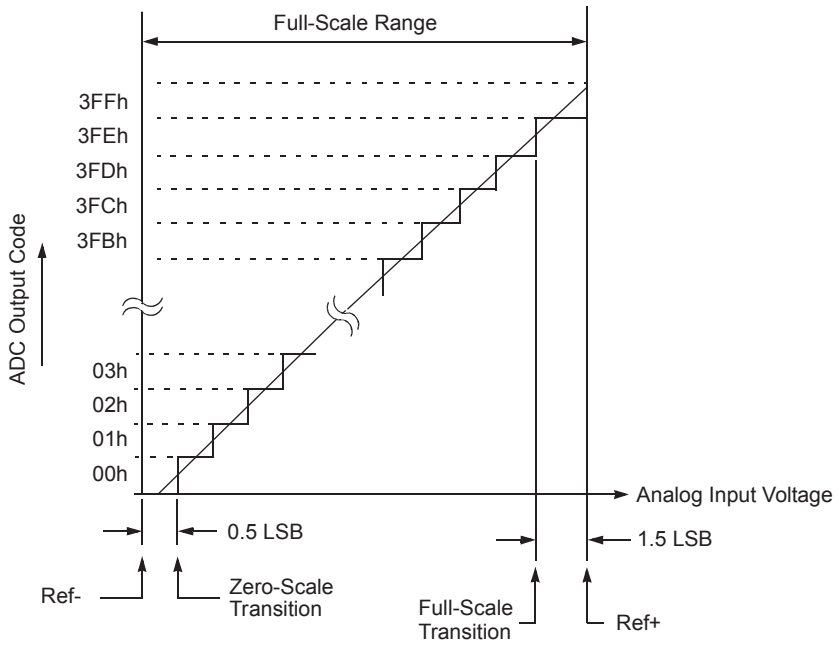


Legend:

CHOLD	=	Sample/Hold Capacitance
CPIN	=	Input Capacitance
I LEAKAGE	=	Leakage Current at the pin due to various junctions
RIC	=	Interconnect Resistance
RSS	=	Resistance of Sampling Switch
SS	=	Sampling Switch
VT	=	Threshold Voltage

Note 1: Refer to Table 36-4 (Parameter D060).

FIGURE 16-5: ADC TRANSFER FUNCTION



24.5 Register Definitions: CCP Control

REGISTER 24-1: CCPxCON: CCPx CONTROL REGISTER

R/W-0/0	U-0	R-x	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	—	OUT	FMT	MODE<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Reset

bit 7 **EN:** CCPx Module Enable bit
1 = CCPx is enabled
0 = CCPx is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** CCPx Output Data bit (read-only)

bit 4 **FMT:** CCPW (Pulse-Width) Alignment bit
If MODE<3:0> = PWM Mode:
1 = Left-aligned format, CCPRxH<7> is the MSB of the PWM duty cycle
0 = Right-aligned format, CCPRxL<0> is the LSB of the PWM duty cycle

bit 3-0 **MODE<3:0>:** CCPx Mode Selection bits
11xx = PWM mode

1011 = Compare mode: Pulse output, clear TMR1
1010 = Compare mode: Pulse output (0 - 1 - 0)
1001 = Compare mode: Clear output on compare match; output is set upon selection of this mode
1000 = Compare mode: Set output on compare match; output is set upon selection of this mode

0111 = Capture mode: Every 16th rising edge
0110 = Capture mode: Every 4th rising edge
0101 = Capture mode: Every rising edge
0100 = Capture mode: Every falling edge

0011 = Capture mode: Every rising or falling edge
0010 = Compare mode: Toggle output on match
0001 = Compare mode: Toggle output and clear TMR1 on match
0000 = Capture/Compare/PWM off (resets CCPx module) (reserved for backwards compatibility)

The maximum PWM resolution is ten bits when T2PR is 255. The resolution is a function of the T2PR register value as shown by Equation 25-4.

Note: If the pulse-width value is greater than the period the assigned PWM pin(s) will remain unchanged.

EQUATION 25-4: PWM RESOLUTION

$$Resolution = \frac{log[4(T2PR + 1)]}{log(2)} \ bits$$

TABLE 25-1: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 20 MHz)

PWM Frequency	0.31 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescale	64	4	1	1	1	1
T2PR Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 25-2: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS (FOSC = 8 MHz)

PWM Frequency	0.31 kHz	4.90 kHz	19.61 kHz	76.92 kHz	153.85 kHz	200.0 kHz
Timer Prescale	64	4	1	1	1	1
T2PR Value	0x65	0x65	0x65	0x19	0x0C	0x09
Maximum Resolution (bits)	8	8	8	6	5	5

25.7 Operation in Sleep Mode

In Sleep mode, the TMR2 register will not increment and the state of the module will not change. If the PWMx pin is driving a value, it will continue to drive that value. When the device wakes up, TMR2 will continue from its previous state.

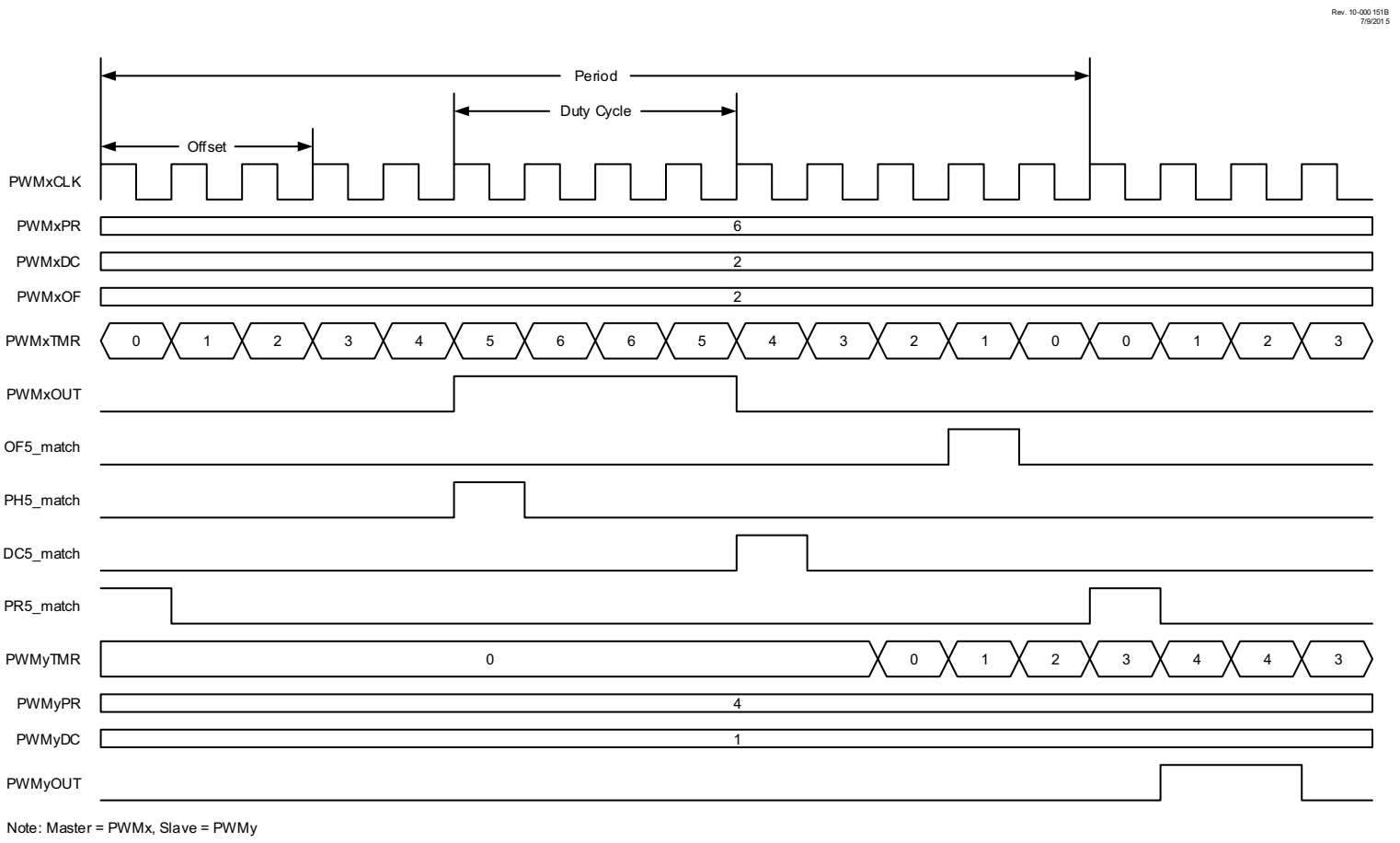
25.8 Changes in System Clock Frequency

The PWM frequency is derived from the system clock frequency (FOSC). Any changes in the system clock frequency will result in changes to the PWM frequency. Refer to **Section 5.0 "Oscillator Module (with Fail-Safe Clock Monitor)"** for additional details.

25.9 Effects of Reset

Any Reset will force all ports to Input mode and the PWM registers to their Reset states.

FIGURE 26-13: OFFSET MATCH ON DECREMENTING TIMER TIMING DIAGRAM



REGISTER 27-5: COGxRSIM0: COGx RISING EVENT SOURCE INPUT MODE REGISTER 0 (CONTINUED)

bit 1 **RSIM1:** COGx Rising Event Input Source 1 Mode bit

RIS1 = 1:

1 = Comparator 1 low-to-high transition will cause a rising event after rising event phase delay
0 = Comparator 1 high level will cause an immediate rising event

RIS1 = 0:

Comparator 1 has no effect on rising event.

bit 0 **RSIM0:** COGx Rising Event Input Source 0 Mode bit

RIS0 = 1:

1 = Pin selected with COGxINPPS register low-to-high transition will cause a rising event after rising event phase delay
0 = Pin selected with COGxINPPS register high level will cause an immediate rising event

RIS0 = 0:

Pin selected with COGxINPPS register has no effect on rising event.

REGISTER 27-9: COGxFSIM0: COGx FALLING EVENT SOURCE INPUT MODE REGISTER 0 (CONTINUED)

bit 1 **FSIM1:** COGx Falling Event Input Source 1 Mode bit

FIS1 = 1:
1 = Comparator 1 high-to-low transition will cause a falling event after falling event phase delay
0 = Comparator 1 low level will cause an immediate falling event

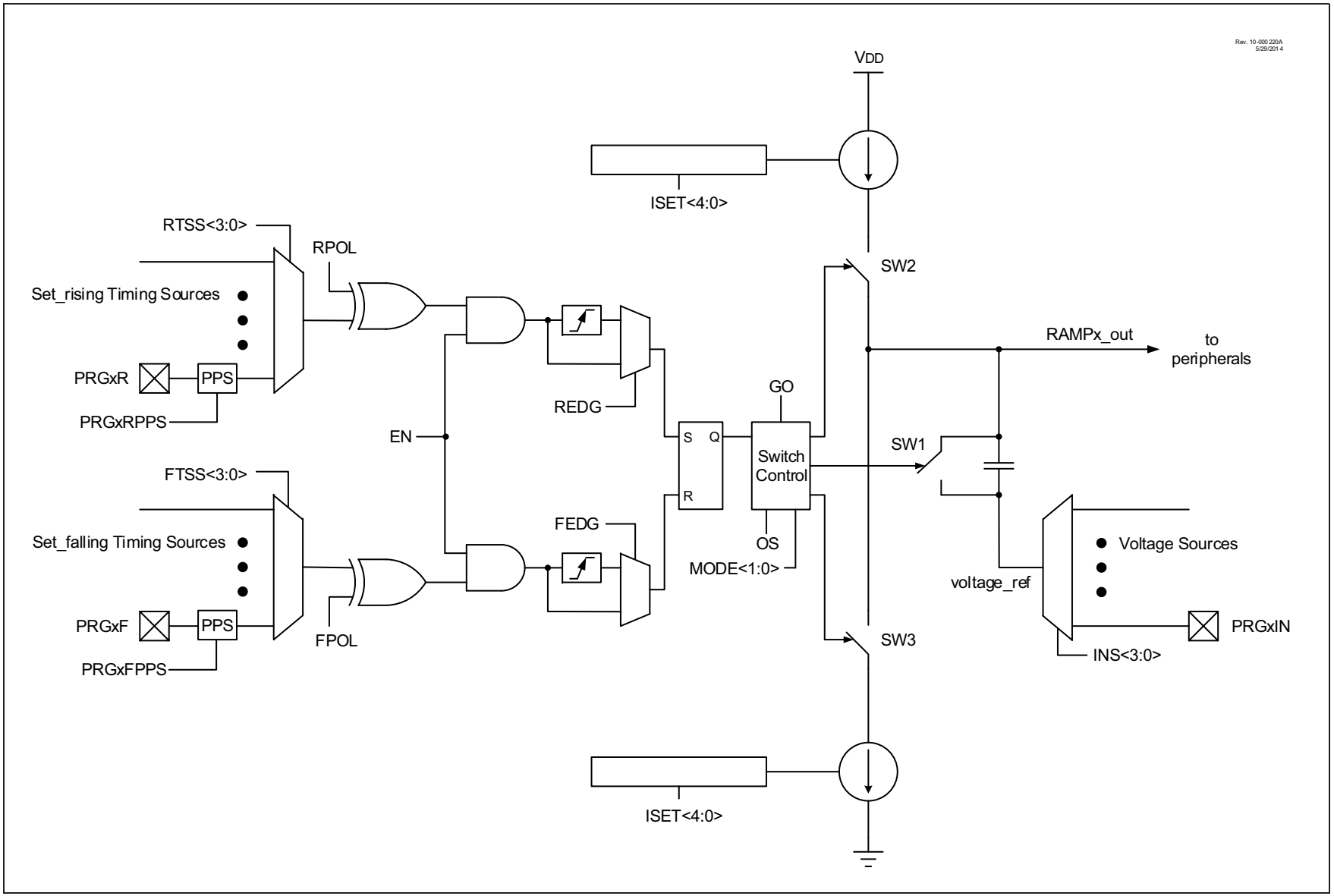
FIS1 = 0:
Comparator 1 has no effect on falling event.

bit 0 **FSIM0:** COGx Falling Event Input Source 0 Mode bit

FIS0 = 1:
1 = Pin selected with COGxINPPS control high-to-low transition will cause a falling event after falling event phase delay
0 = Pin selected with COGxINPPS control low level will cause an immediate falling event

FIS0 = 0:
Pin selected with COGxINPPS control has no effect on falling event.

FIGURE 30-1: SIMPLIFIED PRG MODULE BLOCK DIAGRAM



REGISTER 31-2: MDxCON1: MODULATION x CONTROL REGISTER 1

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
—	—	CHPOL	CHSYNC	—	—	CLPOL	CLSYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **CHPOL:** Modulation High Carrier Polarity Select bit
- 1 = Selected high carrier source is inverted
- 0 = Selected high carrier source is not inverted

bit 4 **CHSYNC:** Modulation High Carrier Synchronization Enable bit
- 1 = Modulator waits for a low edge on the high carrier before allowing a switch to the low carrier
- 0 = Modulator output is not synchronized to the high carrier(1)

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **CLPOL:** Modulation Low Carrier Polarity Select bit
- 1 = Selected low carrier source is inverted
- 0 = Selected low carrier source is not inverted

bit 0 **CLSYNC:** Modulation Low Carrier Synchronization Enable bit
- 1 = Modulator waits for a low edge on the low carrier before allowing a switch to the high carrier
- 0 = Modulator output is not synchronized to the low carrier(1)

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

TABLE 33-3: BAUD RATE FORMULAS

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	FOSC/[64 (n+1)]
0	0	1	8-bit/Asynchronous	FOSC/[16 (n+1)]
0	1	0	16-bit/Asynchronous	
0	1	1	16-bit/Asynchronous	FOSC/[4 (n+1)]
1	0	x	8-bit/Synchronous	
1	1	x	16-bit/Synchronous	

Legend: x = Don't care, n = value of SPxBRGH, SPxBRGL register pair.

TABLE 33-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUD1CON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	442
RC1STA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	441
SP1BRGL	BRG<7:0>								443
SP1BRGH	BRG<15:8>								443
TX1STA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	440

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for the Baud Rate Generator.

* Page provides register information.

TABLE 36-25: SPI MODE REQUIREMENTS

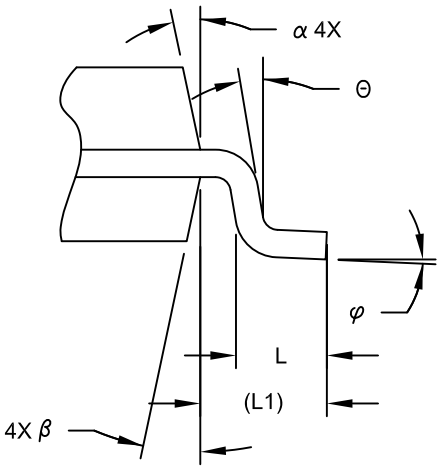
Standard Operating Conditions (unless otherwise stated)							
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
SP70*	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ Input	Tcy	—	—	ns	
SP71*	TscH	SCK Input High Time (Slave mode)	Tcy + 20	—	—	ns	
SP72*	TscL	SCK Input Low Time (Slave mode)	Tcy + 20	—	—	ns	
SP73*	TdiV2scH, TdiV2scL	Setup Time of SDI Data Input to SCK Edge	100	—	—	ns	
SP74*	TscH2diL, TscL2diL	Hold Time of SDI Data Input to SCK Edge	100	—	—	ns	
SP75*	TdoR	SDO Data Output Rise Time	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP76*	TdoF	SDO Data Output Fall Time	—	10	25	ns	
SP77*	TssH2doZ	$\overline{SS}$↑ to SDO Output High-Impedance	10	—	50	ns	
SP78*	TscR	SCK Output Rise Time (Master mode)	—	10	25	ns	3.0V ≤ VDD ≤ 5.5V
			—	25	50	ns	1.8V ≤ VDD ≤ 5.5V
SP79*	TscF	SCK Output Fall Time (Master mode)	—	10	25	ns	
SP80*	TscH2doV, TscL2doV	SDO Data Output Valid after SCK Edge	—	—	50	ns	3.0V ≤ VDD ≤ 5.5V
			—	—	145	ns	1.8V ≤ VDD ≤ 5.5V
SP81*	TdoV2scH, TdoV2scL	SDO Data Output Setup to SCK Edge	1 Tcy	—	—	ns	
SP82*	TssL2doV	SDO Data Output Valid after $\overline{SS}$↓ Edge	—	—	50	ns	
SP83*	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK Edge	1.5 Tcy + 40	—	—	ns	

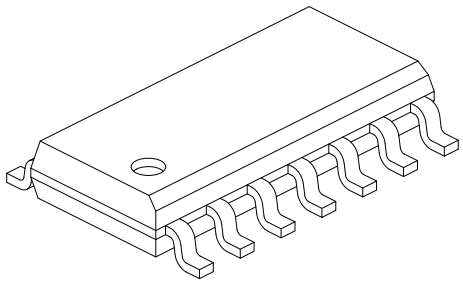
* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2