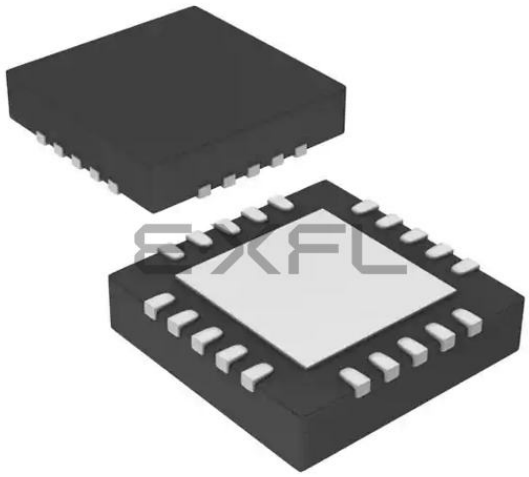

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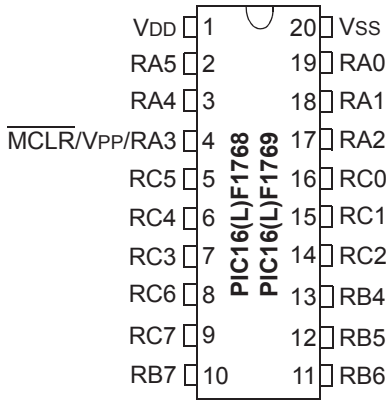
Applications of "Embedded - Microcontrollers"

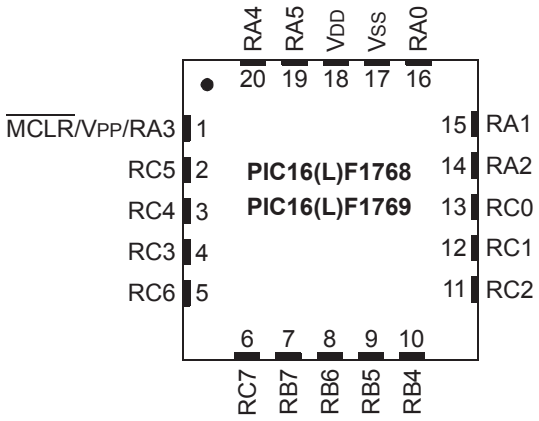
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1769-i-ml

FIGURE 3: 20-PIN PDIP, SOIC, SSOP



Note: See Table 4 for location of all peripheral functions.

FIGURE 4: 20-PIN QFN (4x4)



Note: See Table 4 for location of all peripheral functions.

TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 31											
F8Ch to FE3h	—	Unimplemented								—	—
FE4h	STATUS_SHAD	—	—	—	—	—	Z	DC	C	---- -xxx	---- -uuu
FE5h	WREG_SHAD	Working Register Shadow								xxxx xxxx	uuuu uuuu
FE6h	BSR_SHAD	—	—	—	Bank Select Register Shadow					---x xxxx	---u uuuu
FE7h	PCLATH_SHAD	—	Program Counter Latch High Register Shadow							-xxx xxxx	-uuu uuuu
FE8h	FSR0L_SHAD	Indirect Data Memory Address 0 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FE9h	FSR0H_SHAD	Indirect Data Memory Address 0 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FEAh	FSR1L_SHAD	Indirect Data Memory Address 1 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FEBh	FSR1H_SHAD	Indirect Data Memory Address 1 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FECh	—	Unimplemented								—	—
FEDh	STKPTR	—	—	—	Current Stack Pointer					---1 1111	---1 1111
FEEh	TOSL	Top of Stack Low byte								xxxx xxxx	uuuu uuuu
FEFh	TOSH	—	Top of Stack High Byte							-xxx xxxx	-uuu uuuu

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1768/9 only.

3: PIC16(L)F1764/5 only.

4: Unimplemented on PIC16LF1764/5/8/9.

7.6 Register Definitions: Interrupt Control

REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0
GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF(1)
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts

bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **TMR0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **INTE:** INT External Interrupt Enable bit
1 = Enables the INT external interrupt
0 = Disables the INT external interrupt

bit 3 **IOCIE:** Interrupt-On-Change Enable bit
1 = Enables the Interrupt-On-Change
0 = Disables the Interrupt-On-Change

bit 2 **TMR0IF:** Timer0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed
0 = TMR0 register did not overflow

bit 1 **INTF:** INT External Interrupt Flag bit
1 = The INT external interrupt occurred
0 = The INT external interrupt did not occur

bit 0 **IOCIF:** Interrupt-On-Change Interrupt Flag bit(1)
1 = When at least one of the Interrupt-On-Change pins changed state
0 = None of the Interrupt-On-Change pins have changed state

Note 1: The IOCIF Flag bit is read-only and cleared when all the Interrupt-On-Change flags in the IOCxF registers have been cleared by software.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

8.3 Register Definitions: Voltage Regulator Control

REGISTER 8-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1
—	—	—	—	—	—	VREGPM	r
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	r = Reserved bit
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **VREGPM:** Voltage Regulator Power Mode Selection bit
- 1 = Low-Power Sleep mode is enabled in Sleep(2)
  Draws lowest current in Sleep, slower wake-up.
- 0 = Normal Power mode is enabled in Sleep(2)
  Draws higher current in Sleep, faster wake-up.

bit 0 **Reserved:** Read as '1'. Maintain this bit set.

Note 1: PIC16F1764/5/8/9 only.
2: See **Section 36.0 "Electrical Specifications"**.

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
IOCAP	—	—	IOCAP<5:0>						162
IOCAN	—	—	IOCAN<5:0>						162
IOCAF	—	—	IOCAF<5:0>						163
IOCBP(1)	IOCBP<7:4>				—	—	—	—	163
IOCBN(1)	IOCBN<7:4>				—	—	—	—	164
IOCBF(1)	IOCBF<7:4>				—	—	—	—	164
IOCCP	IOCCP<7:6>(1)		IOCCP<5:0>						165
IOCCN	IOCCN<7:6>(1)		IOCCN<5:0>						165
IOCCF	IOCCF<7:6>(1)		IOCCF<5:0>						166
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	102
PIE2	OSFIE	C2IE	C1IE	—	BCL1IE	C4IE(1)	C3IE(1)	CCP2IE(1)	103
PIE3	PWM6IE(1)	PWM5IE	COG1IE	ZCDIE	COG2IE(1)	CLC3IE	CLC2IE	CLC1IE	104
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	105
PIR2	OSFIF	C2IF	C1IF	—	BCL1IF	C4IF(1)	C3IF(1)	CCP2IF(1)	106
PIR3	PWM6IF(1)	PWM5IF	COG1IF	ZCDIF	COG2IF(1)	CLC3IF	CLC2IF	CLC1IF	107
STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	27
VREGCON(2)	—	—	—	—	—	—	VREGPM	r	112
WDTCON	—	—	WDTPS<4:0>					SWDTEN	115

Legend: — = unimplemented location, read as '0'; r = Reserved bit. Shaded cells are not used in Power-Down mode.
Note 1: PIC16(L)F1768/9 only.
2: PIC16F1764/5/8/9 only.

REGISTER 13-9: IOCCF: INTERRUPT-ON-CHANGE PORTC FLAG REGISTER

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
IOCCF<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware Settable bit

bit 7-0 **IOCCF<7:0>:** Interrupt-On-Change PORTC Flag bits(1)

1 = An enabled change was detected on the associated pin
Set when IOCCPx = 1 and a rising edge was detected on RCx, or when IOCCNx = 1 and a falling edge was detected on RCx

0 = No change was detected or the user cleared the detected change

Note 1: Bits<7:6> are available on PIC16(L)F1768/9 only.

TABLE 13-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELB(1)	ANSB<7:4>				—	—	—	—	143
ANSELC	ANSC<7:6>(1)		—	—	ANSC<3:0>				148
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
IOCAF	—	—	IOCAF<5:0>						163
IOCAN	—	—	IOCAN<5:0>						162
IOCAP	—	—	IOCAP<5:0>						162
IOCBF(1)	IOCBF<7:4>				—	—	—	—	164
IOCBN(1)	IOCBN<7:4>				—	—	—	—	164
IOCBP(1)	IOCBP<7:4>				—	—	—	—	163
IOCCF	IOCCF<7:6>(1)		IOCCF<5:0>						166
IOCCN	IOCCN<7:6>(1)		IOCCN<5:0>						165
IOCCP	IOCCP<7:6>(1)		IOCCP<5:0>						165
TRISA	—	—	TRISA<5:4>		—(2)	TRISA<2:0>			136
TRISB(1)	TRISB<7:4>				—	—	—	—	142
TRISC	TRISC<7:6>(1)		TRISC<5:0>						147

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Interrupt-On-Change.

Note 1: PIC16(L)F1768/9 only.

2: Unimplemented, read as '1'.

15.3 Temperature Output

The output of the circuit is measured using the internal Analog-to-Digital Converter. A channel is reserved for the temperature circuit output. Refer to **Section 16.0 "Analog-to-Digital Converter (ADC) Module"** for detailed information.

15.4 ADC Acquisition Time

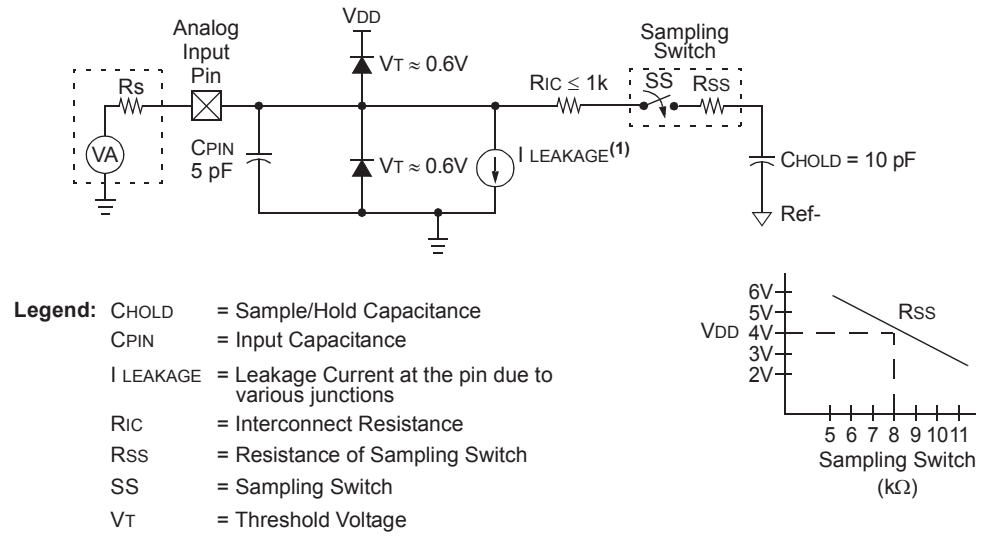
To ensure accurate temperature measurements, the user must wait at least 200 μs after the ADC input multiplexer is connected to the temperature indicator output before the conversion is performed. In addition, the user must wait 200 μs between sequential conversions of the temperature indicator output.

TABLE 15-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE TEMPERATURE INDICATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDFVR<1:0>		ADFVR<1:0>		169

Legend: Shaded cells are unused by the temperature indicator module.

FIGURE 16-4: ANALOG INPUT MODEL

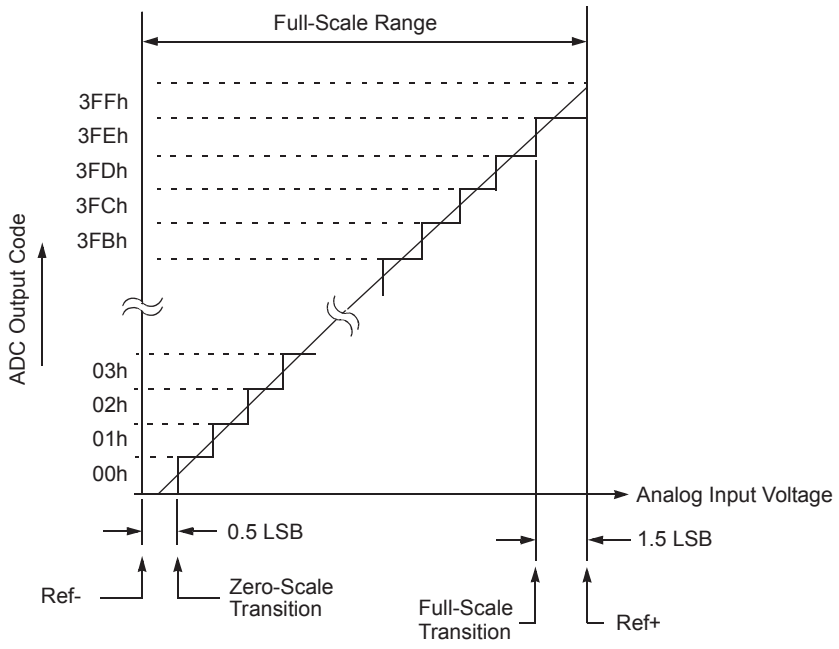


Legend:

CHOLD	=	Sample/Hold Capacitance
CPIN	=	Input Capacitance
I LEAKAGE	=	Leakage Current at the pin due to various junctions
RIC	=	Interconnect Resistance
RSS	=	Resistance of Sampling Switch
SS	=	Sampling Switch
VT	=	Threshold Voltage

Note 1: Refer to Table 36-4 (Parameter D060).

FIGURE 16-5: ADC TRANSFER FUNCTION



20.9 Register Definitions: ZCD Control

Long bit name prefixes for the Zero-Cross Detect peripheral are shown in Table 20-1. Refer to **Section 1.1.2.2 "Long Bit Names"** for more information

TABLE 20-1: BIT NAME PREFIXES

Peripheral	Bit Name Prefix
ZCD1	ZCD1

REGISTER 20-1: ZCDxCON: ZERO-CROSS DETECTION x CONTROL REGISTER

R/W-0/0	U-0	R-x/x	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
EN(1)	—	OUT	POL	—	—	INTP	INTN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = value depends on configuration bits

bit 7 **EN:** Zero-Cross Detection Enable bit(1)
1 = Zero-Cross Detect is enabled; ZCD pin is forced to output to source and sink current
0 = Zero-Cross Detect is disabled; ZCD pin operates according to PPS and TRISx controls

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Zero-Cross Detection Logic Level bit
POL bit = 0:
1 = ZCD pin is sinking current
0 = ZCD pin is sourcing current
POL bit = 1:
1 = ZCD pin is sourcing current
0 = ZCD pin is sinking current

bit 4 **POL:** Zero-Cross Detection Logic Output Polarity bit
1 = ZCD logic output is inverted
0 = ZCD logic output is not inverted

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **INTP:** Zero-Cross Positive Edge Interrupt Enable bit
1 = ZCDIF bit is set on low-to-high OUT transition
0 = ZCDIF bit is unaffected by low-to-high OUT transition

bit 0 **INTN:** Zero-Cross Negative Edge Interrupt Enable bit
1 = ZCDIF bit is set on high-to-low OUT transition
0 = ZCDIF bit is unaffected by high-to-low OUT transition

Note 1: The EN bit has no effect when the $\overline{\text{ZCD}}$ Configuration bit is cleared.

21.2 Register Definitions: Option Register

REGISTER 21-1: OPTION_REG: OPTION REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **$\overline{\text{WPUEN}}$:** Weak Pull-Up Enable bit
1 = All weak pull-ups are disabled (except $\overline{\text{MCLR}}$, if it is enabled)
0 = Weak pull-ups are enabled by individual WPUx latch values

bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **TMR0CS:** Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (FOSC/4)

bit 4 **TMR0SE:** Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is not assigned to the Timer0 module
0 = Prescaler is assigned to the Timer0 module

bit 2-0 **PS<2:0>:** Prescaler Rate Select bits

Bit Value	Timer0 Rate
000	1 : 2
001	1 : 4
010	1 : 8
011	1 : 16
100	1 : 32
101	1 : 64
110	1 : 128
111	1 : 256

TABLE 21-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			214
TMR0	Timer0 Module Register								212*
TRISA	—	—	TRISA<5:4>		—(1)	TRISA2	TRISA<1:0>		136

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the Timer0 module.
* Page provides register information.
Note 1: Unimplemented, read as '1'.

22.3 Timer1 Prescaler

Timer1 has four prescaler options, allowing 1, 2, 4 or 8 divisions of the clock input. The CKPS<1:0> bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

22.4 Timer1 (Secondary) Oscillator

A dedicated low-power 32.768 kHz oscillator circuit is built in between pins, SOSCI (input) and SOSCO (amplifier output). This internal circuit is to be used in conjunction with an external 32.768 kHz crystal.

The oscillator circuit is enabled by setting the OSCEN bit of the T1CON register. The oscillator will continue to run during Sleep.

Note:	The oscillator requires a start-up and stabilization time before use. Thus, OSCEN should be set and a suitable delay observed prior to using Timer1. A suitable delay similar to the OST delay can be implemented in software by clearing the TMR1IF bit then presetting the TMR1H:TMR1L register pair to FC00h. The TMR1IF flag will be set when 1024 clock cycles have elapsed, thereby indicating that the oscillator is running and reasonably stable.

22.5 Timer1 Operation in Asynchronous Counter Mode

If the control bit, $\overline{\text{SYNC}}$ of the T1CON register, is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt-on-overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 22.5.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

22.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

22.6 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 Gate Enable.

Timer1 gate can also be driven by multiple selectable sources.

22.6.1 TIMER1 GATE ENABLE

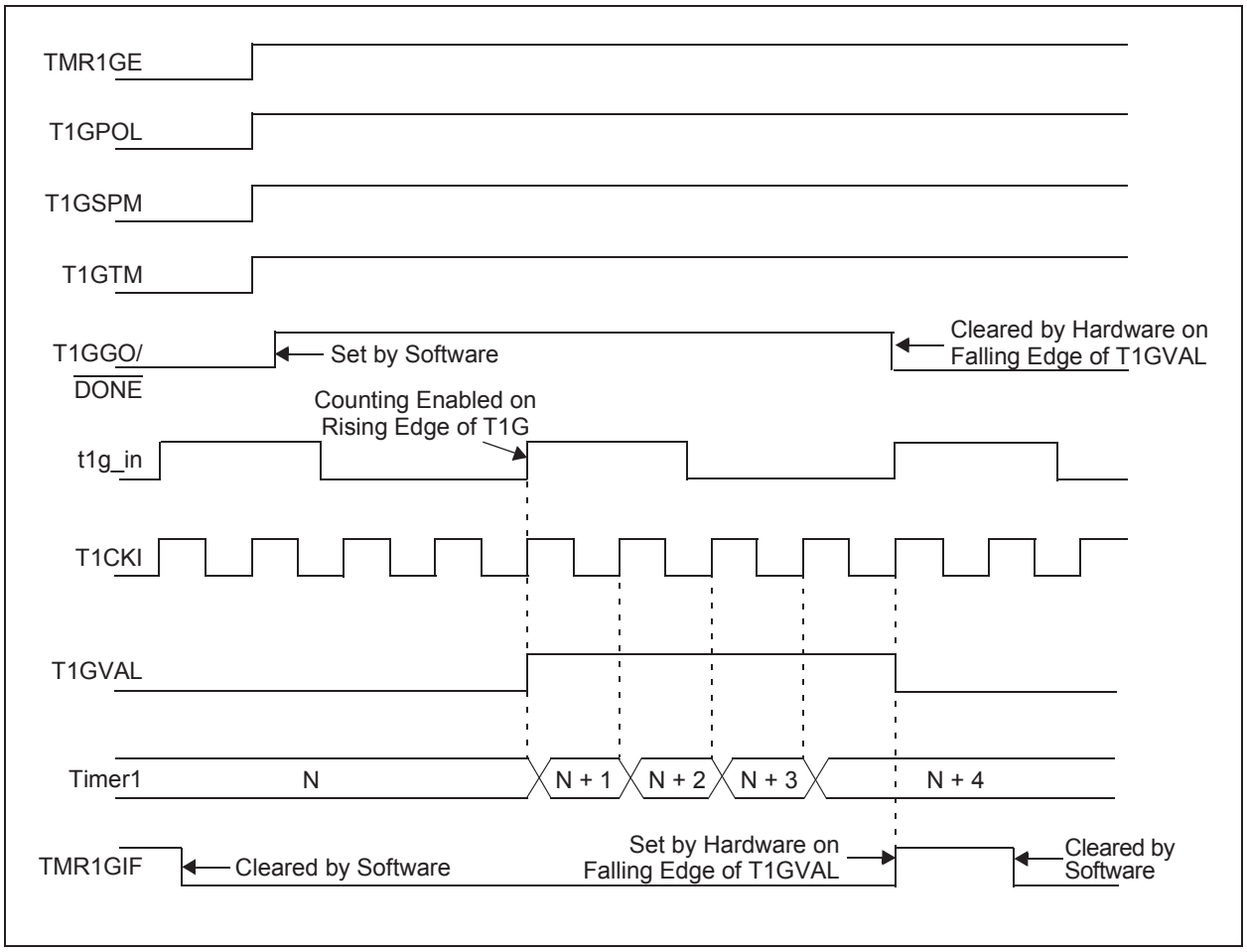
The Timer1 Gate Enable mode is enabled by setting the GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 22-3 for timing details.

TABLE 22-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

FIGURE 22-6: TIMER1 GATE SINGLE-PULSE AND TOGGLE COMBINED MODE



23.6.7 EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE

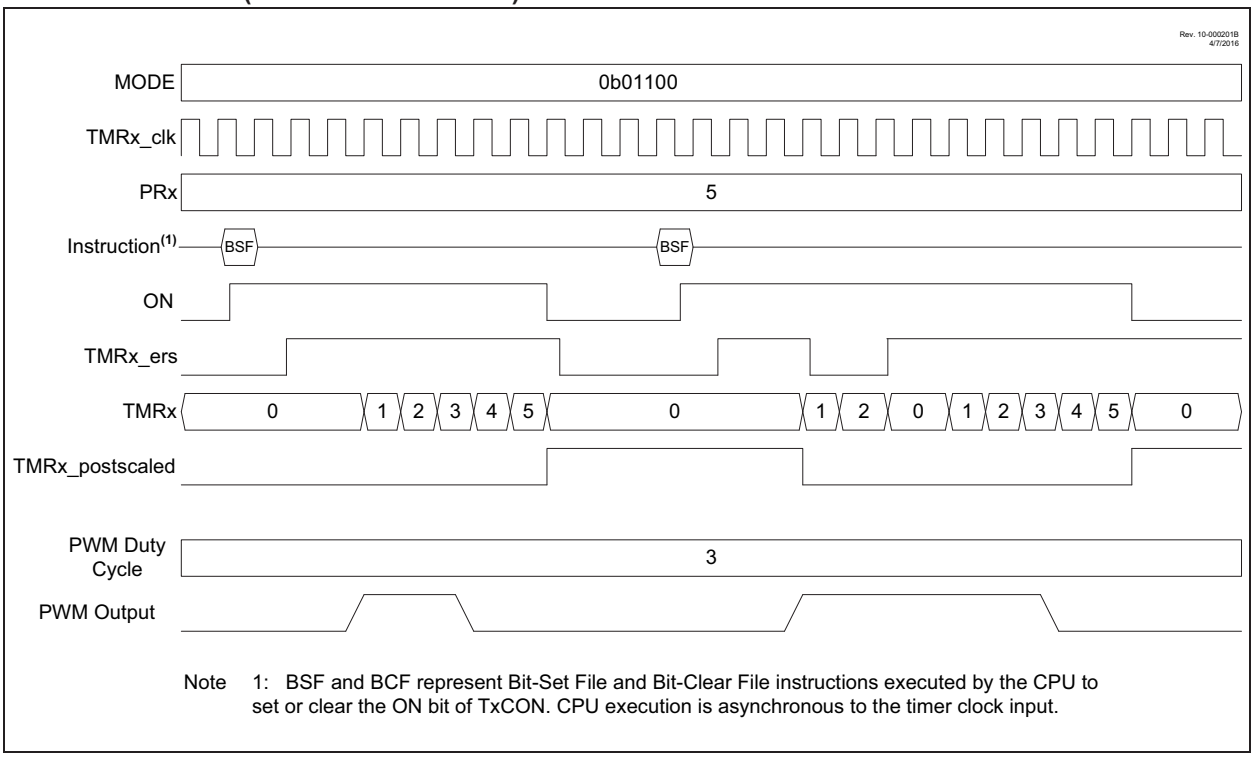
In Edge-Triggered Hardware Limit One-Shot modes, the timer starts on the first external signal edge after the ON bit is set and resets on all subsequent edges. Only the first edge after the ON bit is set is needed to start the timer. The counter will resume counting automatically, two clocks after all subsequent external Reset edges. Edge triggers are as follows:

- Rising edge start and Reset (MODE<4:0> = 01100)
- Falling edge start and Reset (MODE<4:0> = 01101)

The timer resets and clears the ON bit when the timer value matches the PRx period value. External signal edges will have no effect until after software sets the ON bit. Figure 23-10 illustrates the rising edge hardware limit one-shot operation.

When this mode is used in conjunction with the CCP then the first starting edge trigger, and all subsequent Reset edges, will activate the PWM drive. The PWM drive will deactivate when the timer matches the CCPRx pulse-width value and stay deactivated until the timer halts at the PRx period match unless an external signal edge resets the timer before the match occurs.

FIGURE 23-10: EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE<4:0> = 01100)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

REGISTER 27-8: COGxFIS1: COGx FALLING EVENT INPUT SELECTION REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FIS15(1)	FIS14	FIS13	FIS12	FIS11	FIS10	FIS9	FIS8
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **FIS15:** COGx Falling Event Input Source 15 Mode bit(1)
- 1 = DSM2 MD2_out is enabled as a falling event input
- 0 = DSM2 MD2_out has no effect on the falling event

bit 6 **FIS14:** COGx Falling Event Input Source 14 Mode bit
- 1 = DSM1 MD1_out is enabled as a falling event input
- 0 = DSM1 MD1_out has no effect on the falling event

bit 5 **FIS13:** COGx Falling Event Input Source 13 Enable bit
- 1 = CLC3 output is enabled as a falling event input
- 0 = CLC3 output has no effect on the falling event

bit 4 **FIS12:** COGx Falling Event Input Source 12 Enable bit
- 1 = CLC2 output is enabled as a falling event input
- 0 = CLC2 output has no effect on the falling event

bit 3 **FIS11:** COGx Falling Event Input Source 11 Enable bit
- 1 = CLC1 output is enabled as a falling event input
- 0 = CLC1 output has no effect on the falling event

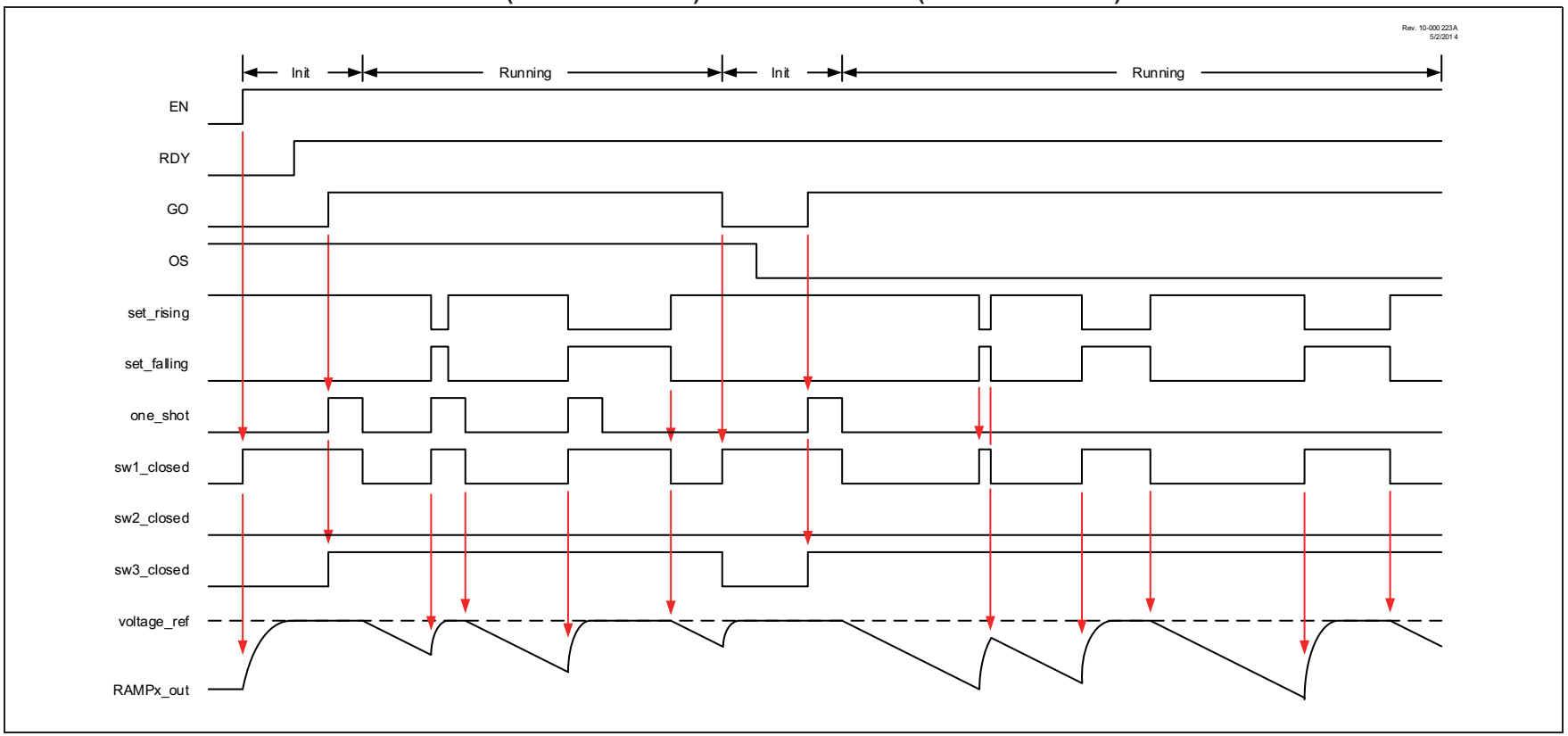
bit 2 **FIS10:** COGx Falling Event Input Source 10 Enable bit
- 1 = PWM6 output is enabled as a falling event input
- 0 = PWM6 output has no effect on the falling event

bit 1 **FIS9:** COGx Falling Event Input Source 9 Enable bit
- 1 = PWM5 output is enabled as a falling event input
- 0 = PWM5 output has no effect on the falling event

bit 0 **FIS8:** COGx Falling Event Input Source 8 Enable bit
- 1 = PWM4 output is enabled as falling event input
- 0 = PWM4 output has no effect on the falling event

Note 1: PIC16(L)F1768/9 only. Otherwise unimplemented, read as '0'.

FIGURE 30-2: SLOPE COMPENSATION (FALLING RAMP) TIMING DIAGRAM (MODE<1:0> = 00)



REGISTER 31-4: MDxCARH: MODULATION x CARRIER HIGH CONTROL REGISTER

U-0	U-0	U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	—	CH<3:0>(1)			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **CH<3:0>** Modulator Data High Carrier Selection bits(1)
See Table 31-4.

Note 1: Narrowed carrier pulse widths or spurs may occur in the signal stream if the carrier is not synchronized.

TABLE 31-4: HIGH CARRIER SOURCES

CH<3:0>	High Carrier Source PIC16(L)F1764/5	High Carrier Source PIC16(L)F1768/9
1111	LC3_out	LC3_out
1110	LC2_out	LC2_out
1101	LC1_out	LC1_out
1100	Fixed Low	PWM6_out
1011	PWM5_out	PWM5_out
1010	Fixed Low	PWM4_out
1001	PWM3_out	PWM3_out
1000	Fixed Low	CCP2_out
0111	CCP1_out	CCP1_out
0110	Fixed Low	Fixed Low
0101	Fixed Low	Fixed Low
0100	Fixed Low	Fixed Low
0011	Fixed Low	Fixed Low
0010	HFINTOSC	HFINTOSC
0001	FOSC	FOSC
0000	MDxCHPPS Pin Selection	MDxCHPPS Pin Selection

33.3 Register Definitions: EUSART Control

REGISTER 33-1: TX1STA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **CSRC:** Clock Source Select bit

Asynchronous mode:
Don't care.

Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-Bit Transmit Enable bit

1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)

1 = Transmit is enabled
0 = Transmit is disabled

bit 4 **SYNC:** EUSART Mode Select bit

1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit

Asynchronous mode:
1 = Sends Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission has completed

Synchronous mode:
Don't care.

bit 2 **BRGH:** High Baud Rate Select bit

Asynchronous mode:
1 = High speed
0 = Low speed

Synchronous mode:
Unused in this mode.

bit 1 **TRMT:** Transmit Shift Register Status bit

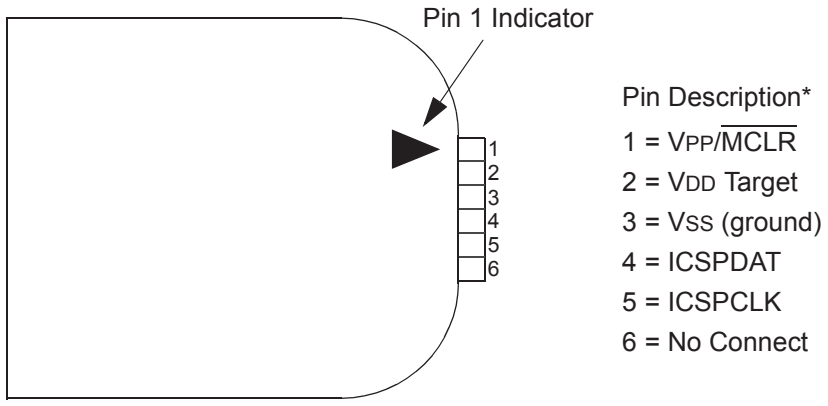
1 = TSR is empty
0 = TSR is full

bit 0 **TX9D:** Ninth bit of Transmit Data

Can be address/data bit or a parity bit.

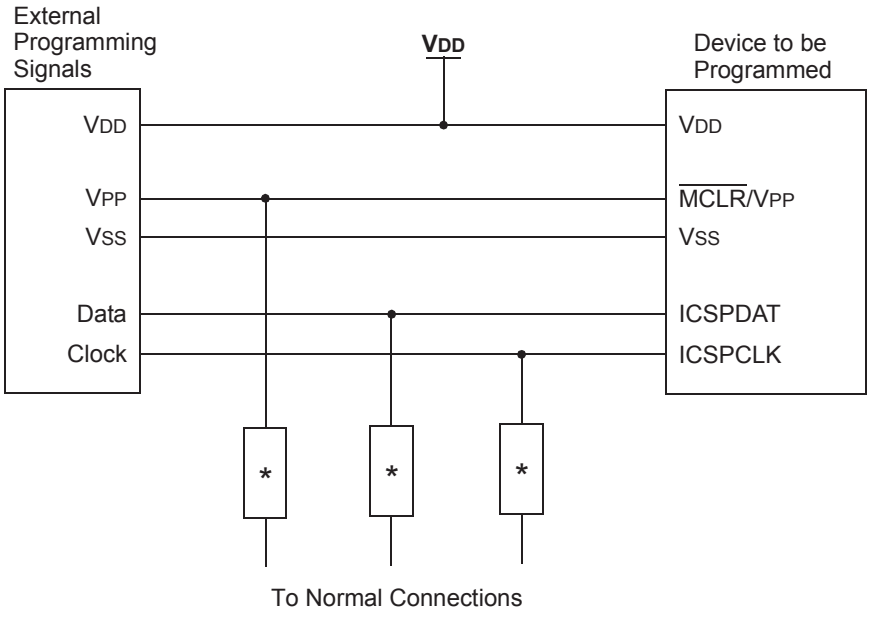
Note 1: SREN/CREN overrides TXEN in Sync mode.

FIGURE 34-2: PICkit™ PROGRAMMER STYLE CONNECTOR INTERFACE



* The 6-pin header (0.100" spacing) accepts 0.025" square pins.

FIGURE 34-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING



* Isolation devices (as required).

TABLE 36-8: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)								
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Typ†	Max.	Units	Conditions
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(1)	±2%	—	16.0	—	MHz	VDD = 3.0V, TA = 25°C **(Note 2)**
OS08A	MFOSC	Internal Calibrated MFINTOSC Frequency(1)	±2%	—	500	—	kHz	VDD = 3.0V, TA = 25°C **(Note 3)**
OS09	LFOSC	Internal LFINTOSC Frequency	—	—	31	—	kHz	-40°C ≤ TA ≤ +125°C
OS10*	TWARM	HFINTOSC Wake-up from Sleep Start-up Time	—	—	3.2	8	µs	
		MFINTOSC Wake-up from Sleep Start-up Time	—	—	24	35	µs	
		LFINTOSC Wake-up from Sleep Start-up Time	—	—	0.5	—	ms	

* These parameters are characterized but not tested.

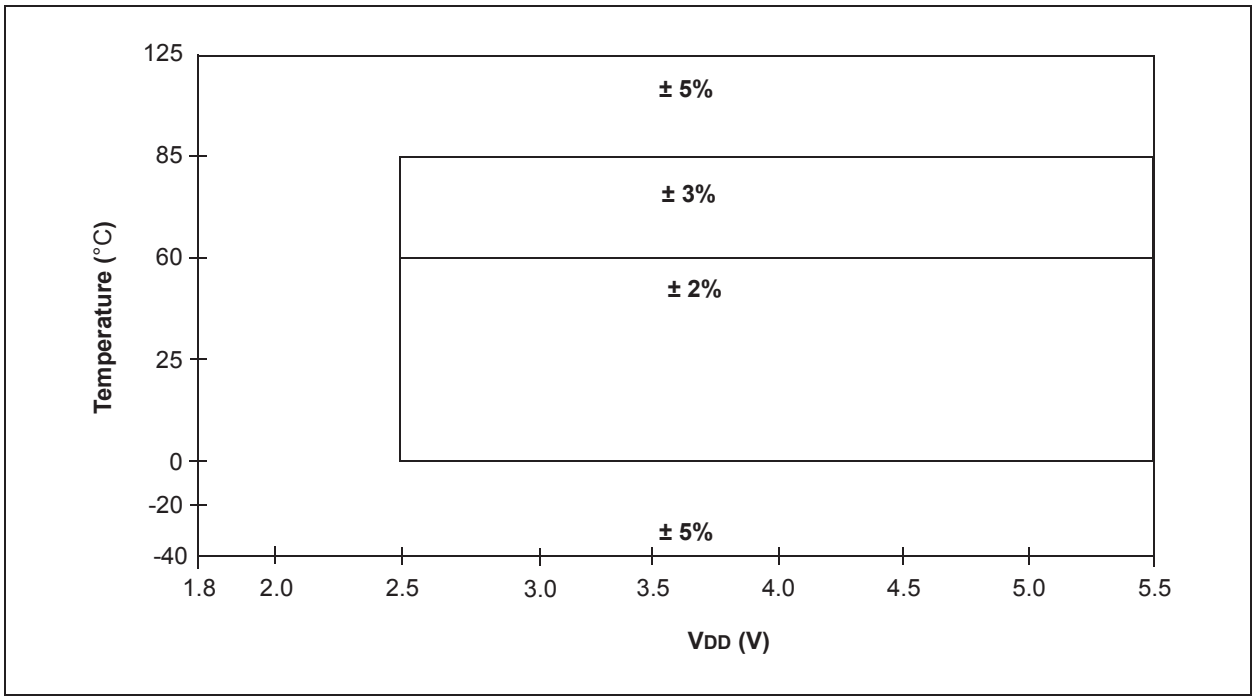
† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

2: See Figure 37-74: Wake From Sleep, VREGPM = 0. and Figure 37-75: Wake From Sleep, VREGPM = 1.

3: See Figure 37-57: LFINTOSC Frequency, PIC16LF1764/5/8/9 Only. and Figure 37-58: LFINTOSC Frequency, PIC16F1764/5/8/9 Only.

FIGURE 36-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

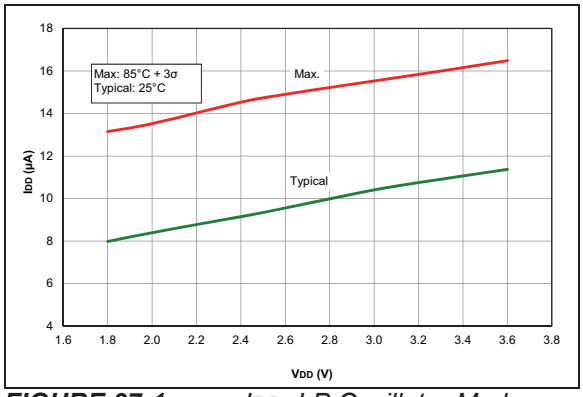


FIGURE 37-1: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16LF1764/5/8/9 Only.*

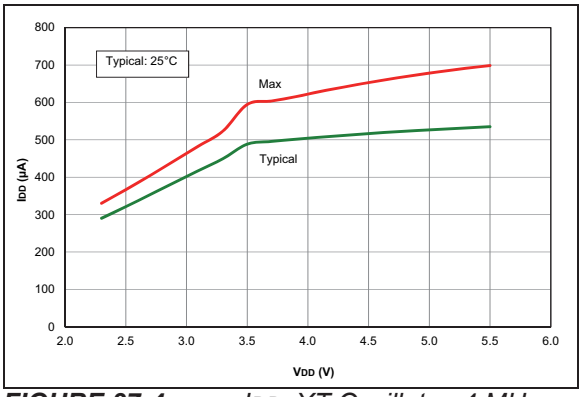


FIGURE 37-4: *IDD, XT Oscillator, 4 MHz, PIC16F1764/5/8/9 Only.*

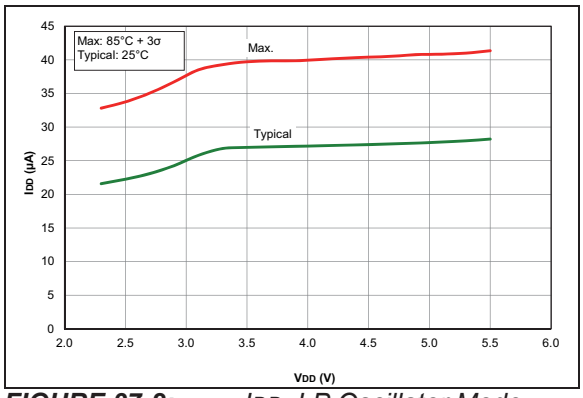


FIGURE 37-2: *IDD, LP Oscillator Mode, Fosc = 32 kHz, PIC16F1764/5/8/9 Only.*

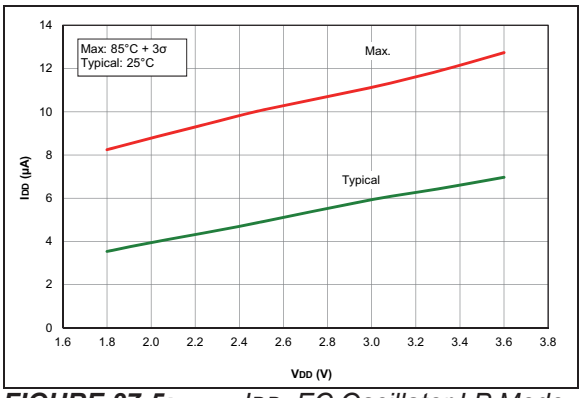


FIGURE 37-5: *IDD, EC Oscillator LP Mode, Fosc = 32 kHz, PIC16LF1764/5/8/9 Only.*

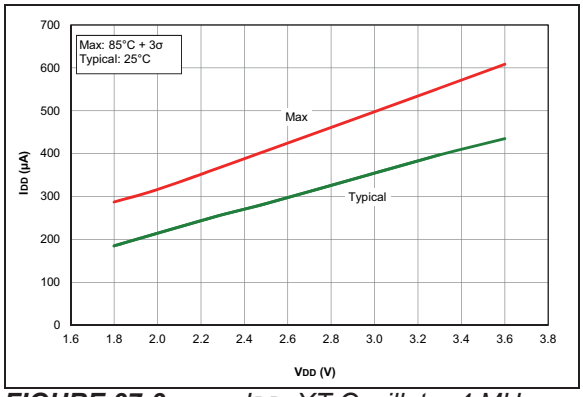


FIGURE 37-3: *IDD, XT Oscillator 4 MHz, PIC16LF1764/5/8/9 Only.*

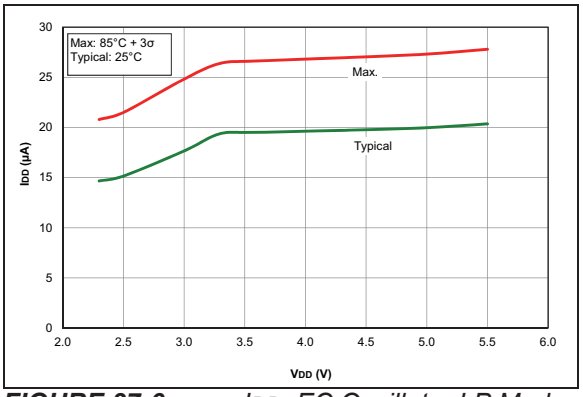


FIGURE 37-6: *IDD, EC Oscillator LP Mode, Fosc = 32 kHz, PIC16F1764/5/8/9 Only.*

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

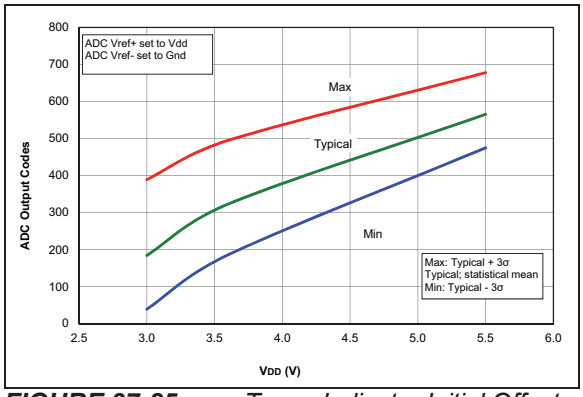


FIGURE 37-85: *Temp. Indicator Initial Offset, High Range, Temp. = 20°C, PIC16F1764/5/8/9 Only..*

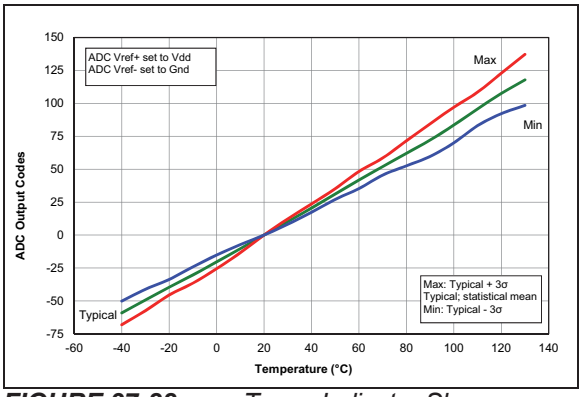


FIGURE 37-88: *Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 5.5V, PIC16F1764/5/8/9 Only.*

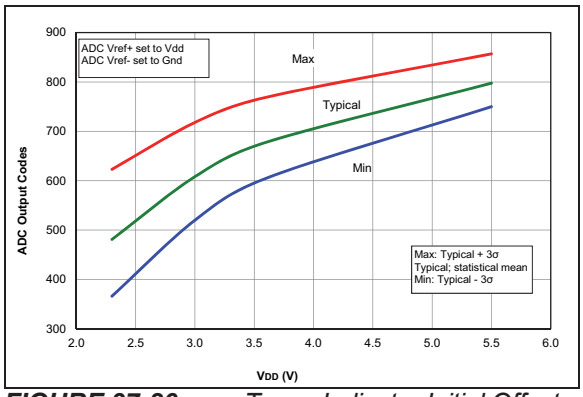


FIGURE 37-86: *Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16F1764/5/8/9 Only.*

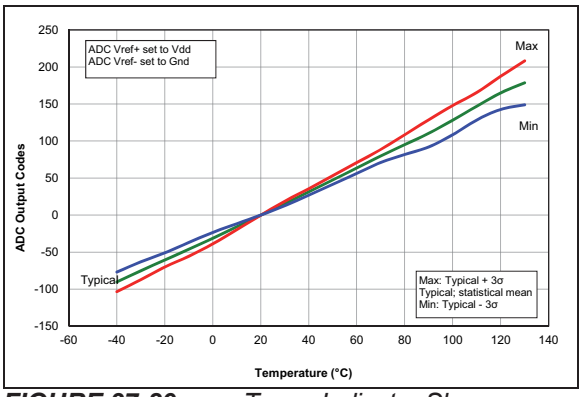


FIGURE 37-89: *Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 3.6V, PIC16F1764/5/8/9 Only.*

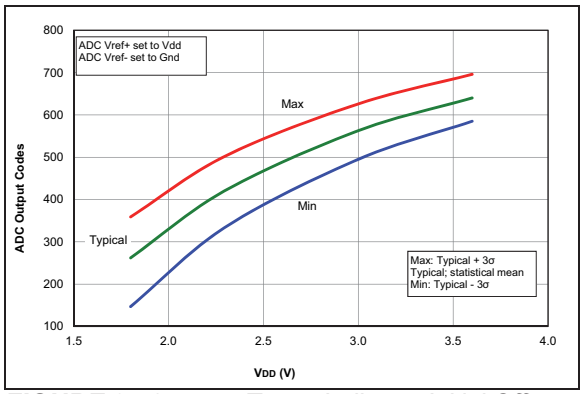


FIGURE 37-87: *Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16LF1764/5/8/9 Only.*

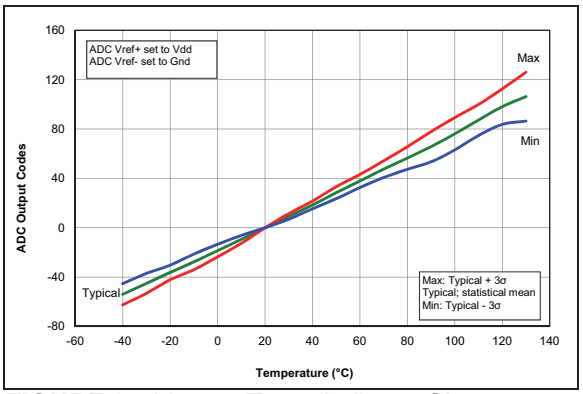


FIGURE 37-90: *Temp. Indicator Slope Normalized to 20°C, Low Range, VDD = 3.0V, PIC16F1764/5/8/9 Only.*