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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1769-i-so

TABLE 3-12: PIC16(L)F1764/5 MEMORY MAP (BANKS 27-30)

	Bank 27		Bank 28		Bank 29		Bank 30
D8Ch	—	E0Ch	—	E8Ch	—	F0Ch	—
D8Dh	—	E0Dh	—	E8Dh	—	F0Dh	—
D8Eh	PWMEN	E0Eh	—	E8Eh	—	F0Eh	—
D8Fh	PWMLD	E0Fh	PPSLOCK	E8Fh	—	F0Fh	CLCDATA
D90h	PWMOUT	E10h	INTPPS	E90h	RA0PPS	F10h	CLC1CON
D91h	PWM5PHL	E11h	T0CKIPPS	E91h	RA1PPS	F11h	CLC1POL
D92h	PWM5PHH	E12h	T1CKIPPS	E92h	RA2PPS	F12h	CLC1SEL0
D93h	PWM5DCL	E13h	T1GPPS	E93h	—	F13h	CLC1SEL1
D94h	PWM5DCH	E14h	CCP1PPS	E94h	RA4PPS	F14h	CLC1SEL2
D95h	PWM5PRL	E15h	—	E95h	RA5PPS	F15h	CLC1SEL3
D96h	PWM5PRH	E16h	COG1INPPS	E96h	—	F16h	CLC1GLS0
D97h	PWM5OFL	E17h	—	E97h	—	F17h	CLC1GLS1
D98h	PWM5OFH	E18h	—	E98h	—	F18h	CLC1GLS2
D99h	PWM5TMRL	E19h	T2INPPS	E99h	—	F19h	CLC1GLS3
D9Ah	PWM5TMRH	E1Ah	T3CKIPPS	E9Ah	—	F1Ah	CLC2CON
D9Bh	PWM5CON	E1Bh	T3GPPS	E9Bh	—	F1Bh	CLC2POL
D9Ch	PWM5INTE	E1Ch	T4INPPS	E9Ch	—	F1Ch	CLC2SEL0
D9Dh	PWM5INTF	E1Dh	T5CKIPPS	E9Dh	—	F1Dh	CLC2SEL1
D9Eh	PWM5CLKCON	E1Eh	T5GPPS	E9Eh	—	F1Eh	CLC2SEL2
D9Fh	PWM5LDCON	E1Fh	T6INPPS	E9Fh	—	F1Fh	CLC2SEL3
DA0h	PWM5OFCON	E20h	SSPCLKPPS	EA0h	RC0PPS	F20h	CLC2GLS0
DA1h	—	E21h	SSPDATPPS	EA1h	RC1PPS	F21h	CLC2GLS1
DA2h	—	E22h	SSPSSPPS	EA2h	RC2PPS	F22h	CLC2GLS2
DA3h	—	E23h	—	EA3h	RC3PPS	F23h	CLC2GLS3
DA4h	—	E24h	RXPPS	EA4h	RC4PPS	F24h	CLC3CON
DA5h	—	E25h	CKPPS	EA5h	RC5PPS	F25h	CLC3POL
DA6h	—	E26h	—	EA6h	—	F26h	CLC3SEL0
DA7h	—	E27h	—	EA7h	—	F27h	CLC3SEL1
DA8h	—	E28h	CLCIN0PPS	EA8h	—	F28h	CLC3SEL2
DA9h	—	E29h	CLCIN1PPS	EA9h	—	F29h	CLC3SEL3
DAAh	—	E2Ah	CLCIN2PPS	EAAh	—	F2Ah	CLC3GLS0
DABh	—	E2Bh	CLCIN3PPS	EABh	—	F2Bh	CLC3GLS1
DACh	—	E2Ch	PRG1FPPS	EACh	—	F2Ch	CLC3GLS2
DADh	—	E2Dh	PRG1RPPS	EADh	—	F2Dh	CLC3GLS3
DAEh	—	E2Eh	—	EAEh	—	F2Eh	—
DAFh	—	E2Fh	—	EAFh	—	F2Fh	—
DB0h	—	E30h	MD1CHPPS	EB0h	—	F30h	—
DB1h	—	E31h	MD1CLPPS	EB1h	—	F31h	—
DB2h	—	E32h	MD1MODPPS	EB2h	—	F32h	—
DB3h	—	E33h	—	EB3h	—	F33h	—
DB4h	—	E34h	—	EB4h	—	F34h	—
DB5h	—	E35h	—	EB5h	—	F35h	—
DB6h	—	E36h	—	EB6h	—	F36h	—
DB7h	—	E37h	—	EB7h	—	F37h	—
DB8h	—	E38h	—	EB8h	—	F38h	—
DB9h	—	E39h	—	EB9h	—	F39h	—
DBAh	—	E3Ah	—	EBAh	—	F3Ah	—
DBBh	—	E3Bh	—	EBBh	—	F3Bh	—
DBCh	—	E3Ch	—	EBCh	—	F3Ch	—
DBDh	—	E3Dh	—	EBDh	—	F3Dh	—
DBEh	—	E3Eh	—	EBEh	—	F3Eh	—
DBFh	—	E3Fh	—	EBFh	—	F3Fh	—
DC0h — DEFh		E40h — E6Fh		EC0h — EEFh		F40h — F6Fh	

Legend: ☐ = Unimplemented data memory locations, read as '0',

TABLE 3-16: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on All Other Resets
Bank 8											
40Ch — 40Dh	—	Unimplemented								—	—
40Eh	HIDRVC	—	—	HIDC<5:4>		—	—	—	—	--00 ----	--00 ----
40Fh — 412h	—	Unimplemented								—	—
413h	T4TMR	Holding Register for the 8-Bit TMR4 Register								0000 0000	0000 0000
413h	T4PR	TMR4 Period Register								1111 1111	1111 1111
415h	T4CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
416h	T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
417h	T4CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
418h	T4RST	—	—	—	—	RSEL<3:0>				---- 0000	---- 0000
419h	—	Unimplemented								—	—
41Ah	T6TMR	Holding Register for the 8-Bit TMR4 Register								0000 0000	0000 0000
41Bh	T6PR	TMR4 Period Register								1111 1111	1111 1111
41Ch	T6CON	ON	CKPS<2:0>			OUTPS<3:0>				0000 0000	0000 0000
41Dh	T6HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					0000 0000	0000 0000
41Eh	T6CLKCON	—	—	—	—	CS<3:0>				---- 0000	---- 0000
41Fh	T6RST	—	—	—	—	RSEL<3:0>				---- 0000	---- 0000
Bank 9											
48Ch to 492h	—	Unimplemented								—	—
493h	TMR3L	Holding Register for the Least Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
494h	TMR3H	Holding Register for the Most Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
495h	T3CON	CS<1:0>		CKPS<1:0>		OSCEN	$\overline{\text{SYNC}}$	—	ON	0000 00-0	uuuu uu-u
496h	T3GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	GSS<1:0>		0000 0x00	uuuu uxuu
497h to 499h	—	Unimplemented								—	—
49Ah	TMR5L	Holding Register for the Least Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
49Bh	TMR5H	Holding Register for the Most Significant Byte of the 16-Bit TMR1 Register								xxxx xxxx	uuuu uuuu
49Ch	T5CON	CS<1:0>		CKPS<1:0>		OSCEN	$\overline{\text{SYNC}}$	—	ON	0000 00-0	uuuu uu-u
49Dh	T5GCON	GE	GPOL	GTM	GSPM	GGO/$\overline{\text{DONE}}$	GVAL	GSS<1:0>		0000 0x00	uuuu uxuu
49Eh to 49Fh	—	Unimplemented								—	—

Legend: x = unknown; u = unchanged; q = value depends on condition; - = unimplemented, read as '0'; r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: Unimplemented, read as '1'.
2: PIC16(L)F1768/9 only.
3: PIC16(L)F1764/5 only.
4: Unimplemented on PIC16LF1764/5/8/9.

REGISTER 7-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **TMR1GIE:** Timer1 Gate Interrupt Enable bit
1 = Enables the Timer1 gate acquisition interrupt
0 = Disables the Timer1 gate acquisition interrupt

bit 6 **ADIE:** Analog-to-Digital Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 5 **RCIE:** EUSART Receive Interrupt Enable bit
1 = Enables the EUSART receive interrupt
0 = Disables the EUSART receive interrupt

bit 4 **TXIE:** EUSART Transmit Interrupt Enable bit
1 = Enables the EUSART transmit interrupt
0 = Disables the EUSART transmit interrupt

bit 3 **SSP1IE:** Master Synchronous Serial Port (MSSP) Interrupt Enable bit
1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 2 **CCP1IE:** CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1 **TMR2IE:** TMR2 to T2PR Match Interrupt Enable bit
1 = Enables the Timer2 to T2PR match interrupt
0 = Disables the Timer2 to T2PR match interrupt

bit 0 **TMR1IE:** Timer1 Overflow Interrupt Enable bit
1 = Enables the Timer1 overflow interrupt
0 = Disables the Timer1 overflow interrupt

Note: Bit PEIE of the INTCON register must be set to enable any peripheral interrupt.

TABLE 7-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPTS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			214
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	102
PIE2	OSFIE	C2IE	C1IE	—	BCL1IE	C4IE(1)	C3IE(1)	CCP2IE(1)	103
PIE3	PWM6IE(1)	PWM5IE	COG1IE	ZCDIE	COG2IE(1)	CLC3IE	CLC2IE	CLC1IE	104
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	105
PIR2	OSFIF	C2IF	C1IF	—	BCL1IF	C4IF(1)	C3IF(1)	CCP2IF(1)	106
PIR3	PWM6IF(1)	PWM5IF	COG1IF	ZCDIF	COG2IF(1)	CLC3IF	CLC2IF	CLC1IF	107

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by interrupts.

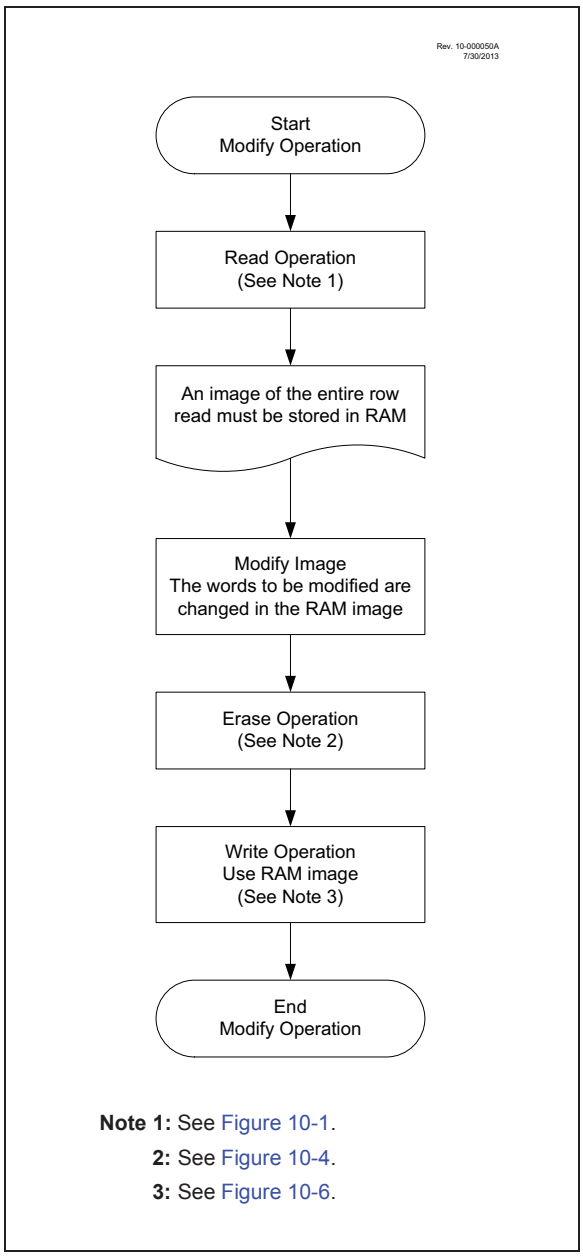
Note 1: PIC16(L)F1768/9 only.

10.3 Modifying Flash Program Memory

When modifying existing data in a program memory row, and data within that row must be preserved, it must first be read and saved in a RAM image. Program memory is modified using the following steps:

1. Load the starting address of the row to be modified.
2. Read the existing data from the row into a RAM image.
3. Modify the RAM image to contain the new data to be written into program memory.
4. Load the starting address of the row to be rewritten.
5. Erase the program memory row.
6. Load the write latches with data from the RAM image.
7. Initiate a programming operation.

FIGURE 10-7: FLASH PROGRAM MEMORY MODIFY FLOWCHART



Note 1: See Figure 10-1.
2: See Figure 10-4.
3: See Figure 10-6.

11.4 Register Definitions: PORTB

REGISTER 11-9: PORTB: PORTB REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0
RB<7:4>(1)				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **RB<7:4>**: PORTB General Purpose I/O Pin bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

bit 3-0 **Unimplemented:** Read as '0'

Note 1: Writes to PORTB are actually written to the corresponding LATB register. Reads from PORTB register are the return of the actual I/O pin values.

REGISTER 11-10: TRISB: PORTB TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
TRISB<7:4>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **TRISB<7:4>:** PORTB Tri-State Control bits
1 = PORTB pin is configured as an input (tri-stated)
0 = PORTB pin is configured as an output

bit 3-0 **Unimplemented:** Read as '0'

REGISTER 11-19: LATC: PORTC DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATC<7:0>(1)							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-0 **LATC<7:0>**: PORTC Output Latch Value bits(1)

Note 1: LATC<7:6> are available on PIC16(L)F1768/9 only.

REGISTER 11-20: ANSELC: PORTC ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSC<7:6>(2)		—	—	ANSC<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-6 **ANSC<7:6>**: Analog Select Between Analog or Digital Function on RC<7:6> Pins bits(2)
- 1 = Analog input; pin is assigned as an analog input, digital input buffer is disabled(1)
- 0 = Digital I/O; pin is assigned to port or digital special function

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **ANSC<3:0>**: Analog Select Between Analog or Digital Function on RC<3:0> Pins bits
- 1 = Analog input; pin is assigned as an analog input, digital input buffer is disabled(1)
- 0 = Digital I/O; pin is assigned to port or digital special function

Note 1: When setting a pin to an analog input, the corresponding TRISx bit must be set to Input mode in order to allow external control of the voltage on the pin.

2: ANSC<7:6> are available on PIC16(L)F1768/9 only.

17.0 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 32 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- Operational amplifier inverting and non-inverting inputs
- ADC input channel
- DACxOUT1 pin

TABLE 17-1: AVAILABLE 5-BIT DACs

Device	D3	D4
PIC16(L)F1764	•	
PIC16(L)F1765	•	
PIC16(L)F1768	•	•
PIC16(L)F1769	•	•

The Digital-to-Analog Converter (DAC) is enabled by setting the EN bit of the DACxCON0 register.

17.1 Output Voltage Selection

The DAC has 32 voltage level ranges. The 32 levels are set with the REF<4:0> bits of the DACxREF register.

The DAC output voltage is determined by Equation 17-1.

EQUATION 17-1: DAC OUTPUT VOLTAGE

IF DACxEN = 1:

$$V_{OUT} = \left((V_{SOURCE+} - V_{SOURCE-}) \times \frac{DACxR[4:0]}{2^5} \right) + V_{SOURCE-}$$

$V_{SOURCE+} = V_{DD}$, V_{REF}, *or FVR Buffer2*

$V_{SOURCE-} = V_{SS}$

17.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

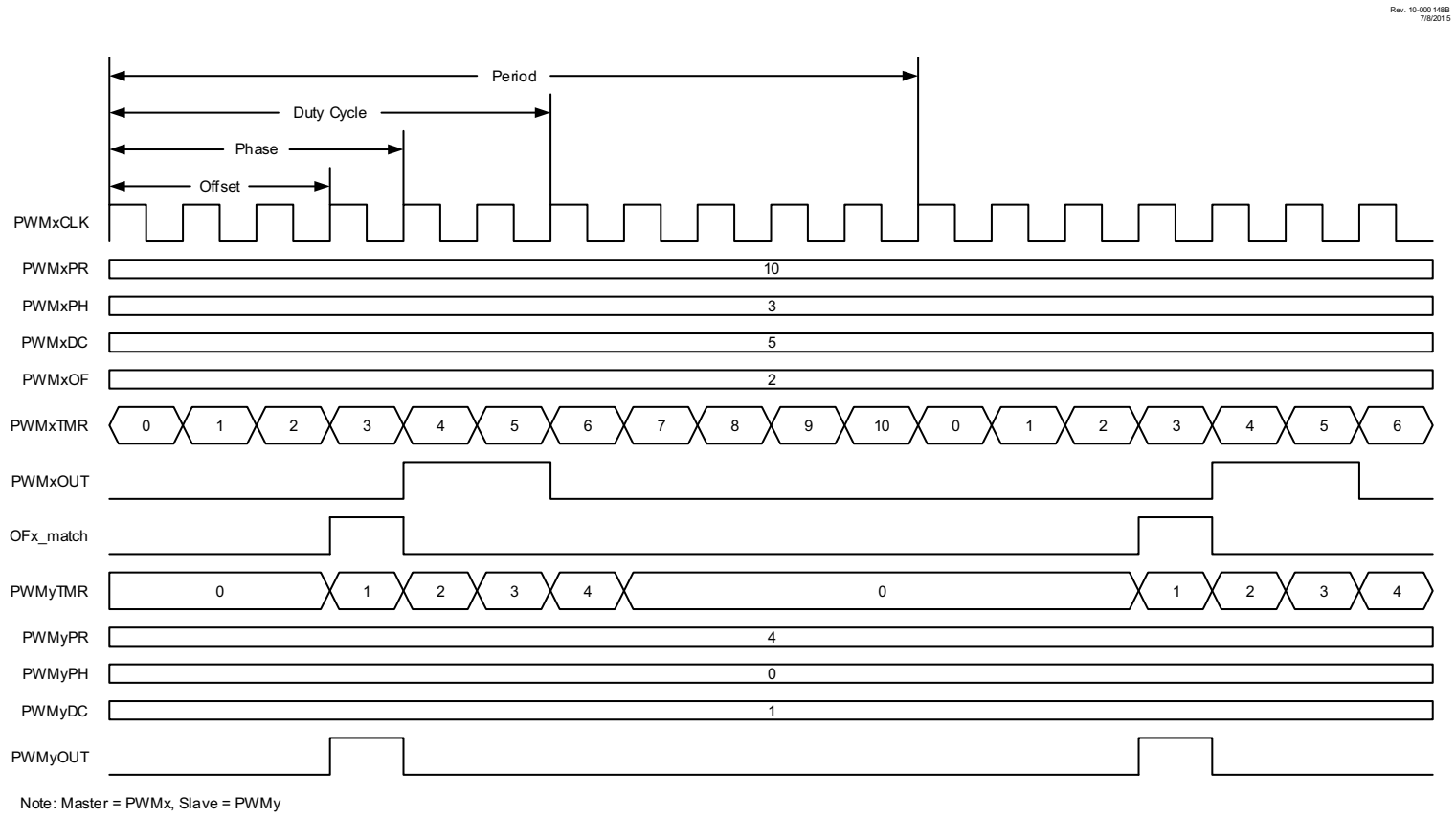
The value of the individual resistors within the ladder can be found in Table 36-20.

17.3 DAC Voltage Reference Output

The DAC voltage can be output to the DACxOUT1 pin by setting the OE1 bit of the DACxCON0 register. Selecting the DAC voltage for output on the DACxOUT1 pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DACxOUT1 pin when it has been configured for DAC voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage output for external connections to the DACxOUT1 pin. Figure 17-2 shows an example buffering technique.

FIGURE 26-10: ONE-SHOT SLAVE RUN MODE WITH SYNC START TIMING DIAGRAM



27.15 Register Definitions: COG Control

Long bit name prefixes for the COG peripherals are shown in Table 27-3. Refer to **Section 1.1 "Register and Bit Naming Conventions"** for more information.

TABLE 27-3: BIT NAME PREFIXES

Peripheral	Bit Name Prefix
COG1	G1
COG2(1)	G2

Note 1: PIC16(L)F1768/9 devices only.

REGISTER 27-1: COGxCON0: COGx CONTROL REGISTER 0

R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
EN	LD	—	CS<1:0>		MD<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **EN:** COGx Enable bit
- 1 = Module is enabled
- 0 = Module is disabled

bit 6 **LD:** COGx Load Buffers bit
- 1 = Phase, blanking and dead-band buffers to be loaded with register values on next input events
- 0 = Register to buffer transfer is complete

bit 5 **Unimplemented:** Read as '0'

bit 4-3 **CS<1:0>:** COGx Clock Selection bits
- 11 = Reserved; do not use
- 10 = COG_clock is HFINTOSC (stays active during Sleep)
- 01 = COG_clock is FOSC
- 00 = COG_clock is FOSC/4

bit 2-0 **MD<2:0>:** COGx Mode Selection bits
- 11x = Reserved; do not use
- 101 = COG outputs operate in Push-Pull mode
- 100 = COG outputs operate in Half-Bridge mode
- 011 = COG outputs operate in Reverse Full-Bridge mode
- 010 = COG outputs operate in Forward Full-Bridge mode
- 001 = COG outputs operate in Synchronous Steered PWM mode
- 000 = COG outputs operate in Steered PWM mode

FIGURE 31-2: ON-OFF KEYING (OOK) SYNCHRONIZATION

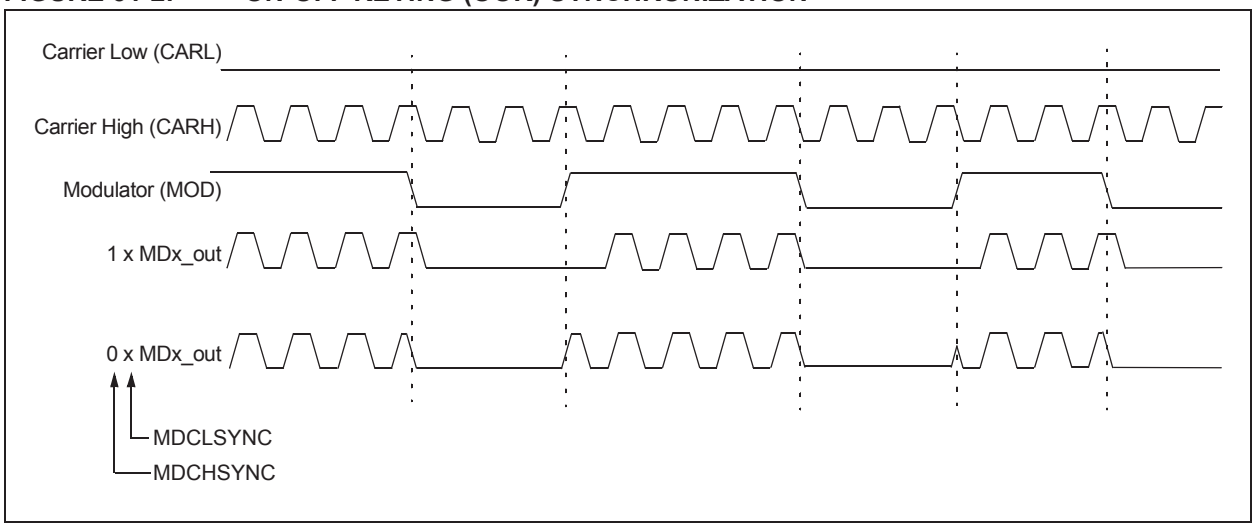


FIGURE 31-3: NO SYNCHRONIZATION (MDCHSYNC = 0, MDCLSYNC = 0)

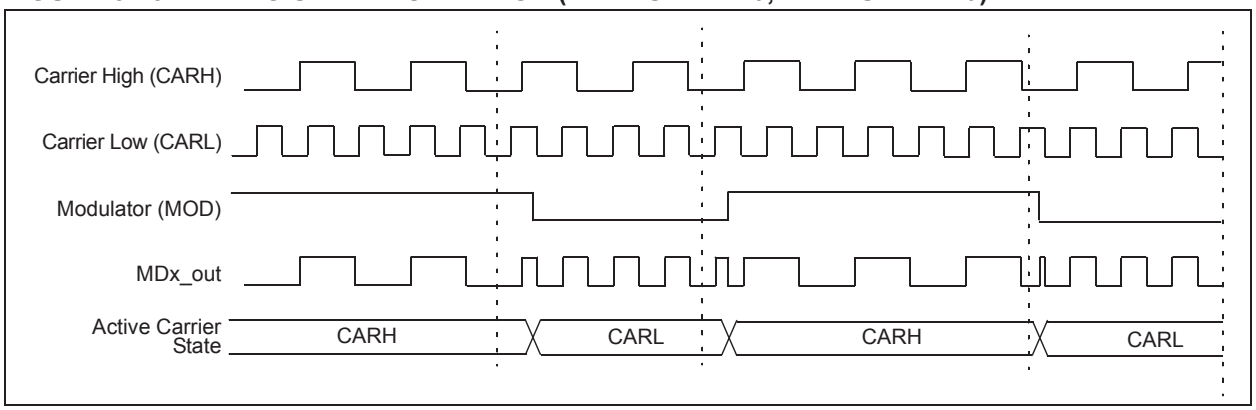
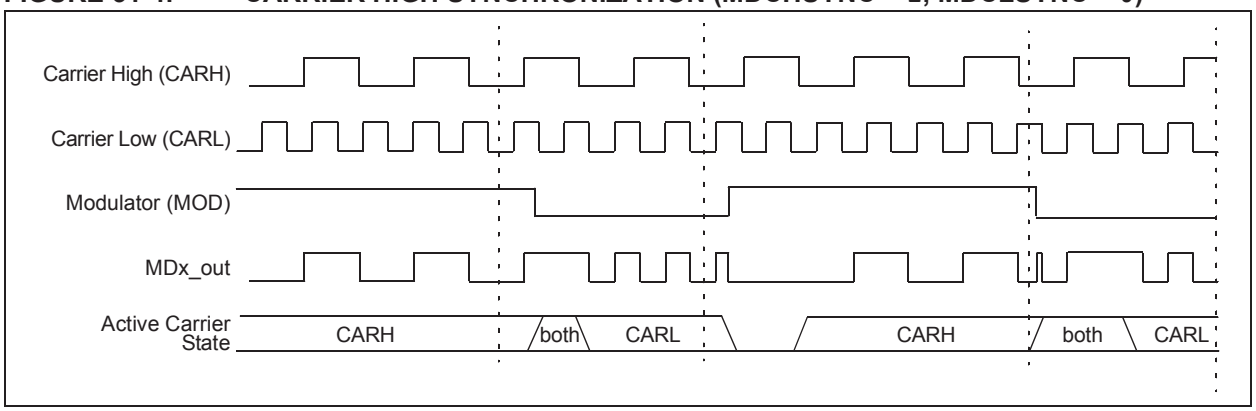


FIGURE 31-4: CARRIER HIGH SYNCHRONIZATION (MDCHSYNC = 1, MDCLSYNC = 0)



32.4.9 ACKNOWLEDGE SEQUENCE

The 9th SCL pulse for any transferred byte in I^{2}C is dedicated as an Acknowledge. It allows receiving devices to respond back to the transmitter by pulling the SDA line low. The transmitter must release control of the line during this time to shift in the response. The Acknowledge ($\overline{ACK}$) is an active-low signal, pulling the SDA line low indicates to the transmitter that the device has received the transmitted data and is ready to receive more.

The result of an $\overline{ACK}$ is placed in the ACKSTAT bit of the SSPxCON2 register.

Slave software, when the AHEN and DHEN bits are set, allows the user to set the $\overline{ACK}$ value sent back to the transmitter. The ACKDT bit of the SSPxCON2 register is set/cleared to determine the response.

Slave hardware will generate an $\overline{ACK}$ response if the AHEN and DHEN bits of the SSPxCON3 register are clear.

There are certain conditions where an $\overline{ACK}$ will not be sent by the slave. If the BF bit of the SSPxSTAT register or the SSPOV bit of the SSPxCON1 register are set when a byte is received.

When the module is addressed, after the eighth falling edge of SCL on the bus, the ACKTIM bit of the SSPxCON3 register is set. The ACKTIM bit indicates the Acknowledge time of the active bus. The ACKTIM status bit is only active when the AHEN bit or DHEN bit is enabled.

32.5 I^{2}C Slave Mode Operation

The MSSP Slave mode operates in one of four modes selected by the SSPM<3:0> bits of SSPxCON1 register. The modes can be divided into 7-Bit and 10-Bit Addressing modes. 10-Bit Addressing mode operates the same as 7-bit with some additional overhead for handling the larger addresses.

Modes with Start and Stop bit interrupts operate the same as the other modes, with SSPxIF additionally getting set upon detection of a Start, Restart or Stop condition.

32.5.1 SLAVE MODE ADDRESSES

The SSPxADD register (Register 32-6) contains the Slave mode address. The first byte received after a Start or Restart condition is compared against the value stored in this register. If the byte matches, the value is loaded into the SSPxBUF register and an interrupt is generated. If the value does not match, the module goes Idle and no indication is given to the software that anything happened.

The SSP Mask register (Register 32-5) affects the address matching process. See **Section 32.5.8 "SSP Mask Register"** for more information.

32.5.1.1 I^{2}C Slave 7-Bit Addressing Mode

In 7-Bit Addressing mode, the LSb of the received data byte is ignored when determining if there is an address match.

32.5.1.2 I^{2}C Slave 10-Bit Addressing Mode

In 10-Bit Addressing mode, the first received byte is compared to the binary value of '1 1 1 1 0 A9 A8 0'. A9 and A8 are the two MSbs of the 10-bit address and stored in bits 2 and 1 of the SSPxADD register.

After the Acknowledge of the high byte, the UA bit is set and SCL is held low until the user updates SSPxADD with the low address. The low address byte is clocked in and all eight bits are compared to the low address value in SSPxADD. Even if there is not an address match, SSPxIF and UA are set, and SCL is held low until SSPxADD is updated to receive a high byte again. When SSPxADD is updated, the UA bit is cleared. This ensures the module is ready to receive the high address byte on the next communication.

A high and low address match as a write request is required at the start of all 10-Bit Addressing communication. A transmission can be initiated by issuing a Restart once the slave is addressed, and clocking in the high address with the R/$\overline{W}$ bit set. The slave hardware will then Acknowledge the read request and prepare to clock out data. This is only valid for a slave after it has received a complete high and low address byte match.

32.5.7 GENERAL CALL ADDRESS SUPPORT

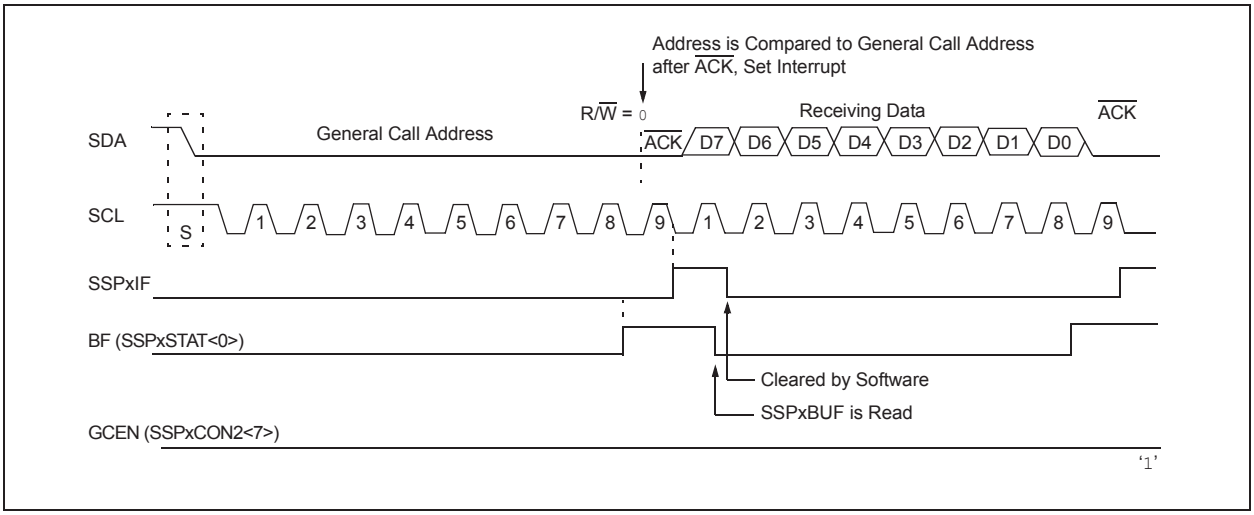
The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is a reserved address in the I^2C protocol, defined as address: 0x00. When the GCEN bit of the SSPxCON2 register is set, the slave module will automatically $\overline{ACK}$ the reception of this address, regardless of the value stored in SSPxADD. After the slave clocks in an address of all zeros, with the R/$\overline{W}$ bit clear, an interrupt is generated and slave software can read SSPxBUF and respond. Figure 32-24 shows a general call reception sequence.

In 10-Bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPxCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the eighth falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.

FIGURE 32-24: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE



32.5.8 SSP MASK REGISTER

An MSSP Mask (SSPxMSK) register (Register 32-5) is available in I^2C Slave mode as a mask for the value held in the SSPSR register during an address comparison operation. A zero ('0') bit in the SSPxMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition, and therefore, has no effect on standard SSP operation until written with a mask value.

The MSSP Mask register is active during:

- 7-Bit Address mode: Address compare of A<7:1>.
- 10-Bit Address mode: Address compare of A<7:0> only. The MSSP mask has no effect during the reception of the first (high) byte of the address.

32.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out (Case 1).

b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high (Case 2).

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSPxADD and counts down to zero. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 32-38). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 32-39).

FIGURE 32-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)

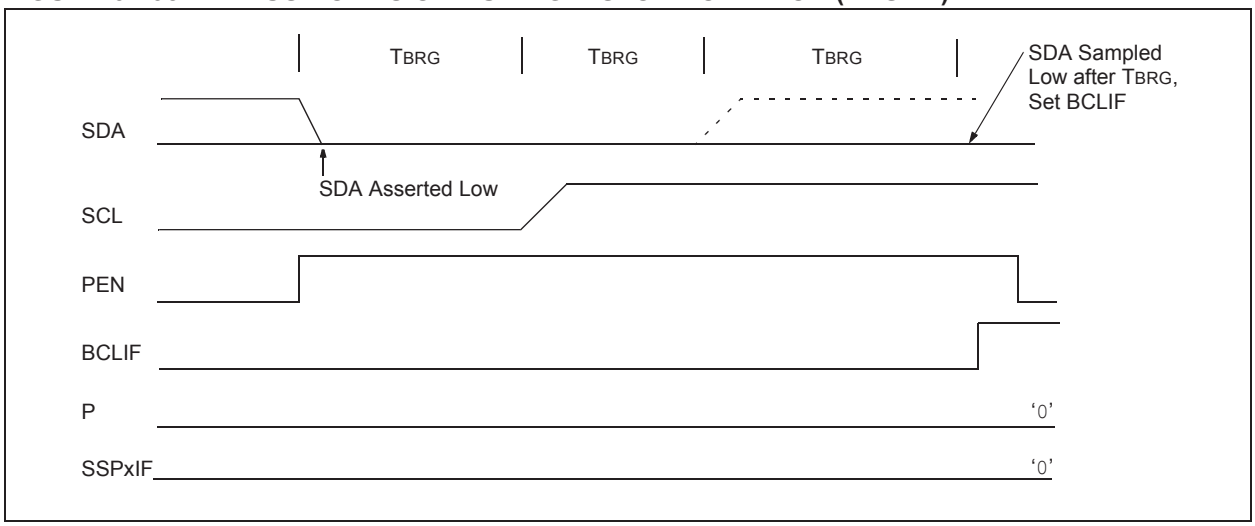
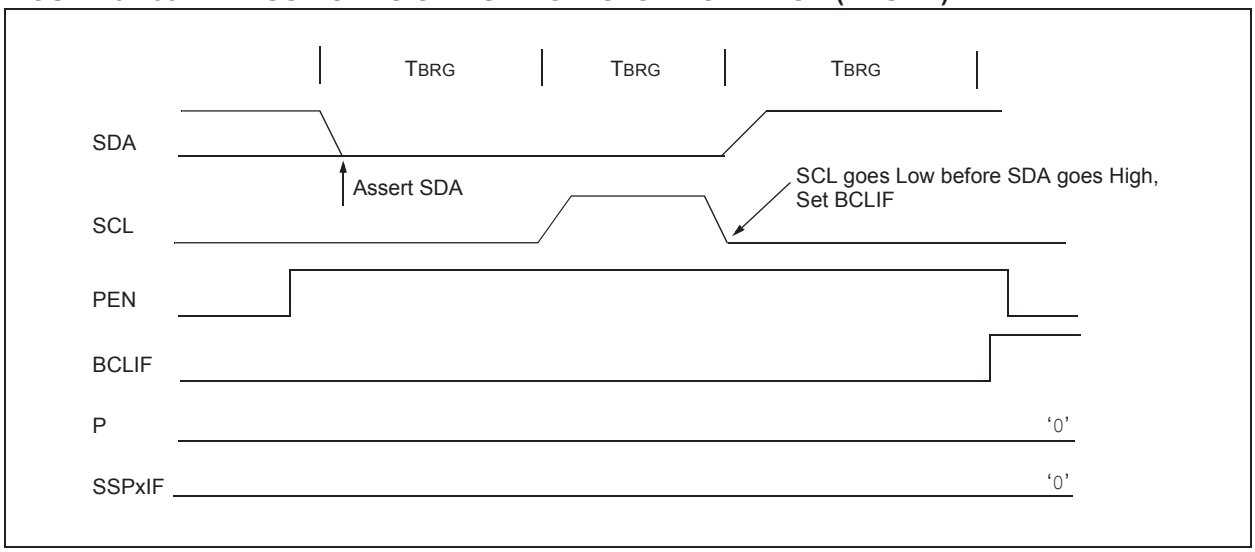


FIGURE 32-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



REGISTER 32-4: SSP1CON3: MSSP CONTROL REGISTER 3

R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ACKTIM(3)	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **ACKTIM:** Acknowledge Time Status bit (I^2C slave modes only)(3)
1 = Indicates the I^2C bus is in an Acknowledge sequence, set on eighth falling edge of SCL clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCL clock

bit 6 **PCIE**: Stop Condition Interrupt Enable bit (I^2C slave modes only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled(2)

bit 5 **SCIE**: Start Condition Interrupt Enable bit (I^2C slave modes only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled(2)

bit 4 **BOEN:** Buffer Overwrite Enable bit
In SPI Slave mode:(1)
1 = SSPxBUF updates every time that a new data byte is shifted in, ignoring the BF bit
0 = If new byte is received with BF bit of the SSPxSTAT register already set, the SSPOV bit of the SSPxCON1 register is set and the buffer is not updated
In I^2C Master mode and SPI Master mode:
This bit is ignored.
In I^2C Slave mode:
1 = SSPxBUF is updated and $\overline{ACK}$ is generated for a received address/data byte, ignoring the state of the SSPOV bit only if the BF bit = 0
0 = SSPxBUF is only updated when SSPOV is clear

bit 3 **SDAHT:** SDA Hold Time Selection bit (I^2C mode only)
1 = Minimum of 300 ns hold time on SDA after the falling edge of SCL
0 = Minimum of 100 ns hold time on SDA after the falling edge of SCL

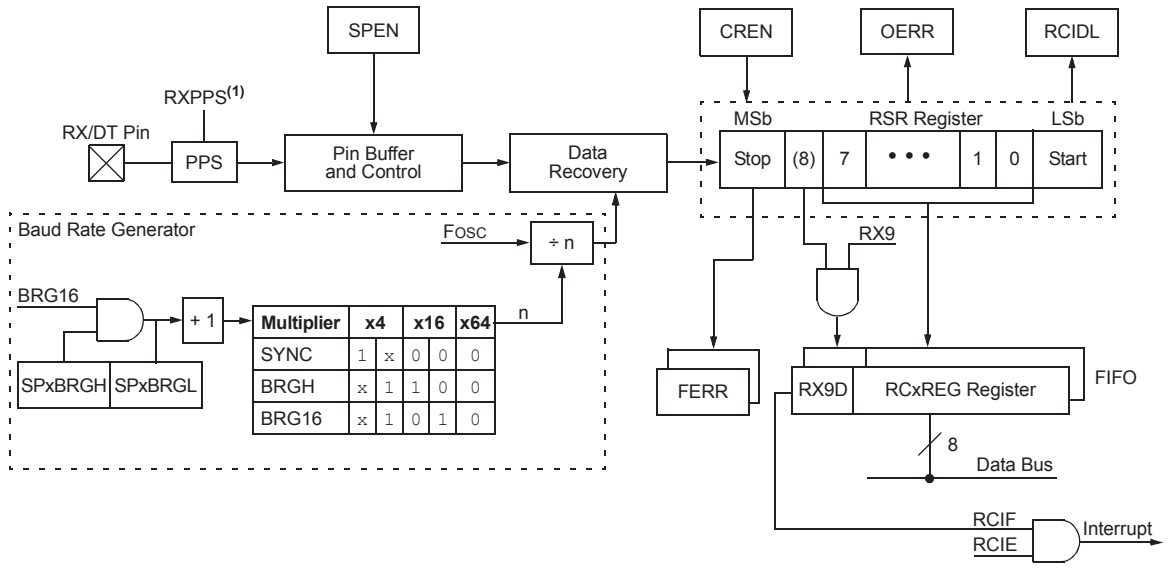
bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
If, on the rising edge of SCL, SDA is sampled low when the module is outputting a high state, the BCL1IF bit of the PIR2 register is set and the bus goes Idle
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the eighth falling edge of SCL for a matching received address byte; CKP bit of the SSPxCON1 register will be cleared and the SCL will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the eighth falling edge of SCL for a received data byte; slave hardware clears the CKP bit of the SSPxCON1 register and SCL is held low
0 = Data holding is disabled

Note 1: For daisy-chained SPI operation; allows the user to ignore all but the last received byte. SSPOV is still set when a new byte is received and BF = 1, but hardware continues to write the most recent byte to SSP1BUF.
2: This bit has no effect in Slave modes in which Start and Stop condition detection is explicitly listed as enabled.
3: The ACKTIM status bit is only active when the AHEN bit or DHEN bit is set.

FIGURE 33-2: EUSART RECEIVE BLOCK DIAGRAM



Note 1: In Synchronous mode, the DT output and RX input PPS selections should enable the same pin.

The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXxSTA)
- Receive Status and Control (RCxSTA)
- Baud Rate Control (BAUDxCON)

These registers are detailed in Register 33-1, Register 33-2 and Register 33-3, respectively.

The RX and CK input pins are selected with the RXPPS and CKPPS registers, respectively. TX, CK and DT output pins are selected with each pin's RxyPPS register. Since the RX input is coupled with the DT output in Synchronous mode, it is the user's responsibility to select the same pin for both of these functions when operating in Synchronous mode. The EUSART control logic will control the data direction drivers automatically.

TABLE 36-15: ANALOG-TO-DIGITAL CONVERTER (ADC) CHARACTERISTICS(1,2,3,4)

Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = +25°C, Single-Ended, 2 µs TAD, VREF+ = 3V, VREF- = VSS							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10	bit	
AD02	EIL	Integral Error	—	—	±1.7	LSb	VREF = 3.0V
AD03	EDL	Differential Error	—	—	±1	LSb	No missing codes, VREF = 3.0V
AD04	EOFF	Offset Error	—	—	±2.5	LSb	VREF = 3.0V
AD05	EGN	Gain Error	—	—	±2.0	LSb	VREF = 3.0V
AD06	VREF	Reference Voltage	1.8	—	VDD	V	VREF = (VREF+ – VREF-)
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	Can go higher if external 0.01 µF capacitor is present on input pin

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The ADC conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF+ pin, VDD pin or FVR, whichever is selected as reference input.

4: See **Section 37.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.

TABLE 36-16: ADC CONVERSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD130*	TAD	ADC Clock Period (TADC)	1.0	—	9.0	µs	FOSC-based
		ADC Internal FRC Oscillator Period (TFRC)	1.0	2	6.0	µs	ADCS<1:0> = 11 (ADC FRC mode)
AD131	TCNV	Conversion Time (not including Acquisition Time)(1)	—	11	—	TAD	Set GO/$\overline{\text{DONE}}$ bit to conversion complete
AD132*	TACQ	Acquisition Time	—	5.0	—	µs	
AD133*	THCD	Holding Capacitor Disconnect Time	—	1/2 TAD	—		ADCS<2:0> ≠ x11 (FOSC-based)
			—	1/2 TAD + 1 TCY	—		ADCS<2:0> = x11 (FRC-based)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The ADRES register may be read on the following TCY cycle.

TABLE 36-17: OPERATIONAL AMPLIFIER (OPA)

Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = +25°C, OPAxSP = 1 (High GBWP mode)							
Param No.	**Symbol**	**Parameters**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
OPA01*	GBWP	Gain Bandwidth Product	—	3	—	MHz	
OPA02*	TON	Turn-on Time	—	10	—	µs	
OPA03*	PM	Phase Margin	—	40	—	degrees	
OPA04*	SR	Slew Rate	—	3	—	V/µs	
OPA05	OFF	Offset	—	±3	±9	mV	
OPA06	CMRR	Common-Mode Rejection Ratio	52	70	—	dB	
OPA07*	AOL	Open-Loop Gain	—	90	—	dB	
OPA08	VICM	Input Common-Mode Voltage	0	—	VDD	V	VDD > 2.5V
OPA09*	PSRR	Power Supply Rejection Ratio	—	80	—	dB	
OPA10*	HZ	High-Impedance On/Off Time	—	50	—	ns	
OPA11*	ISC	Short Circuit Current	—	50	—	mA	

* These parameters are characterized but not tested.

TABLE 36-18: PROGRAMMABLE RAMP GENERATOR (PRG) SPECIFICATIONS

Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = +25°C (unless otherwise stated)							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
PRG01	RRR	Rising Ramp Rate	—	1	—	V/µs	PRGxCON2 = 10h
PRG02	FRR	Falling Ramp Rate	—	1	—	V/µs	PRGxCON2 = 10h

* These parameters are characterized but not tested.

TABLE 36-19: COMPARATOR SPECIFICATIONS

Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = +25°C See **Section 37.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
CM01	VIOFF	Input Offset Voltage	—	±2.5	±5	mV	VICM = VDD/2
CM02	VICM	Input Common-Mode Voltage	0	—	VDD	V	
CM03	CMRR	Common-Mode Rejection Ratio	35	50	—	dB	
CM04A	TRESP(1)	Response Time Rising Edge	—	60	125	ns	Normal Power mode
CM04B		Response Time Falling Edge	—	60	110	ns	Normal Power mode
CM04C		Response Time Rising Edge	—	85	—	ns	Low-Power mode
CM04D		Response Time Falling Edge	—	85	—	ns	Low-Power mode
CM05*	TMC2OV	Comparator Mode Change to Output Valid*	—	—	10	µs	
CM06	CHYSTER	Comparator Hysteresis	20	45	75	mV	CxHYS = 1

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at VDD/2, while the other input transitions from VSS to VDD.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

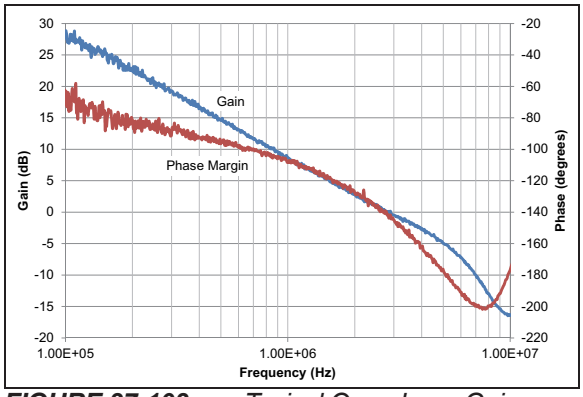


FIGURE 37-103: *Typical Open Loop Gain, Phase Vs. Frequency, PIC16F1764/5/8/9 Only.*

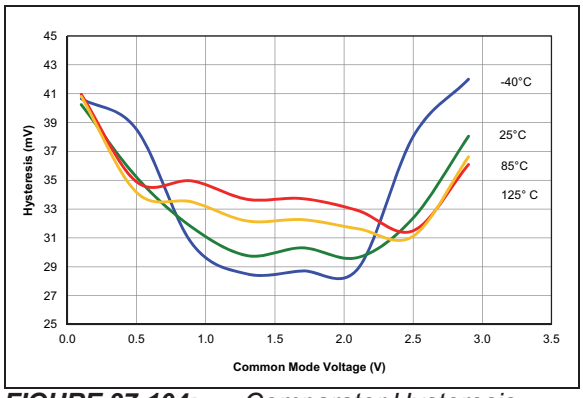


FIGURE 37-104: *Comparator Hysteresis, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values.*

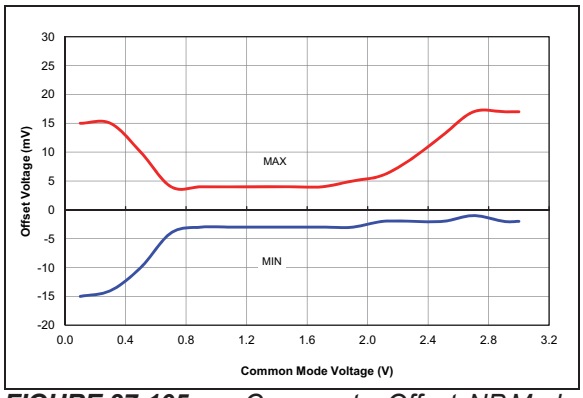


FIGURE 37-105: *Comparator Offset, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values at 25°C.*

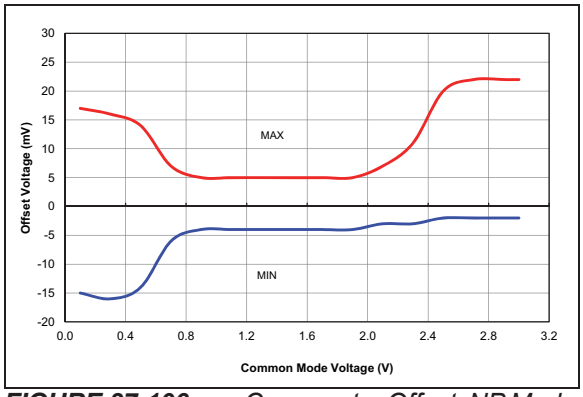


FIGURE 37-106: *Comparator Offset, NP Mode (CxSP = 1), VDD = 3.0V, Typical Measured Values From -40°C to 125°C.*

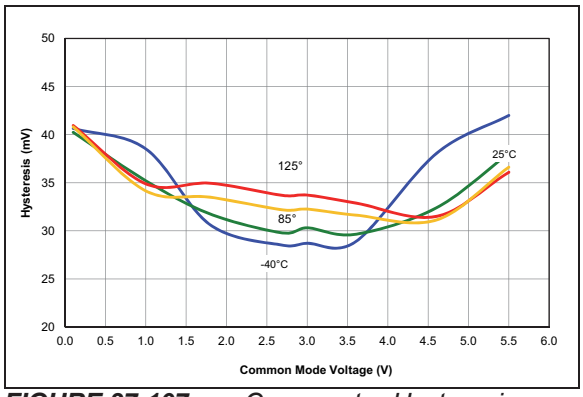


FIGURE 37-107: *Comparator Hysteresis, NP Mode (CxSP = 1), VDD = 5.5V, Typical Measured Values, PIC16F1764/5/8/9 Only.*

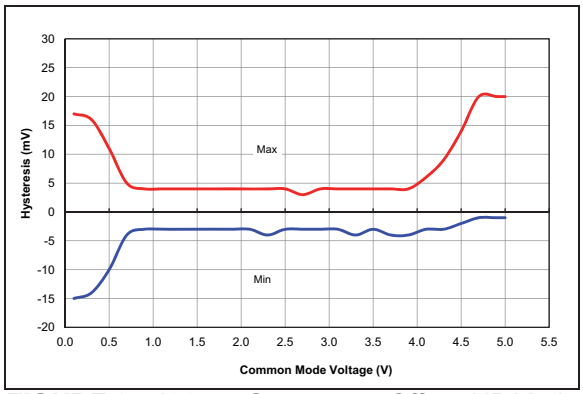


FIGURE 37-108: *Comparator Offset, NP Mode (CxSP = 1), VDD = 5.0V, Typical Measured Values at 25°C, PIC16F1764/5/8/9 Only.*

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