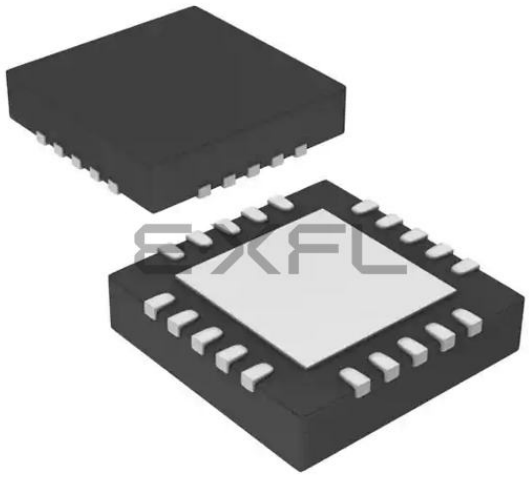

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	18
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x5b, 2x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VFQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1769t-i-ml

TABLE 1-3: PIC16(L)F1768/9 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC6/AN8/OPA2IN0-/$\overline{SS}$	RC6	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN0-	AN	—	Operational Amplifier 2 inverting input.
	$\overline{SS}$(1)	TTL/ST	—	SPI Slave Select input.
RC7/AN9/OPA2IN0+	RC7	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	OPA2IN0+	AN	—	Operational Amplifier 2 non-inverting input.
VDD	VDD	Power	—	Positive supply.
VSS	VSS	Power	—	Ground reference.
OUT(2)	C1OUT		CMOS	Comparator 1 output.
	C2OUT		CMOS	Comparator 2 output.
	C3OUT		CMOS	Comparator 3 output.
	C4OUT		CMOS	Comparator 4 output.
	CCP1		CMOS	Compare/PWM1 output.
	CCP2		CMOS	Compare/PWM2 output.
	MD1OUT		CMOS	Data Signal Modulator 1 output.
	MD2OUT		CMOS	Data Signal Modulator 2 output.
	PWM3		CMOS	PWM3 output.
	PWM4		CMOS	PWM4 output.
	PWM5		CMOS	PWM5 output.
	PWM6		CMOS	PWM6 output.
	COG1A		CMOS	Complementary Output Generator 1 Output A.
	COG1B		CMOS	Complementary Output Generator 1 Output B.
	COG1C		CMOS	Complementary Output Generator 1 Output C.
	COG1D		CMOS	Complementary Output Generator 1 Output D.
	COG2A		CMOS	Complementary Output Generator 2 Output A.
	COG2B		CMOS	Complementary Output Generator 2 Output B.
	COG2C		CMOS	Complementary Output Generator 2 Output C.
	COG2D		CMOS	Complementary Output Generator 2 Output D.
	SDA(3)		OD	I^2C data output.
	SCK		CMOS	SPI clock output.
	SCL(3)		OD	I^2C clock output.
	SDO		CMOS	SPI data output.
	TX		CMOS	EUSART asynchronous TX data out.
	CK		CMOS	EUSART synchronous clock out.
	DT(3)		CMOS	EUSART synchronous data output.
	CLC1OUT		CMOS	Configurable Logic Cell 1 output.
	CLC2OUT		CMOS	Configurable Logic Cell 2 output.
	CLC3OUT		CMOS	Configurable Logic Cell 3 output.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Default peripheral input. Alternate pins can be selected as the peripheral input with the PPS Input Selection registers.

2: All pin digital outputs default to PORT latch data. Alternate outputs can be selected as peripheral digital outputs with the PPS Output Selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

REGISTER 4-2: CONFIG2: CONFIGURATION WORD 2 (CONTINUED)

bit 1-0 **WRT<1:0>:** Flash Memory Self-Write Protection bits

4 kW Flash Memory (PIC16(L)F1764/8):

11 = Off Write protection is off

10 = Boot 0000h to 01FFh are write-protected, 0200h to 0FFFh may be modified by PMCON control

01 = Half 0000h to 07FFh are write-protected, 0800h to 0FFFh may be modified by PMCON control

00 = All 0000h to 0FFFh are write-protected, no addresses may be modified by PMCON control

8 kW Flash Memory (PIC16(L)F1765/9):

11 = Off Write protection is off

10 = Boot 0000h to 01FFh are write-protected, 0200h to 1FFFh may be modified by PMCON control

01 = Half 0000h to 0FFFh are write-protected, 1000h to 1FFFh may be modified by PMCON control

00 = All 0000h to 1FFFh are write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to '0' when Programming mode is entered via LVP.

2: The $\overline{\text{DEBUG}}$ bit in the Configuration Words is managed automatically by device development tools, including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.

3: See V_{BOR} parameter for specific trip point voltages.

5.0 OSCILLATOR MODULE (WITH FAIL-SAFE CLOCK MONITOR)

5.1 Overview

The oscillator module has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. Figure 5-1 illustrates a block diagram of the oscillator module.

Clock sources can be supplied from external oscillators, quartz crystal resonators, ceramic resonators and Resistor-Capacitor (RC) circuits. In addition, the system clock source can be supplied from one of two internal oscillators and PLL circuits, with a choice of speeds selectable via software. Additional clock features include:

- Selectable system clock source between external or internal sources via software.
- Two-Speed Start-up mode, which minimizes latency between external oscillator start-up and code execution.
- Fail-Safe Clock Monitor (FSCM) designed to detect a failure of the external clock source (LP, XT, HS, ECH, ECM, ECL or EXTRC modes) and switch automatically to the internal oscillator.
- Oscillator Start-up Timer (OST) ensures stability of crystal oscillator sources.

The oscillator module can be configured in one of the following clock modes.

1. ECL – External Clock Low-Power mode (0 MHz to 0.5 MHz).
2. ECM – External Clock Medium Power mode (0.5 MHz to 4 MHz).
3. ECH – External Clock High-Power mode (4 MHz to 32 MHz).
4. LP – 32 kHz Low-Power Crystal mode.
5. XT – Medium Gain Crystal or Ceramic Resonator Oscillator mode (up to 4 MHz).
6. HS – High Gain Crystal or Ceramic Resonator mode (4 MHz to 20 MHz).
7. EXTRC – External Resistor-Capacitor.
8. INTOSC – Internal Oscillator (31 kHz to 32 MHz).

Clock source modes are selected by the FOSC<2:0> bits in the Configuration Words. The FOSCx bits determine the type of oscillator that will be used when the device is first powered.

The ECH, ECM and ECL Clock modes rely on an external logic level signal as the device clock source. The LP, XT and HS Clock modes require an external crystal or resonator to be connected to the device. Each mode is optimized for a different frequency range. The EXTRC Clock mode requires an external resistor and capacitor to set the oscillator frequency.

The Internal Oscillator Block (INTOSC) produces low, medium and high-frequency clock sources, designated LFINTOSC, MFINTOSC and HFINTOSC (see Internal Oscillator Block, Figure 5-1). A wide selection of device clock frequencies may be derived from these three clock sources.

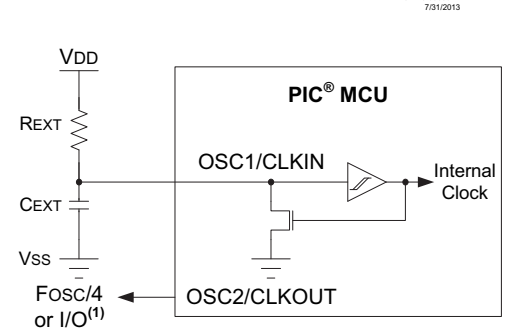
5.2.1.6 External RC Mode

The external Resistor-Capacitor (EXTRC) mode supports the use of an external RC circuit. This allows the designer maximum flexibility in frequency choice while keeping costs to a minimum when clock accuracy is not required.

The RC circuit connects to OSC1. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in the Configuration Words.

Figure 5-6 shows the external RC mode connections.

FIGURE 5-6: EXTERNAL RC MODES



Recommended values: 10 kΩ ≤ REXT ≤ 100 kΩ, <3V
3 kΩ ≤ REXT ≤ 100 kΩ, 3-5V
CEXT > 20 pF, 2-5V

Note 1: Output depends upon the CLKOUTEN bit of the Configuration Words.

The RC oscillator frequency is a function of the supply voltage, the Resistor (REXT) and Capacitor (CEXT) values, and the operating temperature. Other factors affecting the oscillator frequency are:

- Threshold voltage variation
- Component tolerances
- Packaging variations in capacitance

The user also needs to take into account variation due to tolerance of external RC components used.

5.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the Internal Oscillator Block as the system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in the Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to the internal oscillator during run time. See **Section 5.3 "Clock Switching"** for more information.

In **INTOSC** mode, OSC1/CLKIN is available for general purpose I/O. OSC2/CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the CLKOUTEN bit in the Configuration Words.

The Internal Oscillator Block has two independent oscillators and a dedicated Phase-Locked Loop (HFPLL) that can produce one of three internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 16 MHz. The HFINTOSC source is generated from the 500 kHz MFINTOSC source and the dedicated Phase-Locked Loop, HFPLL. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
2. The **MFINTOSC** (Medium Frequency Internal Oscillator) is factory calibrated and operates at 500 kHz. The frequency of the MFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
3. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

REGISTER 7-7: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PWM6IF(1)	PWM5IF	COG1IF	ZCDIF	COG2IF(1)	CLC3IF	CLC2IF	CLC1IF
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **PWM6IF:** PWM6 Interrupt Flag bit(1)
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 6 **PWM5IF:** PWM5 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 5 **COG1IF:** COG1 Auto-Shutdown Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 4 **ZCDIF:** Zero-Cross Detection Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 3 **COG2IF:** COG2 Auto-Shutdown Interrupt Flag bit(1)
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 2 **CLC3IF:** CLC3 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 1 **CLC2IF:** CLC2 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

bit 0 **CLC1IF:** CLC1 Interrupt Flag bit
- 1 = Interrupt is pending
- 0 = Interrupt is not pending

Note 1: PIC16(L)F1768/9 only.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 13-5: IOCBN: INTERRUPT-ON-CHANGE PORTB NEGATIVE EDGE REGISTER(1)

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
IOCBN<7:4>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-4 **IOCBN<7:4>:** Interrupt-On-Change PORTB Negative Edge Enable bits
- 1 = Interrupt-On-Change is enabled on the pin for a negative going edge; IOCBFx bit and IOCIF flag will be set upon edge detection
- 0 = Interrupt-On-Change is disabled for the associated pin

bit 3-0 **Unimplemented:** Read as '0'

Note 1: PIC16(L)F1768/9 only.

REGISTER 13-6: IOCBF: INTERRUPT-ON-CHANGE PORTB FLAG REGISTER(1)

R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	U-0	U-0	U-0	U-0
IOCBF<7:4>				—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS = Hardware Settable bit

bit 7-4 **IOCBF<7:4>:** Interrupt-On-Change PORTB Flag bits
- 1 = An enabled change was detected on the associated pin
  Set when IOCBPx = 1 and a rising edge was detected on RBx, or when IOCBNx = 1 and a falling edge was detected on RBx.
- 0 = No change was detected or the user cleared the detected change

bit 3-0 **Unimplemented:** Read as '0'

Note 1: PIC16(L)F1768/9 only.

REGISTER 23-2: TxCON: TIMERx CONTROL REGISTER

R/W/HC-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ON(1)	CKPS<2:0>			OUTPS<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Hardware Clearable bit

bit 7 **ON:** Timerx On bit
- 1 = Timerx is on
- 0 = Timerx is off; all counters and state machines are reset

bit 6-4 **CKPS<2:0>:** Timer2 Type Clock Prescale Select bits
- 111 = 1:128 Prescaler
- 110 = 1:64 Prescaler
- 101 = 1:32 Prescaler
- 100 = 1:16 Prescaler
- 011 = 1:8 Prescaler
- 010 = 1:4 Prescaler
- 001 = 1:2 Prescaler
- 000 = 1:1 Prescaler

bit 3-0 **OUTPS<3:0>:** Timerx Output Postscaler Select bits
- **1111** = 1:16 Postscaler
- **1110** = 1:15 Postscaler
- **1101** = 1:14 Postscaler
- **1100** = 1:13 Postscaler
- **1011** = 1:12 Postscaler
- **1010** = 1:11 Postscaler
- **1001** = 1:10 Postscaler
- **1000** = 1:9 Postscaler
- **0111** = 1:8 Postscaler
- **0110** = 1:7 Postscaler
- **0101** = 1:6 Postscaler
- **0100** = 1:5 Postscaler
- **0011** = 1:4 Postscaler
- **0010** = 1:3 Postscaler
- **0001** = 1:2 Postscaler
- **0000** = 1:1 Postscaler

Note 1: In certain modes, the ON bit will be auto-cleared by hardware. See **Section 23.6 "Operation Examples"**.

26.7 Register Definitions: PWM Control

Long bit name prefixes for the 16-bit PWM peripherals are shown in Table 26-1. Refer to **Section 1.1 "Register and Bit Naming Conventions"** for more information.

TABLE 26-1: BIT NAME PREFIXES

Peripheral	Bit Name Prefix
PWM5	PWM5
PWM6(1)	PWM6

Note 1: PIC16(L)F1768/9 devices only.

REGISTER 26-1: PWMxCON: PWMx CONTROL REGISTER

R/W-0/0	U-0	R/HS/HC-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0
EN	—	OUT	POL	MODE<1:0>		—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
HC = Hardware Clearable bit	HS = Hardware Settable bit	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **EN:** PWMx Module Enable bit
1 = Module is enabled
0 = Module is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **OUT:** Output State of the PWMx Module bit

bit 4 **POL:** PWMx Output Polarity Control bit
1 = PWMx output active state is low
0 = PWMx output active state is high

bit 3-2 **MODE<1:0>:** PWMx Mode Control bits
11 = Center-Aligned mode
10 = Toggle On Match mode
01 = Set On Match mode
00 = Standard PWM mode

bit 1-0 **Unimplemented:** Read as '0'

27.8.1 FALLING EVENT BLANKING OF RISING EVENT INPUTS

The falling event blanking counter inhibits rising event inputs from triggering a rising event. The falling event blanking time starts when the rising_event output drive goes false.

The falling event blanking time is set by the value contained in the COGxBLKF register (Register 27-17). Blanking times are calculated using the formula shown in Equation 27-1.

When the COGxBLKF value is zero, falling event blanking is disabled and the blanking counter output is true, thereby, allowing the event signal to pass straight through to the event trigger circuit.

27.8.2 RISING EVENT BLANKING OF FALLING EVENT INPUTS

The rising event blanking counter inhibits falling event inputs from triggering a falling event. The rising event blanking time starts when the falling_event output drive goes false.

The rising event blanking time is set by the value contained in the COGxBLKR register (Register 27-16).

When the COGxBLKR value is zero, rising event blanking is disabled and the blanking counter output is true, thereby, allowing the event signal to pass straight through to the event trigger circuit.

27.8.3 BLANKING TIME UNCERTAINTY

When the rising and falling sources that trigger the blanking counters are asynchronous to the COG_clock, it creates uncertainty in the blanking time. The maximum uncertainty is equal to one COG_clock period. Refer to Equation 27-1 and Example 27-1 for more detail.

27.9 Phase Delay

It is possible to delay the assertion of either, or both, the rising event and falling events. This is accomplished by placing a non-zero value in COGxPHR or COGxPHF phase-delay count registers, respectively (Register 27-18 and Register 27-19). Refer to Figure 27-10 for COG operation with CCP1 and phase delay. The delay from the input rising event signal switching to the actual assertion of the events is calculated the same as the dead-band and blanking delays. Refer to Equation 27-1.

When the phase-delay count value is zero, phase delay is disabled and the phase-delay counter output is true, thereby, allowing the event signal to pass straight through to the complementary output driver flop.

27.9.1 CUMULATIVE UNCERTAINTY

It is not possible to create more than one COG_clock of uncertainty by successive stages. Consider that the phase-delay stage comes after the blanking stage, the dead-band stage comes after either the blanking or phase-delay stages, and the blanking stage comes after the dead-band stage. When the preceding stage is enabled, the output of that stage is necessarily synchronous with the COG_clock, which removes any possibility of uncertainty in the succeeding stage.

EQUATION 27-1: PHASE, DEAD-BAND AND BLANKING TIME CALCULATION

$$T_{min} = \frac{Count}{F_{COG\_clock}}$$

$$T_{max} = \frac{Count + 1}{F_{COG\_clock}}$$

$$T_{uncertainty} = T_{max} - T_{min}$$

Also:

$$T_{uncertainty} = \frac{1}{F_{COG\_clock}}$$

Where:

T	Count
Rising Phase Delay	COGxPHR
Falling Phase Delay	COGxPHF
Rising Dead Band	COGxDBR
Falling Dead Band	COGxDBF
Rising Event Blanking	COGxBLKR
Falling Event Blanking	COGxBLKF

Note: All inputs to the COG should be treated as asynchronous for the purpose of determining blanking, phase delay, and dead-band delay uncertainty. One clock of uncertainty may occur as a result of signal path length differences between the source signal, such as a PWM output, and the source clock, such as FOSC, even though they both use the system clock as a timing source. The uncertainty is more evident at high frequencies and high temperature.

Work around

When possible, choose timing source frequencies less than 20 MHz. Use the asynchronous delay chain for dead-band delay.

27.10.3 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

The restart method is selected with the ARSEN bit of the COGxASD0 register. Waveforms of a software controlled automatic restart are shown in Figure 27-15.

27.10.3.1 Software Controlled Restart

When the ARSEN bit of the COGxASD0 register is cleared, software must clear the ASE bit to restart COG operation after an auto-shutdown event.

The COG will resume operation on the first rising event after the ASE bit is cleared. Clearing the shutdown state requires all selected shutdown inputs to be false; otherwise, the ASE bit will remain set.

27.10.3.2 Auto-Restart

When the ARSEN bit of the COGxASD0 register is set, the COG will restart from the auto-shutdown state automatically.

The ASE bit will clear automatically and the COG will resume operation on the first rising event after all selected shutdown inputs go false.

REGISTER 27-3: COGxRIS0: COGx RISING EVENT INPUT SELECTION REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
RIS7	RIS6	RIS5	RIS4	RIS3	RIS2	RIS1	RIS0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **RIS7:** COGx Rising Event Input Source 7 Enable bit
1 = PWM3 output is enabled as a rising event input
0 = PWM3 output has no effect on the rising event

bit 6 **RIS6:** COGx Rising Event Input Source 6 Enable bit
1 = CCP2 output is enabled as a rising event input
0 = CCP2 output has no effect on the rising event

bit 5 **RIS5:** COGx Rising Event Input Source 5 Enable bit
1 = CCP1 output is enabled as a rising event input
0 = CCP1 output has no effect on the rising event

bit 4 **RIS4:** COGx Rising Event Input Source 4 Enable bit
1 = Comparator 4 output is enabled as a rising event input
0 = Comparator 4 output has no effect on the rising event

bit 3 **RIS3:** COGx Rising Event Input Source 3 Enable bit
1 = Comparator 3 output is enabled as a rising event input
0 = Comparator 3 output has no effect on the rising event

bit 2 **RIS2:** COGx Rising Event Input Source 2 Enable bit
1 = Comparator 2 output is enabled as a rising event input
0 = Comparator 2 output has no effect on the rising event

bit 1 **RIS1:** COGx Rising Event Input Source 1 Enable bit
1 = Comparator 1 output is enabled as a rising event input
0 = Comparator 1 output has no effect on the rising event

bit 0 **RIS0:** COGx Rising Event Input Source 0 Enable bit
1 = Pin selected with COGxINPPS register is enabled as rising event input
0 = Pin selected with COGxINPPS register has no effect on the rising event

REGISTER 28-11: CLCxDATA: CLCx DATA OUTPUT

U-0	U-0	U-0	U-0	U-0	R-0	R-0	R-0
—	—	—	—	—	MLC3OUT	MLC2OUT	MLC1OUT
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **MLC3OUT:** Mirror copy of LC3OUT bit

bit 1 **MLC2OUT:** Mirror copy of LC2OUT bit

bit 0 **MLC1OUT:** Mirror copy of LC1OUT bit

TABLE 28-4: SUMMARY OF REGISTERS ASSOCIATED WITH CLCx

Name	Bit7	Bit6	Bit5	Bit4	BIt3	Bit2	Bit1	Bit0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELB(1)	ANSB<7:4>				—	—	—	—	143
ANSELC	ANSC<7:6>(1)		—	—	ANSC<3:0>				148
CLCxCON	EN	—	OUT	INTP	INTN	MODE<2:0>			338
CLCDATA	—	—	—	—	—	MLC3OUT	MLC2OUT	MLC1OUT	345
CLCxGLS0	G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N	341
CLCxGLS1	G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N	342
CLCxGLS2	G3D4T	G3D4N	G3D3T	G3D3N	G3D2T	G3D2N	G3D1T	G3D1N	343
CLCxGLS3	G4D4T	G4D4N	G4D3T	G4D3N	G4D2T	G4D2N	G4D1T	G4D1N	344
CLCxPOL	POL	—	—	—	G4POL	G3POL	G2POL	G1POL	339
CLCxSEL0	—	—	D1S<5:0>						340
CLCxSEL1	—	—	D2S<5:0>						340
CLCxSEL2	—	—	D3S<5:0>						340
CLCxSEL3	—	—	D4S<5:0>						341
CLCxPPS	—	—	—	CLCxPPS<4:0>					154, 156
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
PIE3	PWM6IE(1)	PWM5IE	COG1IE	ZCDIE	COG2IE(1)	CLC3IE	CLC2IE	CLC1IE	104
PIR3	PWM6IF(1)	PWM5IF	COG1IF	ZCDIF	COG2IF(1)	CLC3IF	CLC2IF	CLC1IF	107
RxyPPS	—	—	—	RxyPPS<4:0>					154
TRISA	—	—	TRISA<5:4>		—(3)	TRISA<2:0>			136
TRISB(1)	TRISB<7:4>				—	—	—	—	142
TRISC	TRISC<7:6>(1)		TRISC<5:0>						147

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for CLCx module.

Note 1: PIC16(L)F1768/9 only.

2: Unimplemented, read as '1'.

31.0 DATA SIGNAL MODULATOR (DSM)

The Data Signal Modulator (DSM) is a peripheral that allows the user to mix a data stream, also known as a modulator signal, with a carrier signal to produce a modulated output.

Both the carrier and the modulator signals are supplied to the DSM module either internally, from the output of a peripheral, or externally through an input pin.

The modulated output signal is generated by performing a logical “AND” operation of both the carrier and modulator signals and then provided to the MDxOUT pin.

The carrier signal is comprised of two distinct and separate signals: a Carrier High (CARH) signal and a Carrier Low (CARL) signal. During the time in which the Modulator (MOD) signal is in a logic high state, the DSM mixes the Carrier High signal with the Modulator signal. When the Modulator signal is in a logic low state, the DSM mixes the Carrier Low signal with the Modulator signal.

Using this method, the DSM can generate the following types of key modulation schemes:

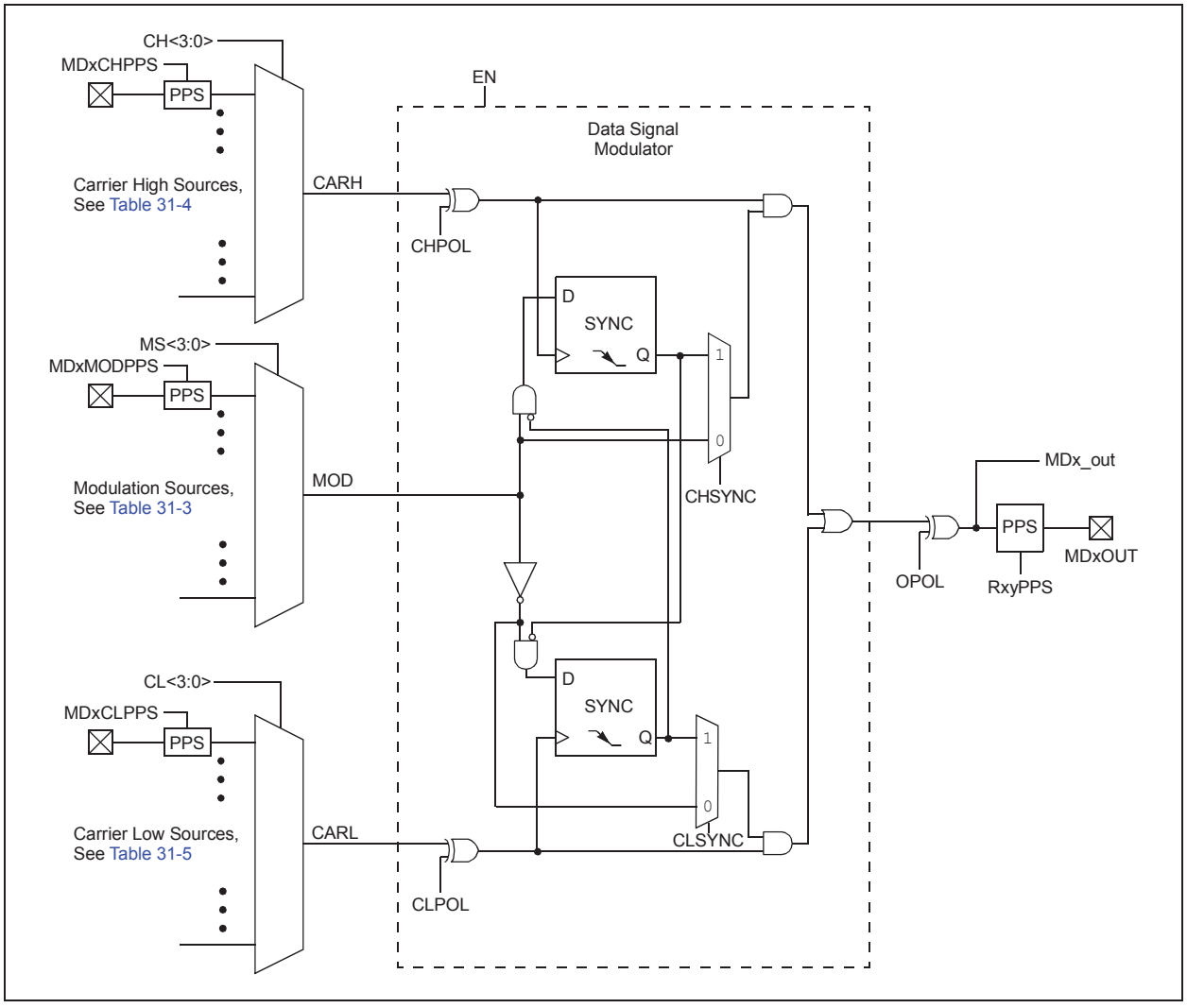
- Frequency-Shift Keying (FSK)
- Phase-Shift Keying (PSK)
- On-Off Keying (OOK)

Additionally, the following features are provided within the DSM module:

- Carrier Synchronization
- Carrier Source Polarity Select
- Carrier Source Pin Disable
- Programmable Modulator Data
- Modulator Source Pin Disable
- Modulated Output Polarity Select
- Slew Rate Control

Figure 31-1 shows a simplified block diagram of the Data Signal Modulator peripheral.

FIGURE 31-1: SIMPLIFIED BLOCK DIAGRAM OF THE DATA SIGNAL MODULATOR



32.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

TABLE 32-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA<2:0>			137
ANSELC	ANSC<7:6>(2)		—	—	ANSC<3:0>				148
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	101
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	102
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	105
RxyPPS	—	—	—	RxyPPS<4:0>					154
SSPCLKPPS	—	—	—	SSPCLKPPS<4:0>					154, 156
SSPDATPPS	—	—	—	SSPDATPPS<4:0>					154, 156
SSPSSPPS	—	—	—	SSPSSPPS<4:0>					154, 156
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								380*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				426
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	424
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	424
TRISA	—	—	TRISA<5:4>		—(1)	TRISA<2:0>			136
TRISB(2)	TRISB<7:4>				—	—	—	—	142
TRISC	TRISC<7:6>(2)		TRISC<5:0>						147

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

* Page provides register information.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1768/9 only.

33.3 Register Definitions: EUSART Control

REGISTER 33-1: TX1STA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	
u = Bit is unchanged	x = Bit is unknown	U = Unimplemented bit, read as '0'
'1' = Bit is set	'0' = Bit is cleared	-n/n = Value at POR and BOR/Value at all other Resets

bit 7 **CSRC:** Clock Source Select bit

Asynchronous mode:
Don't care.

Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-Bit Transmit Enable bit

1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)

1 = Transmit is enabled
0 = Transmit is disabled

bit 4 **SYNC:** EUSART Mode Select bit

1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit

Asynchronous mode:
1 = Sends Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission has completed

Synchronous mode:
Don't care.

bit 2 **BRGH:** High Baud Rate Select bit

Asynchronous mode:
1 = High speed
0 = Low speed

Synchronous mode:
Unused in this mode.

bit 1 **TRMT:** Transmit Shift Register Status bit

1 = TSR is empty
0 = TSR is full

bit 0 **TX9D:** Ninth bit of Transmit Data

Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

36.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \leq V_{DD} \leq V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \leq T_A \leq T_{A\_MAX}$

V_{DD} – Operating Supply Voltage(1)

PIC16LF1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +1.8V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +3.6V

PIC16F1764/5/8/9

V_{DDMIN} ($F_{OSC} \leq 16$ MHz) ..... +2.3V
V_{DDMIN} ($F_{OSC} > 16$ MHz) ..... +2.5V
V_{DDMAX} ..... +5.5V

T_A – Operating Ambient Temperature Range

Industrial Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +85°C

Extended Temperature

T_{A_MIN} ..... -40°C
T_{A_MAX} ..... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

TABLE 36-8: OSCILLATOR PARAMETERS

Standard Operating Conditions (unless otherwise stated)								
Param No.	Sym.	Characteristic	Freq. Tolerance	Min.	Typ†	Max.	Units	Conditions
OS08	HFOSC	Internal Calibrated HFINTOSC Frequency(1)	±2%	—	16.0	—	MHz	VDD = 3.0V, TA = 25°C **(Note 2)**
OS08A	MFOSC	Internal Calibrated MFINTOSC Frequency(1)	±2%	—	500	—	kHz	VDD = 3.0V, TA = 25°C **(Note 3)**
OS09	LFOSC	Internal LFINTOSC Frequency	—	—	31	—	kHz	-40°C ≤ TA ≤ +125°C
OS10*	TWARM	HFINTOSC Wake-up from Sleep Start-up Time	—	—	3.2	8	µs	
		MFINTOSC Wake-up from Sleep Start-up Time	—	—	24	35	µs	
		LFINTOSC Wake-up from Sleep Start-up Time	—	—	0.5	—	ms	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, +25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

2: See Figure 37-74: Wake From Sleep, VREGPM = 0. and Figure 37-75: Wake From Sleep, VREGPM = 1.

3: See Figure 37-57: LFINTOSC Frequency, PIC16LF1764/5/8/9 Only. and Figure 37-58: LFINTOSC Frequency, PIC16F1764/5/8/9 Only.

FIGURE 36-6: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE

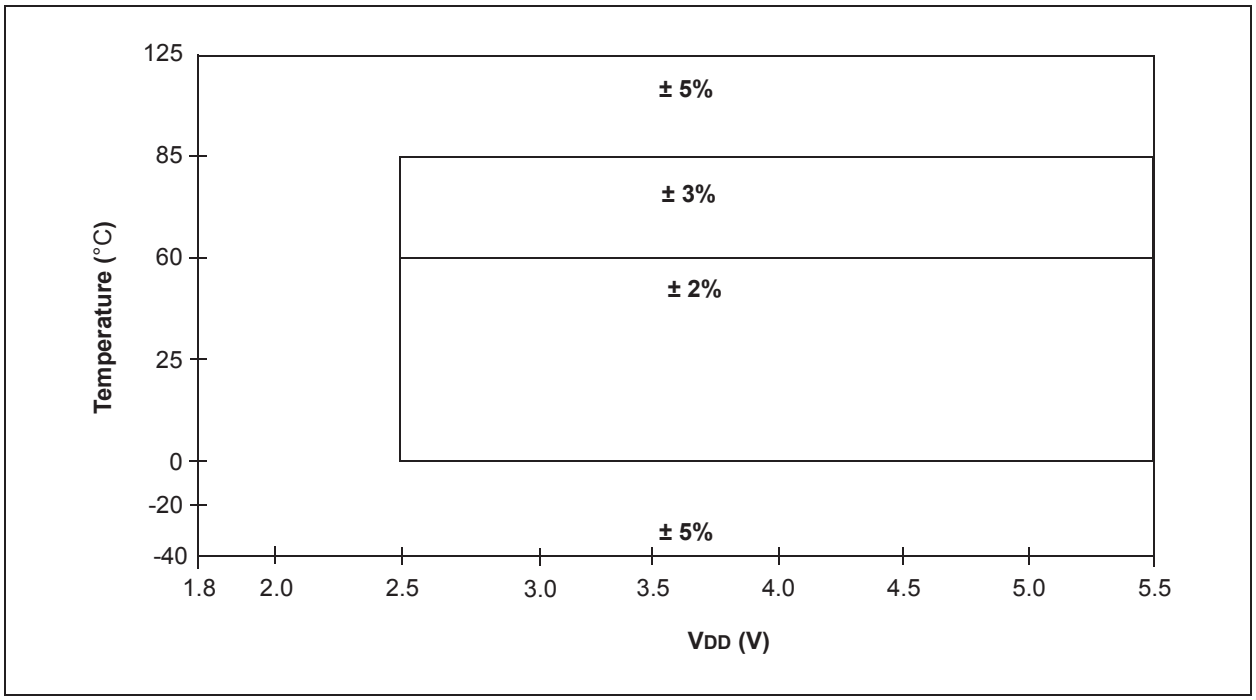


TABLE 36-27: I²C BUS DATA REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
SP100*	THIGH	Clock High Time	100 kHz mode	4.0	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	1.5 TCY	—	TCY	
SP101*	TLOW	Clock Low Time	100 kHz mode	4.7	—	µs	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	µs	Device must operate at a minimum of 10 MHz
			SSP module	1.5 TCY	—	TCY	
SP102*	TR	SDA and SCL Rise Time	100 kHz mode	—	1000	ns	
			400 kHz mode	20 + 0.1 CB	300	ns	CB is specified to be from 10-400 pF
SP103*	TF	SDA and SCL Fall Time	100 kHz mode	—	250	ns	
			400 kHz mode	20 + 0.1 CB	250	ns	CB is specified to be from 10-400 pF
SP106*	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	ns	
			400 kHz mode	0	0.9	µs	
SP107*	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	**(Note 2)**
			400 kHz mode	100	—	ns	
SP109*	TAA	Output Valid from Clock	100 kHz mode	—	3500	ns	**(Note 1)**
			400 kHz mode	—	—	ns	
SP110*	TBUF	Bus Free Time	100 kHz mode	4.7	—	µs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	µs	
SP111	CB	Bus Capacitive Loading		—	400	pF	

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement, TSU:DAT ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line, TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

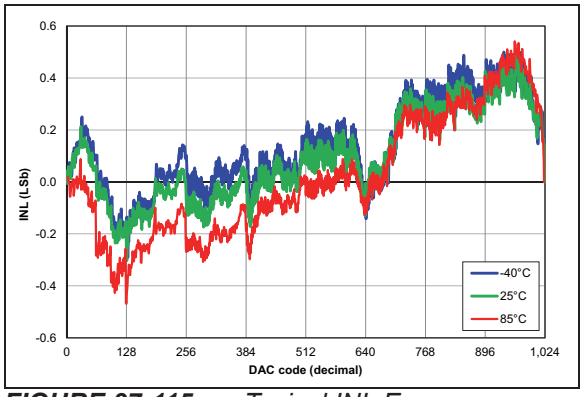


FIGURE 37-115: *Typical INL Error, VDD = 3.6V, VREF = VDD.*

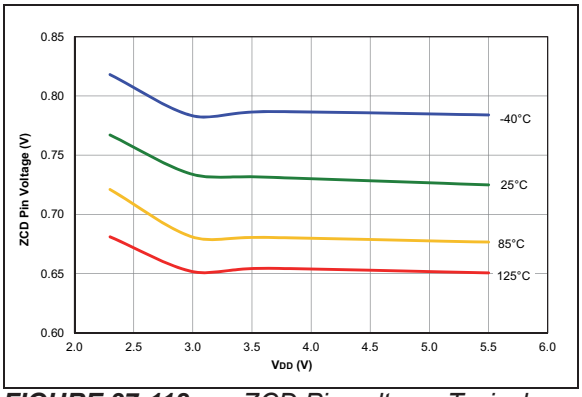


FIGURE 37-118: *ZCD Pin voltage, Typical Measured Values.*

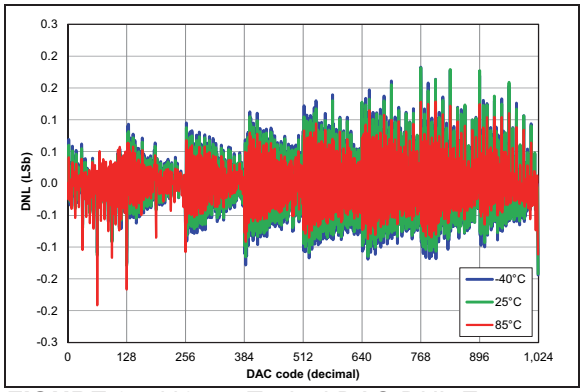


FIGURE 37-116: *Typical DAC DNL Error, VDD = 5.0V, VREF = VDD, PIC16F1764/5/8/9 Only.*

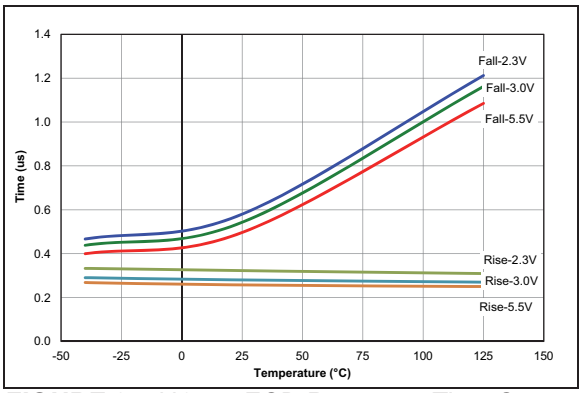


FIGURE 37-119: *ZCD Response Time Over Voltage, Typical Measured Values.*

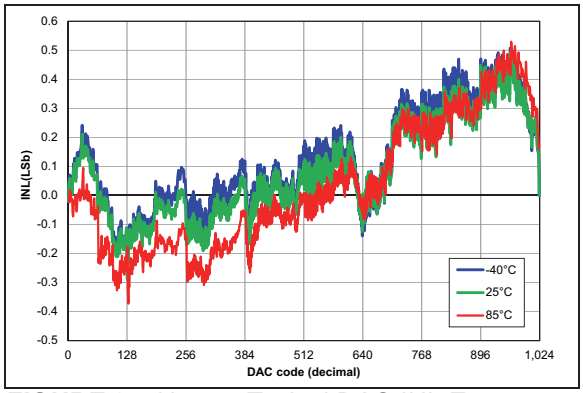
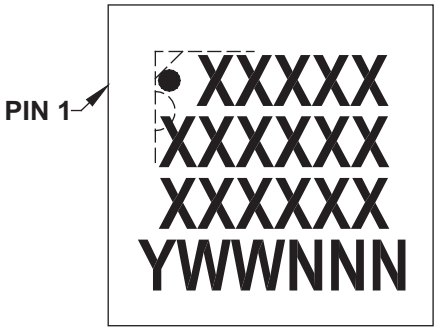


FIGURE 37-117: *Typical DAC INL Error, VDD = 5.0V, VREF = VDD, PIC16F1764/5/8/9 Only.*

Package Marking Information (Continued)

20-Lead QFN (4x4x0.9 mm)



Example