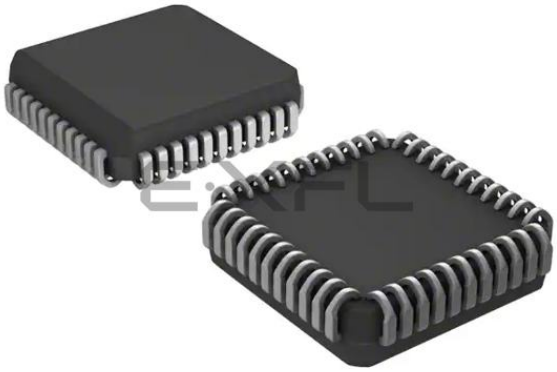

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Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705c9acfne

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2.4 EPROM Security

A security feature has been incorporated into the MC68HC705C9A to help prevent external access to the contents of the EPROM in any mode of operation. Once enabled, this feature can be disabled only by completely erasing the EPROM.

NOTE

For OTP (plastic) packages, once the security feature has been enabled, it cannot be disabled.

2.5 ROM

The bootloader ROM occupies 239 bytes in the memory space from $3F00 to $3FEF. The bootloader mode provides for self-programming of the EPROM array. See Appendix A EPROM Programming.

2.6 I/O Registers

Except for the option register, mask option registers, and the C12 COP clear register, all I/O, control and status registers are located within one 32-byte block in page zero of the address space ($0000–$001F). A summary of these registers is shown in Figure 2-3. More detail about the contents of these registers is given Figure 2-4.

Table 4-1. Vector Addresses for Interrupts and Resets

Function	Source	Local Mask	Global Mask	Priority (1 = Highest)	Vector Address
Reset	Power-on reset	None	None	1	$3FFE–$3FFF
	$\overline{\text{RESET}}$ pin				
	COP watchdog				
Software interrupt (SWI)	User code	None	None	Same priority as instruction	$3FFC–$3FFD
External interrupt	$\overline{\text{IRQ}}$ pin port B pins	None	I bit	2	$3FFA–$3FFB
Timer interrupts	ICF bit	ICIE bit	I bit	3	$3FF8–$3FF9
	OCF bit	OCIE bit			
	TOF bit	TOIE bit			
SCI interrupts	TDRE bit	TCIE bit	I bit	4	$3FF6–$3FF7
	TC bit				
	RDRF bit	RIE bit			
	OR bit				
	IDLE bit	ILIE bit			
SPI interrupts	SPIF bit	SPIE	I bit	5	$3FF4–$3FF5
	MODF bit				

4.3 External Interrupt ($\overline{\text{IRQ}}$ or Port B)

If the interrupt mask bit (I bit) of the CCR is set, all maskable interrupts (internal and external) are disabled. Clearing the I bit enables interrupts. The interrupt request is latched immediately following the falling edge of $\overline{\text{IRQ}}$. It is then synchronized internally and serviced as specified by the contents of $3FFA and $3FFB.

When any of the port B pullups are enabled, each pin becomes an additional external interrupt source which is executed identically to the $\overline{\text{IRQ}}$ pin. Port B interrupts follow the same edge/edge-level selection as the $\overline{\text{IRQ}}$ pin. The branch instructions BIL and BIH also respond to the port B interrupts in the same way as the $\overline{\text{IRQ}}$ pin. See 7.3 Port B.

Either a level-sensitive and edge-sensitive trigger or an edge-sensitive-only trigger operation is selectable. In MC68HC05C9A mode, the sensitivity is software controlled by the IRQ bit in the C9A option register ($3FDF). In the MC68HC05C12A mode, the sensitivity is determined by the C12IRQ bit in the C12 mask option register ($3FF1).

NOTE

The internal interrupt latch is cleared in the first part of the interrupt service routine; therefore, one external interrupt pulse can be latched and serviced as soon as the I bit is cleared.

5.5 MC68HC05C9A Compatible COP

This COP is controlled with two registers; one to reset the COP timer and the other to enable and control COP and clock monitor functions. Figure 5-3 shows a block diagram of the MC68HC05C9A COP.

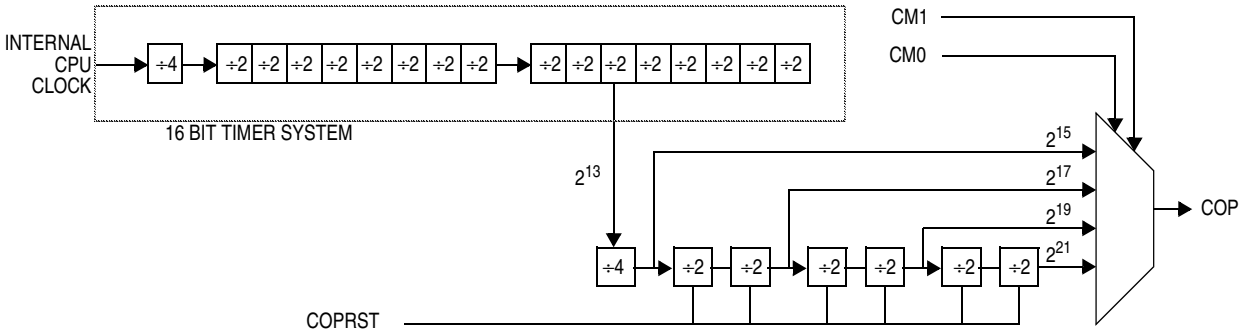


Figure 5-3. C9A COP Block Diagram

5.5.1 C9A COP Reset Register

This write-only register, shown in Figure 5-4, is used to reset the COP.

$001D	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 5-4. COP Reset Register (COPRST)

The sequence required to reset the COP timer is:

- Write $55 to the COP reset register
- Write $AA to the COP reset register

Both write operations must occur in the order listed, but any number of instructions may be executed between the two write operations provided that the COP does not time out between the two writes. The elapsed time between software resets must not be greater than the COP timeout period. If the COP should time out, a system reset will occur and the device will be re-initialized in the same fashion as a power-on reset or reset.

Reading this register does not return valid data.

5.5.2 C9A COP Control Register

The COP control register, shown in Figure 5-5, performs these functions:

- Enables clock monitor function
- Enables MC68HC05C9A compatible COP function
- Selects timeout duration of COP timer

and flags the following conditions:

- A COP timeout
- Clock monitor reset

8.2 Timer Operation

The core of the capture/compare timer is a 16-bit free-running counter. The counter provides the timing reference for the input capture and output compare functions. The input capture and output compare functions provide a means to latch the times at which external events occur, to measure input waveforms, and to generate output waveforms and timing delays. Software can read the value in the 16-bit free-running counter at any time without affecting the counter sequence.

Because of the 16-bit timer architecture, the I/O registers for the input capture and output compare functions are pairs of 8-bit registers.

Because the counter is 16 bits long and preceded by a fixed divide-by-4 prescaler, the counter rolls over every 262,144 internal clock cycles. Timer resolution with a 4-MHz crystal is 2 μs.

8.2.1 Input Capture

The input capture function is a means to record the time at which an external event occurs. When the input capture circuitry detects an active edge on the TCAP pin, it latches the contents of the timer registers into the input capture registers. The polarity of the active edge is programmable.

Latching values into the input capture registers at successive edges of the same polarity measures the period of the input signal on the TCAP pin. Latching values into the input capture registers at successive edges of opposite polarity measures the pulse width of the signal.

8.2.2 Output Compare

The output compare function is a means of generating an output signal when the 16-bit counter reaches a selected value. Software writes the selected value into the output compare registers. On every fourth internal clock cycle the output compare circuitry compares the value of the counter to the value written in the output compare registers. When a match occurs, the timer transfers the programmable output level bit (OLVL) from the timer control register to the TCMP pin.

The programmer can use the output compare register to measure time periods, to generate timing delays, or to generate a pulse of specific duration or a pulse train of specific frequency and duty cycle on the TCMP pin.

8.3 Timer I/O Registers

The following I/O registers control and monitor timer operation:

- Timer control register (TCR)
- Timer status register (TSR)
- Timer registers (TRH and TRL)
- Alternate timer registers (ATRH and ATRL)
- Input capture registers (ICRH and ICRL)
- Output compare registers (OCRH and OCRL)

8.3.3 Timer Registers

The timer registers (TRH and TRL), shown in Figure 8-4, contains the current high and low bytes of the 16-bit counter. Reading TRH before reading TRL causes TRL to be latched until TRL is read. Reading TRL after reading the timer status register clears the timer overflow flag (TOF). Writing to the timer registers has no effect.

TRH $0018	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write								
Reset:	1	1	1	1	1	1	1	1

TRL $0019	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	1	1	1	1	1	1	0	0

= Unimplemented

Figure 8-4. Timer Registers (TRH and TRL)

8.3.4 Alternate Timer Registers

The alternate timer registers (ATRH and ATRL), shown in Figure 8-5, contain the current high and low bytes of the 16-bit counter. Reading ATRH before reading ATRL causes ATRL to be latched until ATRL is read. Reading ATRL has no effect on the timer overflow flag (TOF). Writing to the alternate timer registers has no effect.

ATRH $001A	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	1	1	1	1	1	1	1	1

ATRL $001B	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	1	1	1	1	1	1	0	0

= Unimplemented

Figure 8-5. Alternate Timer Registers (ATRH and ATRL)

NOTE

To prevent interrupts from occurring between readings of ATRH and ATRL, set the interrupt flag in the condition code register before reading ATRH, and clear the flag after reading ATRL.

8.3.5 Input Capture Registers

When a selected edge occurs on the TCAP pin, the current high and low bytes of the 16-bit counter are latched into the input capture registers (ICRH and ICRL). Reading ICRH before reading ICRL inhibits further capture until ICRL is read. Reading ICRL after reading the status register clears the input capture flag (ICF). Writing to the input capture registers has no effect.

ICRH $0014	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:								
Reset:	Unaffected by reset							

ICRL $0015	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							

= Unimplemented

Figure 8-6. Input Capture Registers (ICRH and ICRL)

NOTE

To prevent interrupts from occurring between readings of ICRH and ICRL, set the interrupt flag in the condition code register before reading ICRH, and clear the flag after reading ICRL.

8.3.6 Output Compare Registers

When the value of the 16-bit counter matches the value in the output compare registers (OCRH and OCRL), the planned TCMP pin action takes place. Writing to OCRH before writing to OCRL inhibits timer compares until OCRL is written. Reading or writing to OCRL after the timer status register clears the output compare flag (OCF).

OCRH $0016	Bit 7	6	5	4	3	2	1	Bit 0
Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Read:								
Reset:	Unaffected by reset							

OCRL $0017	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:								
Reset:	Unaffected by reset							

Figure 8-7. Output Compare Registers (OCRH and OCRL)

9.9 Address Mark Wakeup

In address mark wakeup, the most significant bit (MSB) in a character is used to indicate whether it is an address (logic 1) or data (logic 0) character. Sleeping receivers will wake up whenever an address character is received. Systems using this method for wakeup would set the MSB of the first character of each message and leave it clear for all other characters in the message. Idle periods may be present within messages and no idle time is required between messages for this wakeup method.

9.10 Receive Data In (RDI)

Receive data is the serial data that is applied through the input line and the SCI to the internal bus. The receiver circuitry clocks the input at a rate equal to 16 times the baud rate. This time is referred to as the RT rate in Figure 9-4 and as the receiver clock in Figure 9-6.

The receiver clock generator is controlled by the baud rate register; however, the SCI is synchronized by the start bit, independent of the transmitter.

Once a valid start bit is detected, the start bit, each data bit, and the stop bit are sampled three times at RT intervals 8 RT, 9 RT, and 10 RT
(1 RT is the position where the bit is expected to start), as shown in Figure 9-5. The value of the bit is determined by voting logic which takes the value of the majority of the samples. A noise flag is set when all three samples on a valid start bit or data bit or the stop bit do not agree.

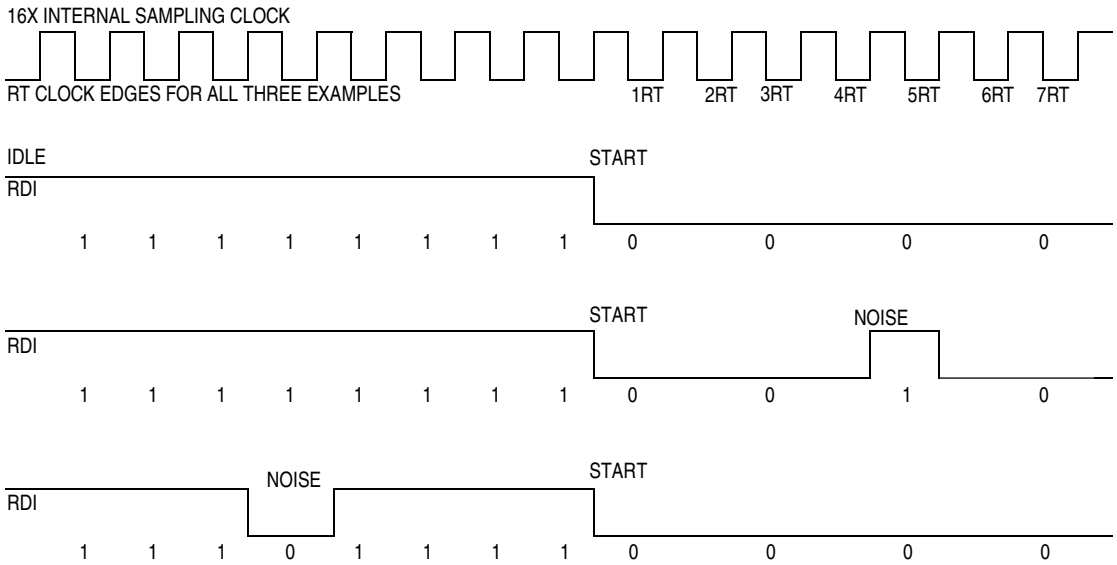


Figure 9-4. SCI Examples of Start Bit Sampling Techniques

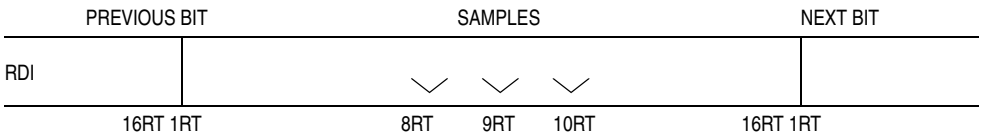


Figure 9-5. SCI Sampling Technique Used on All Bits

The SPI is double buffered on read, but not on write. If a write is performed during data transfer, the transfer occurs uninterrupted, and the write will be unsuccessful. This condition will cause the write collision (WCOL) status bit in the SPSR to be set. After a data byte is shifted, the SPIF flag of the SPSR is set.

In the master mode, the SCK pin is an output. It idles high or low, depending on the CPOL bit in the SPCR, until data is written to the shift register, at which point eight clocks are generated to shift the eight bits of data and then SCK goes idle again.

In a slave mode, the slave select start logic receives a logic low at the $\overline{SS}$ pin and a clock at the SCK pin. Thus, the slave is synchronized with the master. Data from the master is received serially at the MOSI line and loads the 8-bit shift register. After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer. During a write cycle, data is written into the shift register, then the slave waits for a clock train from the master to shift the data out on the slave's MISO line.

Figure 10-3 illustrates the MOSI, MISO, SCK, and $\overline{SS}$ master-slave interconnections.

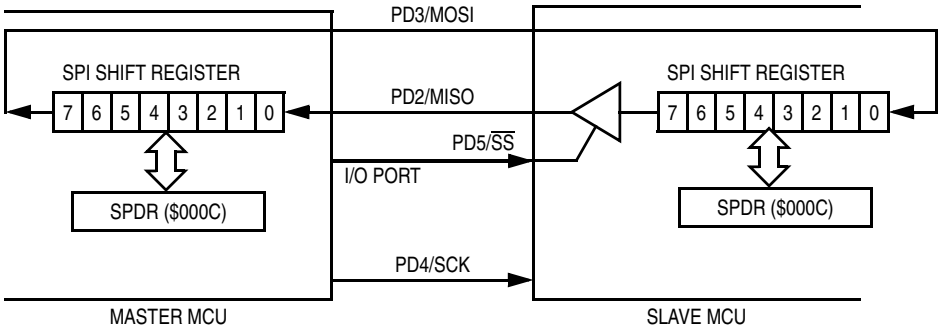


Figure 10-3. Serial Peripheral Interface Master-Slave Interconnection

10.5 SPI Registers

Three registers in the SPI provide control, status, and data storage functions. These registers are called the serial peripheral control register (SPCR), serial peripheral status register (SPSR), and serial peripheral data I/O register (SPDR) and are described in the following paragraphs.

10.5.1 Serial Peripheral Control Register

The SPI control register (SPCR), shown in Figure 10-4, controls these functions:

- Enables SPI interrupts
- Enables the SPI system
- Selects between standard CMOS or open drain outputs for port D (C9A mode only)
- Selects between master mode and slave mode
- Controls the clock/data relationship between master and slave
- Determines the idle level of the clock pin

Clearing the MODF bit is accomplished by reading the SPSR (with MODF set), followed by a write to the SPCR. Control bits SPE and MSTR may be restored by user software to their original state during this clearing sequence or after the MODF bit has been cleared. When configured as an MC68HC05C9A, it is also necessary to restore DDRD after a mode fault.

Bits 5 and 3–0 — Not Implemented

These bits always read 0.

10.5.3 Serial Peripheral Data I/O Register

The serial peripheral data I/O register (SPDR), shown in Figure 10-6, is used to transmit and receive data on the serial bus. Only a write to this register will initiate transmission/reception of another byte and this will only occur in the master device. At the completion of transmitting a byte of data, the SPIF status bit is set in both the master and slave devices.

When the user reads the serial peripheral data I/O register, a buffer is actually being read. The first SPIF must be cleared by the time a second transfer of the data from the shift register to the read buffer is initiated or an overrun condition will exist. In cases of overrun, the byte which causes the overrun is lost.

A write to the serial peripheral data I/O register is not buffered and places data directly into the shift register for transmission.

$000C	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Reset:	Unaffected by reset							

Figure 10-6. PI Data Register (SPDR)

11.4 Instruction Set Summary

Table 11-6. Instruction Set Summary (Sheet 1 of 6)

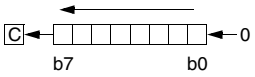
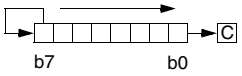
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AN*D opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BIH *rel*	Branch if IRQ Pin High	PC ← (PC) + 2 + *rel* ? IRQ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	PC ← (PC) + 2 + *rel* ? IRQ = 0	—	—	—	—	—	REL	2E	rr	3

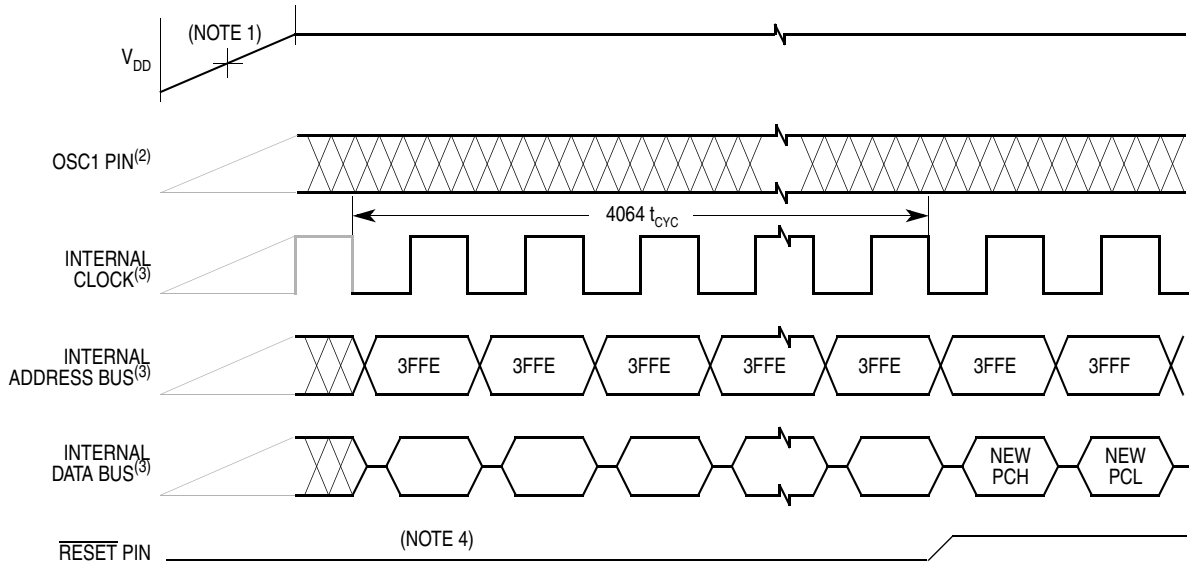
Table 11-6. Instruction Set Summary (Sheet 6 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
TXA	Transfer Index Register to Accumulator	A ← (X)	—	—	—	—	—	INH	9F		2
WAIT	Stop CPU Clock and Enable Interrupts		—	0	—	—	—	INH	8F		2

A	Accumulator	*opr*	Operand (one or two bytes)
C	Carry/borrow flag	PC	Program counter
CCR	Condition code register	PCH	Program counter high byte
dd	Direct address of operand	PCL	Program counter low byte
dd rr	Direct address of operand and relative offset of branch instruction	REL	Relative addressing mode
DIR	Direct addressing mode	*rel*	Relative program counter offset byte
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing	rr	Relative program counter offset byte
EXT	Extended addressing mode	SP	Stack pointer
ff	Offset byte in indexed, 8-bit offset addressing	X	Index register
H	Half-carry flag	Z	Zero flag
hh ll	High and low bytes of operand address in extended addressing	#	Immediate value
I	Interrupt mask	∧	Logical AND
ii	Immediate operand byte	∨	Logical OR
IMM	Immediate addressing mode	⊕	Logical EXCLUSIVE OR
INH	Inherent addressing mode	( )	Contents of
IX	Indexed, no offset addressing mode	–( )	Negation (two's complement)
IX1	Indexed, 8-bit offset addressing mode	←	Loaded with
IX2	Indexed, 16-bit offset addressing mode	?	If
M	Memory location	:	Concatenated with
N	Negative flag	↕	Set or cleared
n	Any bit	—	Not affected

11.5 Opcode Map

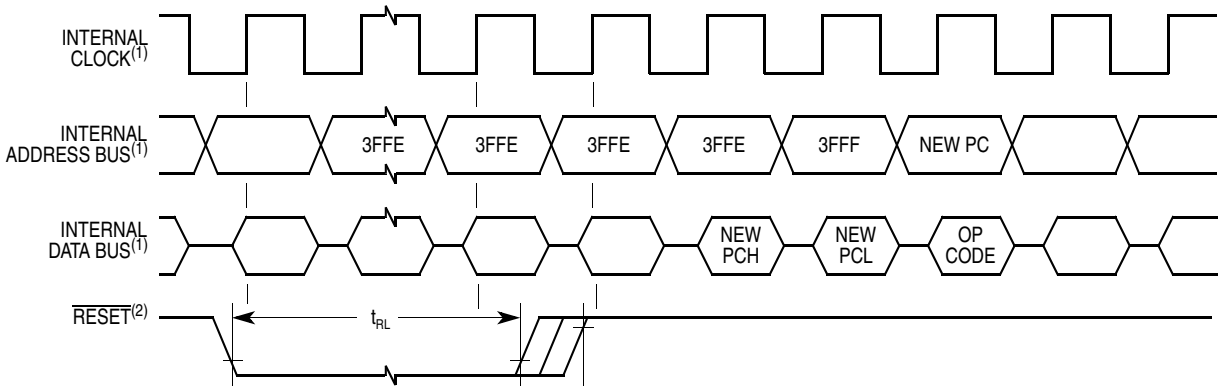
See Table 11-7.



Notes:

1. Power-on reset threshold is typically between 1 V and 2 V.
2. OSC1 line is meant to represent time only, not frequency.
3. Internal clock, internal address bus, and internal data bus are not available externally.
4. $\overline{\text{RESET}}$ outputs V_{OL} during 4064 POR cycles.

Figure 12-7. Power-On Reset Timing Diagram



Notes:

1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 12-8. External Reset Timing

Appendix B
M68HC05Cx Family Feature Comparisons

Refer to Table B-1 for a comparison of the features for all the M68HC05C Family members.