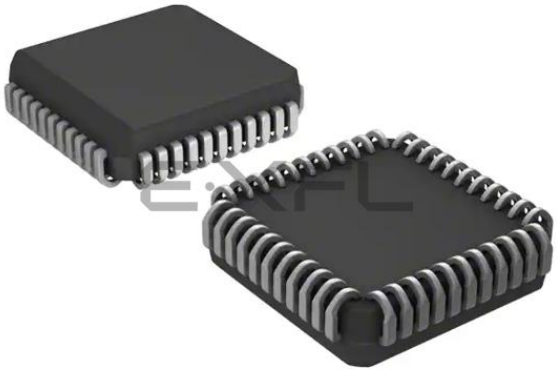

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705c9afne

1.5 Software-Programmable Options (MC68HC05C9A Mode Only)

The C9A option register (OR), shown in Figure 1-4, is enabled only if configured in C9A mode. This register contains the programmable bits for the following options:

- Map two different areas of memory between RAM and EPROM, one of 48 bytes and one of 128 bytes
- Edge-triggered only or edge- and level-triggered external interrupt ($\overline{\text{IRQ}}$ pin and any port B pin configured for interrupt)

This register must be written to by user software during operation of the microcontroller.

$3FDF	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	RAM0	RAM1					IRQ	
Reset:	0	0	0	0	0	0	1	0

= Unimplemented

Figure 1-4. C9A Option Register

RAM0 — Random Access Memory Control Bit 0

This read/write bit selects between RAM or EPROM in location $0020 to $004F. This bit can be read or written at any time.

1 = RAM selected
0 = EPROM selected

RAM1— Random Access Memory Control Bit 1

This read/write bit selects between RAM or EPROM in location $0100 to $017F. This bit can be read or written at any time.

1 = RAM selected
0 = EPROM selected

IRQ — Interrupt Request Bit

This bit selects between an edge-triggered only or edge- and level- triggered external interrupt pin. This bit is set by reset, but can be cleared by software. This bit can be written only once.

1 = Edge and level interrupt option selected
0 = Edge-only interrupt option selected

1.6.5 $\overline{\text{RESET}}$

As an input pin, this active low $\overline{\text{RESET}}$ pin is used to reset the MCU to a known startup state by pulling $\overline{\text{RESET}}$ low. As an output pin, when in MC68HC05C9A mode only, the $\overline{\text{RESET}}$ pin indicates that an internal MCU reset has occurred. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to
Chapter 5 Resets for more detail.

1.6.6 TCAP

This pin controls the input capture feature for the on-chip programmable timer. The TCAP pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to Chapter 8 Capture/Compare Timer for more detail.

1.6.7 TCMP

The TCMP pin provides an output for the output compare feature of the on-chip programmable timer. Refer to Chapter 8 Capture/Compare Timer for more detail.

1.6.8 PA0–PA7

These eight I/O lines comprise port A. The state of each pin is software programmable and all port A pins are configured as inputs during reset. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.9 PB0–PB7

These eight I/O lines comprise port B. The state of each pin is software programmable and all port B pins are configured as inputs during reset. Port B has mask option register enabled pullup devices and interrupt capability selectable for any pin. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.10 PC0–PC7

These eight I/O lines comprise port C. The state of each pin is software programmable and all port C pins are configured as inputs during reset. PC7 has high current sink and source capability. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.11 PD0–PD5 and PD7

These seven I/O lines comprise port D. When configured as a C9A the state of each pin is software programmable and all port D pins are configured as inputs during reset. When configured as a C12A, the port D pins are input only. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

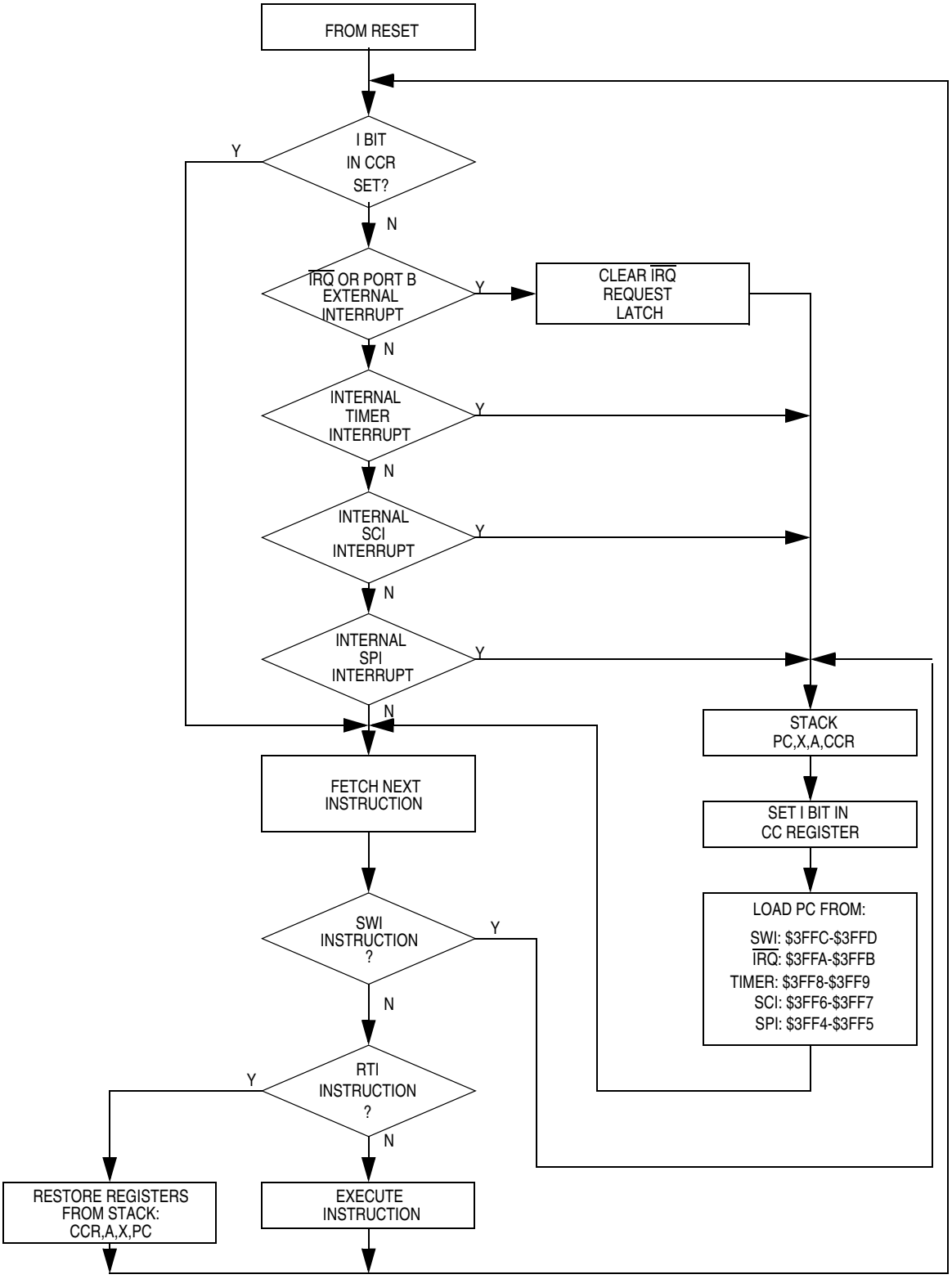


Figure 4-1. Interrupt Flowchart

4.4 Timer Interrupt

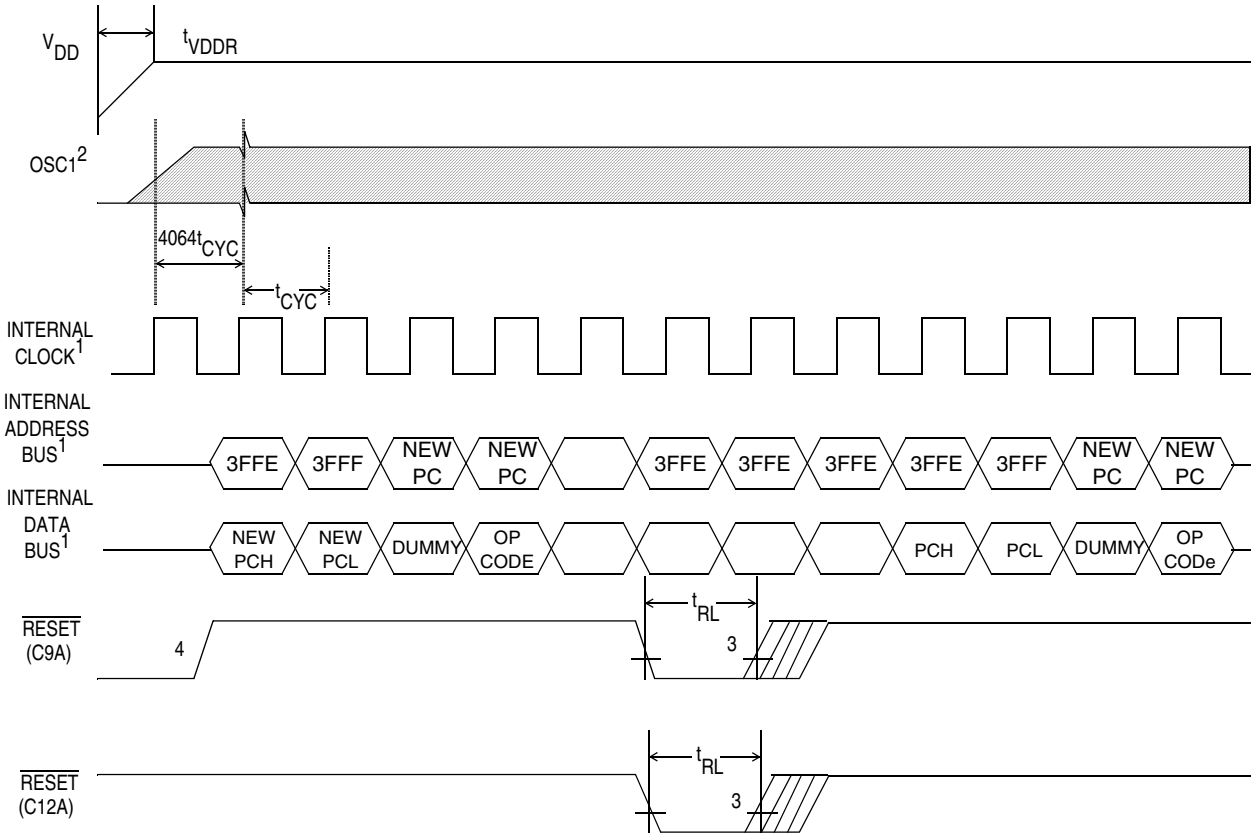
Three different timer interrupt flags cause a timer interrupt whenever they are set and enabled. The interrupt flags are in the timer status register (TSR), and the enable bits are in the timer control register (TCR). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF8 and $3FF9.

4.5 SCI Interrupt

Five different SCI interrupt flags cause an SCI interrupt whenever they are set and enabled. The interrupt flags are in the SCI status register (SCSR), and the enable bits are in the SCI control register 2 (SCCR2). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF6 and $3FF7.

4.6 SPI Interrupt

Two different SPI interrupt flags cause an SPI interrupt whenever they are set and enabled. The interrupt flags are in the SPI status register (SPSR), and the enable bits are in the SPI control register (SPCR). Either of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF4 and $3FF5.



Notes:
1. Internal timing signal and bus information are not available externally.
2. OSC1 line is not meant to represent frequency. It is only meant to represent time.
3. The next rising edge of the internal processor clock following the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.
4. $\overline{\text{RESET}}$ outputs V_{OL} during 4064 power-on reset cycles when in C9A mode only.

Figure 5-2. Power-On Reset and $\overline{\text{RESET}}$

5.4 Computer Operating Properly (COP) Reset

This device includes a watchdog COP feature which guards against program run-away failures. A timeout of the computer operating properly (COP) timer generates a COP reset. The COP watchdog is a software error detection system that automatically times out and resets the MCU if not cleared periodically by a program sequence.

This device includes two COP types, one for C12A compatibility and the other for C9A compatibility. When configured as a C9A the COP can be enabled by user software by setting COPE in the C9A COP control register (C9ACOPCR). When configured as a C12A, the COP is enabled prior to operation by programming the C12COPE bit in the C12A mask option register (C12MOR). The function and control of both COPs is detailed below.

Chapter 7
Input/Output (I/O) Ports

7.1 Introduction

This section briefly describes the 31 input/output (I/O) lines arranged as one 7-bit and three 8-bit ports. All of these port pins are programmable as either inputs or outputs under software control of the data direction registers.

NOTE

To avoid a glitch on the output pins, write data to the I/O port data register before writing a one to the corresponding data direction register.

7.2 Port A

Port A is an 8-bit bidirectional port which does not share any of its pins with other subsystems. The port A data register is at $0000 and the data direction register (DDR) is at $0004. The contents of the port A data register are indeterminate at initial powerup and must be initialized by user software. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a 1 to a DDR bit sets the corresponding port bit to output mode. A block diagram of the port logic is shown in Figure 7-1.

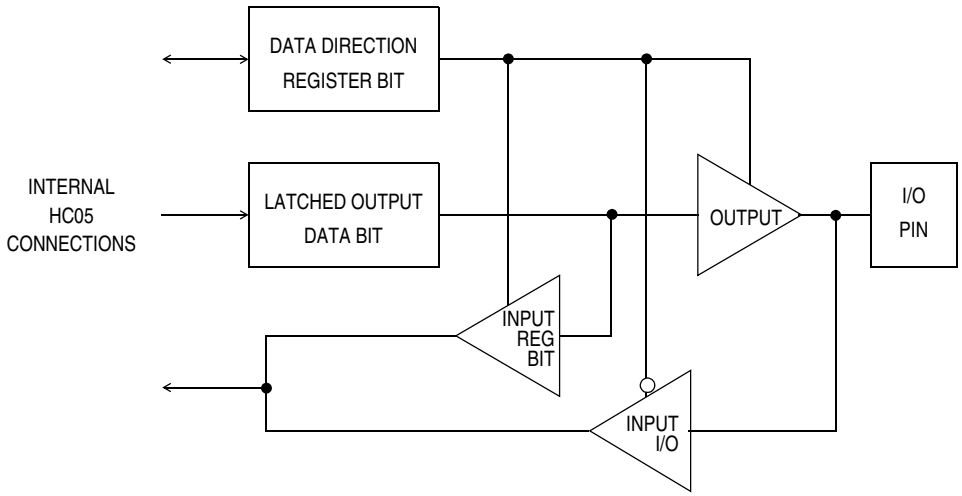


Figure 7-1. Port A I/O Circuit

7.3 Port B

Port B is an 8-bit bidirectional port. The port B data register is at $0001 and the data direction register (DDR) is at $0005. The contents of the port B data register are indeterminate at initial powerup and must be initialized by user software. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a 1 to a DDR bit sets the corresponding port pin to output mode. Each of the port B pins has an optional external interrupt capability that can be enabled by programming the corresponding bit in the port B mask option register ($3FF0).

The interrupt option also enables a pullup device when the pin is configured as an input. The edge or edge- and level-sensitivity of the $\overline{\text{IRQ}}$ pin will also pertain to the enabled port B pins. Care needs to be taken when using port B pins that have the pullup enabled. Before switching from an output to an input, the data should be preconditioned to a 1 to prevent an interrupt from occurring. The port B logic is shown in Figure 7-2.

7.4 Port C

Port C is an 8-bit bidirectional port. The port C data register is at $0002 and the data direction register (DDR) is at $0006. The contents of the port C data register are indeterminate at initial powerup and must be initialized by user software. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a 1 to a DDR bit sets the corresponding port bit to output mode. PC7 has a high current sink and source capability. Figure 7-1 is also applicable to port C.

7.5 Port D

When configured as a C9A, port D is a 7-bit bidirectional port; when configured as a C12A, port D is a 7-bit fixed input port. Four of its pins are shared with the SPI subsystem and two more are shared with the SCI subsystem. The contents of the port D data register are indeterminate at initial powerup and must be initialized by user software. During reset all seven bits become valid input ports because the C9A DDR bits are cleared and the special function output drivers associated with the SCI and SPI subsystems are disabled, thereby returning the ports to inputs. Writing a 1 to a DDR bit sets the corresponding port bit to output mode only when configured as a C9A.

Chapter 9
Serial Communications Interface (SCI)

9.1 Introduction

This section describes the on-chip asynchronous serial communications interface (SCI). The SCI allows full-duplex, asynchronous, RS232 or RS422 serial communication between the MCU and remote devices, including other MCUs. The transmitter and receiver of the SCI operate independently, although they use the same baud rate generator.

9.2 Features

Features of the SCI include:

- Standard mark/space non-return-to-zero format
- Full-duplex operation
- 32 programmable baud rates
- Programmable 8-bit or 9-bit character length
- Separately enabled transmitter and receiver
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation capability with five interrupt flags:
  - Transmitter data register empty
  - Transmission complete
  - Transmission data register full
  - Receiver overrun
  - Idle receiver input
- Receiver framing error detection
- 1/16 bit-time noise detection

9.3 SCI Receiver Features

Features of the SCI receiver include:

- Receiver wakeup function (idle line or address bit)
- Idle line detection
- Framing error detection
- Noise detection
- Overrun detection
- Receiver data register full flag

T8 — Bit 8 (Transmitted)

When the SCI is transmitting 9-bit characters, T8 is the ninth bit of the transmitted character. T8 is loaded into the transmit shift register at the same time that the SCDR is loaded into the transmit register. Resets have no effect on the T8 bit.

M — Character Length Bit

This read/write bit determines whether SCI characters are 8 bits long or 9 bits long. The ninth bit can be used as an extra stop bit, as a receiver wakeup signal, or as a mark or space parity bit. Resets have no effect on the M bit.

1 = 9-bit SCI characters
0 = 8-bit SCI characters

WAKE — Wakeup Method Bit

This read/write bit determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit (MSB) position of a received character or an idle condition on the PD0/RDI pin. Resets have no effect on the WAKE bit.

1 = Address mark wakeup
0 = Idle line wakeup

9.13.3 SCI Control Register 2

SCI control register 2 (SCCR2), shown in Figure 9-10, has these functions:

- Enables the SCI receiver and SCI receiver interrupts
- Enables the SCI transmitter and SCI transmitter interrupts
- Enables SCI receiver idle interrupts
- Enables SCI transmission complete interrupts
- Enables SCI wakeup
- Transmits SCI break characters

$000F	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset:	0	0	0	0	0	0	0	0

Figure 9-10. SCI Control Register 2 (SCCR2)

TIE — Transmit Interrupt Enable Bit

This read/write bit enables SCI interrupt requests when the TDRE flag becomes set. Resets clear the TIE bit.

1 = TDRE interrupt requests enabled
0 = TDRE interrupt requests disabled

TCIE — Transmission Complete Interrupt Enable Bit

This read/write bit enables SCI interrupt requests when the TC flag becomes set. Resets clear the TCIE bit.

1 = TC interrupt requests enabled
0 = TC interrupt requests disabled

Clearing the MODF bit is accomplished by reading the SPSR (with MODF set), followed by a write to the SPCR. Control bits SPE and MSTR may be restored by user software to their original state during this clearing sequence or after the MODF bit has been cleared. When configured as an MC68HC05C9A, it is also necessary to restore DDRD after a mode fault.

Bits 5 and 3–0 — Not Implemented

These bits always read 0.

10.5.3 Serial Peripheral Data I/O Register

The serial peripheral data I/O register (SPDR), shown in Figure 10-6, is used to transmit and receive data on the serial bus. Only a write to this register will initiate transmission/reception of another byte and this will only occur in the master device. At the completion of transmitting a byte of data, the SPIF status bit is set in both the master and slave devices.

When the user reads the serial peripheral data I/O register, a buffer is actually being read. The first SPIF must be cleared by the time a second transfer of the data from the shift register to the read buffer is initiated or an overrun condition will exist. In cases of overrun, the byte which causes the overrun is lost.

A write to the serial peripheral data I/O register is not buffered and places data directly into the shift register for transmission.

$000C	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Reset:	Unaffected by reset							

Figure 10-6. PI Data Register (SPDR)

11.3 Instruction Types

The MCU instructions fall into the following five categories:

- Register/Memory instructions
- Read-Modify-Write instructions
- Jump/Branch instructions
- Bit Manipulation instructions
- Control instructions

11.3.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 11-1. Register/Memory Instructions

Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

11.3.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

Table 11-4. Bit Manipulation Instructions

Instruction	Mnemonic
Bit Clear	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Bit Set	BSET

11.3.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 11-5. Control Instructions

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

12.6 3.3-Vdc Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	V_{OL} V_{OH}	— V_{DD} –0.1	— —	0.1 —	V
Output high voltage (I_{Load} = –0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP, PD7, PD0 (I_{Load} = –0.4 mA) PD5–PD1 (I_{Load} = –1.5 mA) PC7	V_{OH}	V_{DD} –0.3 V_{DD} –0.3 V_{DD} –0.3	— — —	— — —	V
Output low voltage (I_{Load} = 0.4mA) PA7–PA0, PB7–PB0, PC6–PC0, PD7, PD5–PD0, TCMP (I_{Load} = 6 mA) PC7	V_{OL}	— —	— —	0.3 0.3	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current (3.0–3.6 Vdc @ f_{OP} = 1.0 MHz) Run[3] Wait[4] Stop[5] 25°C –40 to 85°C	I_{DD}	 — — — —	 1.0 500 1.0 2.5	 1.6 900 8 20	 mA µA µA µA
I/O ports hi-Z leakage current PA7–PA0, PB7–PB0 (without pullup) PC7–PC0, PD7, PD5–PD0	I_{OZ}	—	—	10	µA
Input current $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5–PD0	I_{In}	—	—	1	µA
Input pullup current[6] PB7–PB0 (with pullup)	I_{In}	0.5	—	20	µA
Capacitance Ports (as input or output) $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5, PD0	C_{Out} C_{In}	— —	— —	12 8	pF

1. V_{DD} = 3.3 Vdc ± 0.3 Vdc, V_{SS} = 0 Vdc, T_A = –40 to +85 °C, unless otherwise noted
2. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.
5. Stop I_{DD} measured with OSC1 = 0.2 V; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V.
6. Input pullup current measured with V_{IL} = 0.2 V.

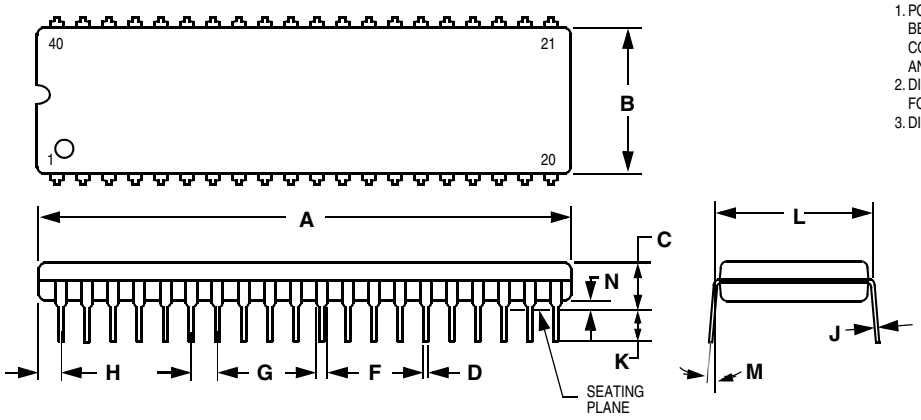
Chapter 13
Mechanical Specifications

13.1 Introduction

This section describes the dimensions of the plastic dual in-line package (DIP), plastic shrink dual in-line package (SDIP), plastic leaded chip carrier (PLCC), and quad flat pack (QFP) MCU packages.

The following figures show the latest package drawings at the time of this publication. To make sure that you have the latest package specifications, contact your local Freescale Sales Office.

13.2 40-Pin Plastic Dual In-Line (DIP) Package (Case 711-03)



NOTES:
1. POSITION TOLERANCE OF LEADS (D), SHALL BEWITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITIONS, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	1°	0°	1°
N	0.51	1.02	0.020	0.040

Figure 13-1. 40-Pin Plastic DIP Package (Case 711-03)

A.4 Programming Register (PROG)

This register is used to program the EPROM array. To program a byte of EPROM, set LATCH, write data to the desired address, and set EPGM for t_{EPGM}.

$001X	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:						LATCH		EPGM
Reset:	0	0	0	0	0	0	0	0

Figure A-1. EPROM Programming Register

LATCH — EPROM Latch Control Bit

This read/write bit controls the latching of the address and data buses when programming the EPROM.

1 = Address and data buses latched when the following instruction is a write to 1 of the EPROM locations. Normal reading is disabled if LATCH = 1.

0 = EPROM address and data bus configured for normal reading

EPGM — EPROM Program Control Bit

This read/write bit controls whether the programming voltage is applied to the EPROM array. For programming, this bit can be set only if the LATCH bit has been set previously. Both EPGM and LATCH cannot be set in the single write.

1 = Programming voltage applied to EPROM array

0 = Programming voltage not applied to EPROM array

NOTE

Bits 7–3 and bit 1 MUST be set to 0 when writing to the EPROM programming register.

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