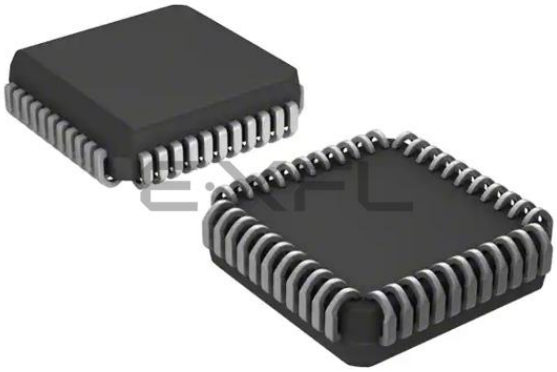

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.59x16.59)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc705c9avfne

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General Description

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Memory

Chapter 3
Central Processor Unit (CPU)

1.3 Configuration Options

The options and functions of the MC68HC705C9A can be configured to emulate either the MC68HC05C9A or the MC68HC05C12A.

The ROM device MC68HC05C9A has eight ROM mask options to select external interrupt/internal pullup capability on each of the eight port B bits. Other optional features are controlled by software addressable registers during operation of the microcontroller. These features are IRQ sensitivity and memory map configuration.

On the ROM device MC68HC05C12A, all optional features are controlled by ROM mask options. These features are the eight port B interrupt/pullup options, IRQ sensitivity, STOP instruction disable, and COP enable.

On the MC68HC705C9A the ROM mask options of the MC68HC05C9A and the MC68HC05C12A are controlled by mask option registers (MORs). The MORs are EPROM registers which must be programmed appropriately prior to operation of the microcontroller. The software options of the MC68HC05C9A are implemented by identical software registers in the MC68HC705C9A.

When configured as an MC68HC05C9A:

- The entire 16K memory map of the C9A is enabled, including dual-mapped RAM and EPROM at locations $0020–$004F and $0100–$017F.
- C12A options in the C12MOR ($3FF1) are disabled.
- The C9A option register ($3FDF) is enabled, allowing software control over the IRQ sensitivity and the memory map configuration.
- The C9A COP reset register ($001D) and the C9A COP control register ($001E) are enabled, allowing software control over the C9A COP and clock monitor.
- The C12 COP clear register ($3FF0) is disabled.
- The port D data direction register ($0007) is enabled, allowing output capability on the seven port D pins.
- SPI output signals (MOSI, MISO, and SCK) require the corresponding bits in the port D data direction register to be set for output.
- The port D wire-OR mode control bit (bit 5 of SPCR $000A) is enabled, allowing open-drain configuration of port D.
- The $\overline{\text{RESET}}$ pin becomes bidirectional; this pin is driven low by a C9A COP or clock monitor timeout or during power-on reset.

When configured as an MC68HC05C12A:

- Memory locations $0100–$0FFF are disabled, creating a memory map identical to the MC68HC05C12A.
- C12A options in the C12MOR ($3FF1) are enabled; these bits control IRQ sensitivity, STOP instruction disable and C12 COP enable.
- The C9A option register ($3FDF) is disabled, preventing software control over the IRQ sensitivity and the memory map configuration.
- The C9A COP reset register ($001D) and the C9A COP control register ($001E) are disabled, preventing software control over the C9A COP and clock monitor.
- The C12 COP clear register ($3FF0) is enabled; this write-only register is used to clear the C12 COP.

- The port D data direction register ($0007) is disabled and the seven port D pins become input only.
- SPI output signals (MOSI, MISO, and SCK) do not require the data direction register control for output capability.
- The port D wire-OR mode control bit (bit 5 of SPCR $000A) is disabled, preventing open-drain configuration of port D.
- The $\overline{\text{RESET}}$ pin becomes input only.

1.4 Mask Options

The following two mask option registers are used to select features controlled by mask changes on the MC68HC05C9A and the MC68HC05C12A:

- Port B mask option register (PBMOR)
- C12 mask option register (C12MOR)

The mask option registers are EPROM locations which must be programmed prior to operation of the microcontroller.

1.4.1 Port B Mask Option Register (PBMOR)

The PBMOR register, shown in Figure 1-2, contains eight programmable bits which determine whether each port B bit (when in input mode) has the pullup and interrupt enabled. The port B interrupts share the vector and edge/edge-level sensitivity with the $\overline{\text{IRQ}}$ pin. For more details, (see 4.3 External Interrupt (IRQ or Port B)).

$3FF0	Bit 7	6	5	4	3	2	1	Bit 0
	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0

Figure 1-2. Port B Mask Option Register

PBPU7–PBPU0 — Port B Pullup/Interrupt Enable Bits
1 = Pullup and CPU interrupt enabled
0 = Pullup and CPU interrupt disabled

NOTE

The current capability of the port B pullup devices is equivalent to the MC68HC05C9A, which is less than the MC68HC05C12A.

1.4.2 C12 Mask Option Register (C12MOR)

The C12MOR register, shown in Figure 1-3, controls the following options:

- Select between MC68HC05C9A/C12A configuration
- Enable/disable stop mode (C12A mode only)
- Enable/disable COP (C12A mode only)
- Edge-triggered only or edge- and level-triggered external interrupt pin (IRQ pin) (C12A mode only).

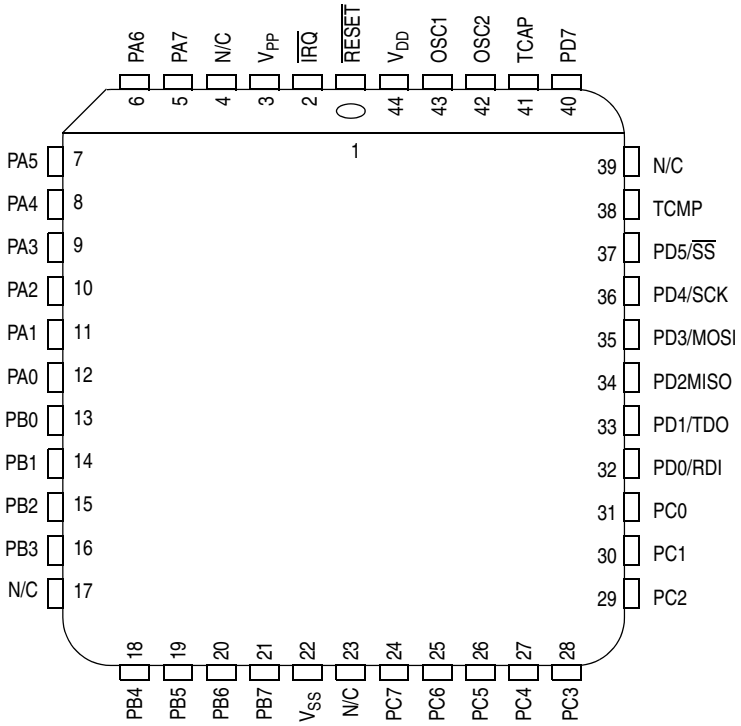


Figure 1-7. 44-Lead PLCC Pin Assignments

NOTE

The above 44-pin PLCC pin assignment diagram is for compatibility with MC68HC05C9A. To allow compatibility with the 44-pin PLCC MC68HC05C12A, pin17 and pin18 must be tied together and pin 39 and pin 40 also must be tied together.

To allow compatibility with MC68HC705C8A, pin 3 and pin 4 also should be tied together.

1.6.5 $\overline{\text{RESET}}$

As an input pin, this active low $\overline{\text{RESET}}$ pin is used to reset the MCU to a known startup state by pulling $\overline{\text{RESET}}$ low. As an output pin, when in MC68HC05C9A mode only, the $\overline{\text{RESET}}$ pin indicates that an internal MCU reset has occurred. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to
Chapter 5 Resets for more detail.

1.6.6 TCAP

This pin controls the input capture feature for the on-chip programmable timer. The TCAP pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to Chapter 8 Capture/Compare Timer for more detail.

1.6.7 TCMP

The TCMP pin provides an output for the output compare feature of the on-chip programmable timer. Refer to Chapter 8 Capture/Compare Timer for more detail.

1.6.8 PA0–PA7

These eight I/O lines comprise port A. The state of each pin is software programmable and all port A pins are configured as inputs during reset. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.9 PB0–PB7

These eight I/O lines comprise port B. The state of each pin is software programmable and all port B pins are configured as inputs during reset. Port B has mask option register enabled pullup devices and interrupt capability selectable for any pin. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.10 PC0–PC7

These eight I/O lines comprise port C. The state of each pin is software programmable and all port C pins are configured as inputs during reset. PC7 has high current sink and source capability. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

1.6.11 PD0–PD5 and PD7

These seven I/O lines comprise port D. When configured as a C9A the state of each pin is software programmable and all port D pins are configured as inputs during reset. When configured as a C12A, the port D pins are input only. Refer to Chapter 7 Input/Output (I/O) Ports for more detail.

4.4 Timer Interrupt

Three different timer interrupt flags cause a timer interrupt whenever they are set and enabled. The interrupt flags are in the timer status register (TSR), and the enable bits are in the timer control register (TCR). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF8 and $3FF9.

4.5 SCI Interrupt

Five different SCI interrupt flags cause an SCI interrupt whenever they are set and enabled. The interrupt flags are in the SCI status register (SCSR), and the enable bits are in the SCI control register 2 (SCCR2). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF6 and $3FF7.

4.6 SPI Interrupt

Two different SPI interrupt flags cause an SPI interrupt whenever they are set and enabled. The interrupt flags are in the SPI status register (SPSR), and the enable bits are in the SPI control register (SPCR). Either of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF4 and $3FF5.

Chapter 5
Resets

5.1 Introduction

The MCU can be reset four ways: by the initial power-on reset function, by an active low input to the $\overline{\text{RESET}}$ pin, by the COP, or by the clock monitor. A reset immediately stops the operation of the instruction being executed, initializes some control bits, and loads the program counter with a user-defined reset vector address. Figure 5-1 is a block diagram of the reset sources.

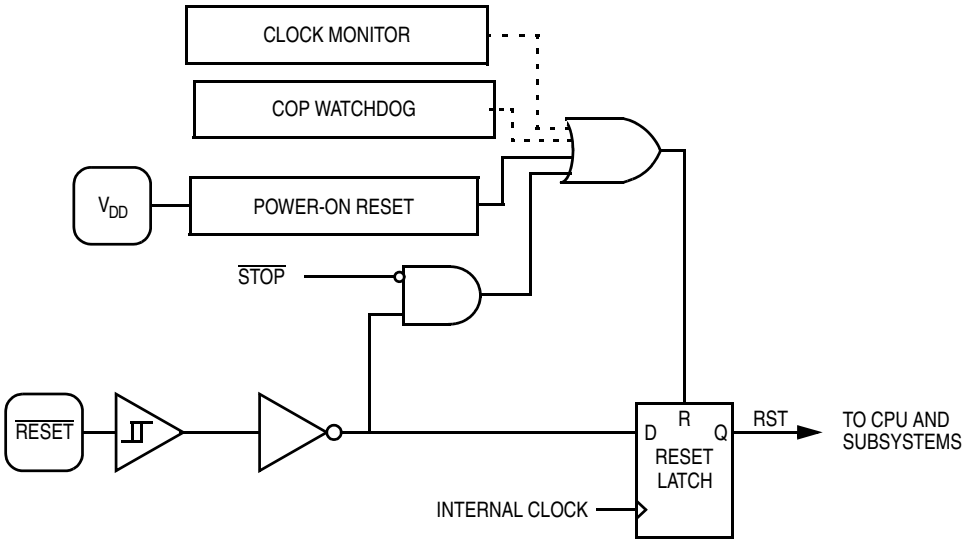


Figure 5-1. Reset Sources

5.2 Power-On Reset (POR)

A power-on-reset occurs when a positive transition is detected on V_{DD}. The power-on reset is strictly for power turn-on conditions and should not be used to detect a drop in the power supply voltage. There is a 4064 internal processor clock cycle (t_{cyc}) oscillator stabilization delay after the oscillator becomes active. (When configured as a C9A, the $\overline{\text{RESET}}$ pin will output a logic 0 during the 4064-cycle delay.) If the $\overline{\text{RESET}}$ pin is low after the end of this 4064-cycle delay, the MCU will remain in the reset condition until $\overline{\text{RESET}}$ is driven high externally.

5.3 $\overline{\text{RESET}}$ Pin

The function of the $\overline{\text{RESET}}$ pin is dependent on whether the device is configured as an MC68HC05C9A or an MC68HC05C12A. When it is in the MC68HC05C12A configuration, the pin is input only. When in MC68HC05C9A configuration the pin is bidirectional. In both cases the MCU is reset when a logic 0 is applied to the $\overline{\text{RESET}}$ pin for a period of one and one-half machine cycles (t_{RL}). For the MC68HC05C9A configuration, the $\overline{\text{RESET}}$ pin will be driven low by a COP, clock monitor, or power-on reset.

7.3 Port B

Port B is an 8-bit bidirectional port. The port B data register is at $0001 and the data direction register (DDR) is at $0005. The contents of the port B data register are indeterminate at initial powerup and must be initialized by user software. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a 1 to a DDR bit sets the corresponding port pin to output mode. Each of the port B pins has an optional external interrupt capability that can be enabled by programming the corresponding bit in the port B mask option register ($3FF0).

The interrupt option also enables a pullup device when the pin is configured as an input. The edge or edge- and level-sensitivity of the $\overline{\text{IRQ}}$ pin will also pertain to the enabled port B pins. Care needs to be taken when using port B pins that have the pullup enabled. Before switching from an output to an input, the data should be preconditioned to a 1 to prevent an interrupt from occurring. The port B logic is shown in Figure 7-2.

7.4 Port C

Port C is an 8-bit bidirectional port. The port C data register is at $0002 and the data direction register (DDR) is at $0006. The contents of the port C data register are indeterminate at initial powerup and must be initialized by user software. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a 1 to a DDR bit sets the corresponding port bit to output mode. PC7 has a high current sink and source capability. Figure 7-1 is also applicable to port C.

7.5 Port D

When configured as a C9A, port D is a 7-bit bidirectional port; when configured as a C12A, port D is a 7-bit fixed input port. Four of its pins are shared with the SPI subsystem and two more are shared with the SCI subsystem. The contents of the port D data register are indeterminate at initial powerup and must be initialized by user software. During reset all seven bits become valid input ports because the C9A DDR bits are cleared and the special function output drivers associated with the SCI and SPI subsystems are disabled, thereby returning the ports to inputs. Writing a 1 to a DDR bit sets the corresponding port bit to output mode only when configured as a C9A.

9.4 SCI Transmitter Features

Features of the SCI transmitter include:

- Transmit data register empty flag
- Transmit complete flag
- Send break

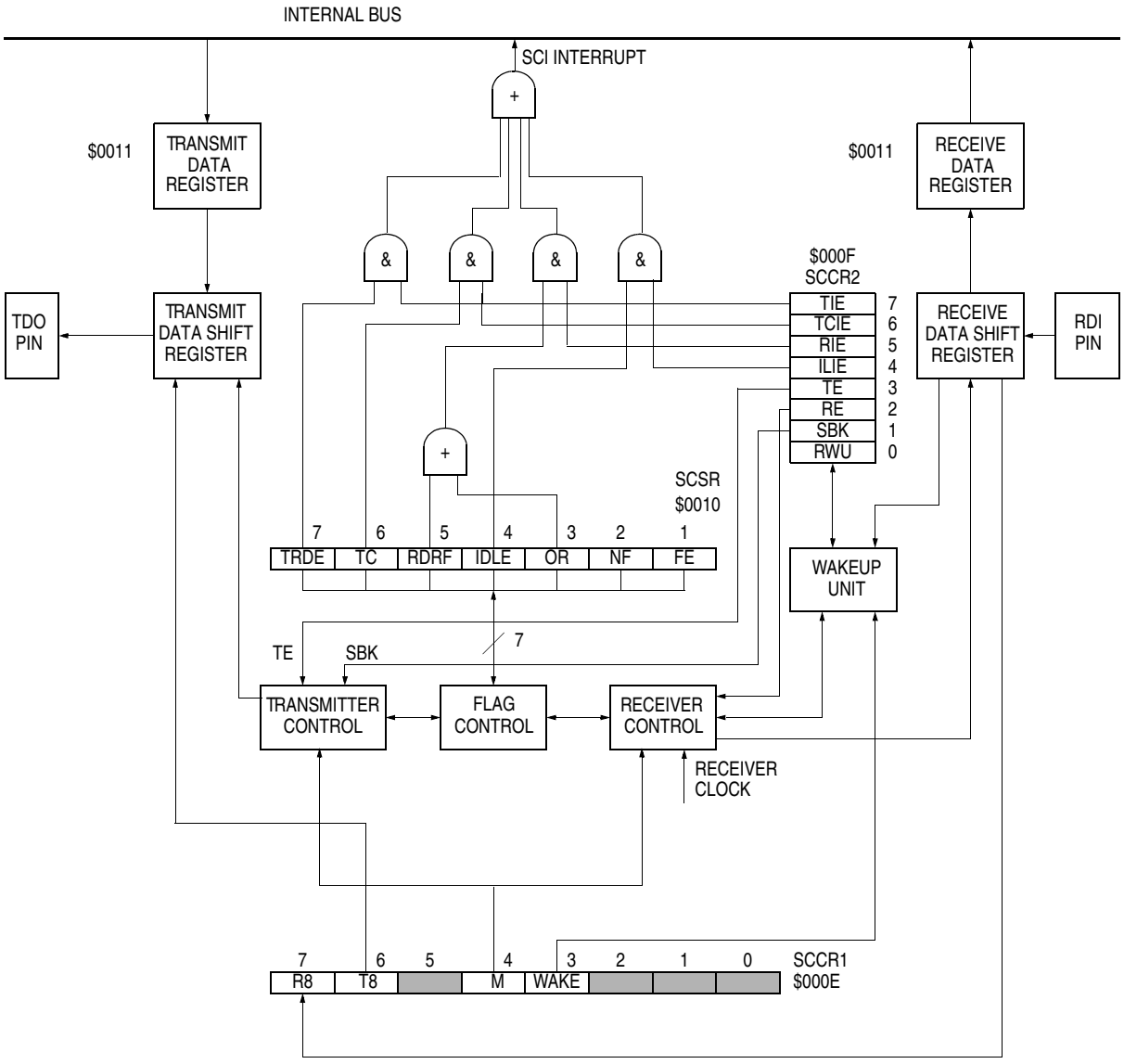


Figure 9-1. Serial Communications Interface Block Diagram

NOTE

The serial communications data register (SCI SCDR) is controlled by the internal R/W signal. It is the transmit data register when written to and the receive data register when read.

$0010	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	
Write:								
Reset:	1	1	0	0	0	0	0	—

= Unimplemented

Figure 9-11. SCI Status Register (SCSR)

TDRE — Transmit Data Register Empty Flag

This clearable, read-only flag is set when the data in the SCDR transfers to the transmit shift register. TDRE generates an interrupt request if the TIE bit in SCCR2 is also set. Clear the TDRE bit by reading the SCSR with TDRE set and then writing to the SCDR. Reset sets the TDRE bit. Software must initialize the TDRE bit to logic 0 to avoid an instant interrupt request when turning the transmitter on.

1 = SCDR data transferred to transmit shift register
0 = SCDR data not transferred to transmit shift register

TC — Transmission Complete Flag

This clearable, read-only flag is set when the TDRE bit is set, and no data, preamble, or break character is being transmitted. TDRE generates an interrupt request if the TCIE bit in SCCR2 is also set. Clear the TC bit by reading the SCSR with TC set, and then writing to the SCDR. Reset sets the TC bit. Software must initialize the TC bit to logic 0 to avoid an instant interrupt request when turning the transmitter on.

1 = No transmission in progress
0 = Transmission in progress

RDRF — Receive Data Register Full Flag

This clearable, read-only flag is set when the data in the receive shift register transfers to the SCI data register. RDRF generates an interrupt request if the RIE bit in the SCCR2 is also set. Clear the RDRF bit by reading the SCSR with RDRF set and then reading the SCDR.

1 = Received data available in SCDR
0 = Received data not available in SCDR

IDLE — Receiver Idle Flag

This clearable, read-only flag is set when 10 or 11 consecutive logic 1s appear on the receiver input. IDLE generates an interrupt request if the ILIE bit in the SCCR2 is also set. Clear the ILIE bit by reading the SCSR with IDLE set and then reading the SCDR.

1 = Receiver input idle
0 = Receiver input not idle

OR — Receiver Overrun Flag

This clearable, read-only flag is set if the SCDR is not read before the receive shift register receives the next word. OR generates an interrupt request if the RIE bit in the SCCR2 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading the SCSR with OR set and then reading the SCDR.

1 = Receive shift register full and RDRF = 1
0 = No receiver overrun

NF — Receiver Noise Flag

This clearable, read-only flag is set when noise is detected in data received in the SCI data register. Clear the NF bit by reading the SCSR and then reading the SCDR.

1 = Noise detected in SCDR
0 = No noise detected in SCDR

$000A	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	DWOM (C9A)	MSTR	CPOL	CPHA	SPR1	SPR0
Reset:	0	0	0	0	0	1	U	U

U = Undetermined

Figure 10-4. SPI Control Register (SPCR)

SPIE — Serial Peripheral Interrupt Enable Bit

This read/write bit enables SPI interrupts. Reset clears the SPIE bit.

1 = SPI interrupts enabled
0 = SPI interrupts disabled

SPE — Serial Peripheral System Enable Bit

This read/write bit enables the SPI. Reset clears the SPE bit.

1 = SPI system enabled
0 = SPI system disabled

DWOM — Port D Wire-OR Mode Option Bit

This read/write bit disables the high side driver transistors on port D outputs so that port D outputs become open-drain drivers. DWOM affects all seven port D pins together. This option is only available when configured as a C9A.

1 = Port D outputs act as open-drain outputs.
0 = Port D outputs are normal CMOS outputs.

MSTR — Master Mode Select Bit

This read/write bit selects master mode operation or slave mode operation. Reset clears the MSTR bit.

1 = Master mode
0 = Slave mode

CPOL — Clock Polarity Bit

When the clock polarity bit is cleared and data is not being transferred, a steady state low value is produced at the SCK pin of the master device. Conversely, if this bit is set, the SCK pin will idle high. This bit is also used in conjunction with the clock phase control bit to produce the desired clock-data relationship between master and slave. See Figure 10-1.

CPHA — Clock Phase Bit

The clock phase bit, in conjunction with the CPOL bit, controls the clock-data relationship between master and slave. The CPOL bit can be thought of as simply inserting an inverter in series with the SCK line. The CPHA bit selects one of two fundamentally different clocking protocols. When CPHA = 0, the shift clock is the OR of SCK with $\overline{SS}$. As soon as $\overline{SS}$ goes low, the transaction begins and the first edge on SCK invokes the first data sample. When CPHA=1, the $\overline{SS}$ pin may be thought of as a simple output enable control. See Figure 10-1.

SPR1 and SPR0 — SPI Clock Rate Selects

These read/write bits select one of four master mode serial clock rates, as shown in Table 10-1. They have no effect in the slave mode.

11.3.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register.

NOTE

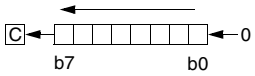
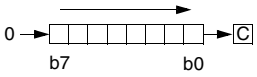
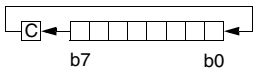
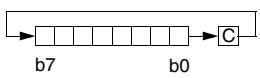
Do not use read-modify-write operations on write-only registers.

Table 11-2. Read-Modify-Write Instructions

Instruction	Mnemonic
Arithmetic Shift Left (Same as LSL)	ASL
Arithmetic Shift Right	ASR
Bit Clear	BCLR(1)
Bit Set	BSET(1)
Clear Register	CLR
Complement (One's Complement)	COM
Decrement	DEC
Increment	INC
Logical Shift Left (Same as ASL)	LSL
Logical Shift Right	LSR
Negate (Two's Complement)	NEG
Rotate Left through Carry Bit	ROL
Rotate Right through Carry Bit	ROR
Test for Negative or Zero	TST(2)

1. Unlike other read-modify-write instructions, BCLR and BSET use only direct addressing.
2. TST is an exception to the read-modify-write sequence because it does not write a replacement value.

Table 11-6. Instruction Set Summary (Sheet 4 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff 	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		1 1
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff 	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff 	5 3 3 6 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2

12.5 5.0-Vdc Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	V_{OL} V_{OH}	— V_{DD} –0.1	— —	0.1 —	V
Output high voltage (I_{Load} = –0.8 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP, PD7, PD0 (I_{Load} = –1.6 mA) PD5–PD1 (I_{Load} = –5.0 mA) PC7	V_{OH}	V_{DD} –0.8 V_{DD} –0.8 V_{DD} –0.8	— — —	— — —	V
Output low voltage (I_{Load} = 1.6 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD7, PD5–PD0, TCMP (I_{Load} = 10 mA) PC7	V_{OL}	— —	— —	0.4 0.4	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current (4.5–5.5 Vdc @ f_{OP} = 2.1 MHz) Run[3] Wait[4] Stop[5] 25°C –40 to 85 °C	I_{DD}	 — — — —	 3.5 1.0 1.0 7.0	 5.25 3.25 20.0 50.0	 mA mA µA µA
I/O ports hi-Z leakage current PA7–PA0, PB7–PB0 (without pullup) PC7–PC0, PD7, PD5–PD0	I_{OZ}	—	—	10	µA
Input current $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5–PD0	I_{In}	—	—	1	µA
Input pullup current[6] PB7–PB0 (with pullup)	I_{In}	5	—	60	µA
Capacitance Ports (as input or output) $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5, PD0	C_{Out} C_{In}	— —	— —	12 8	pF
Programming voltage (25°C)	V_{PP}	15.0	16.0	17.0	V
Programming current (25°C)	I_{PP}	—	—	200	mA

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 to +85 °C, unless otherwise noted
2. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.
5. Stop I_{DD} measured with OSC1 = 0.2 V; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V.
6. Input pullup current measured with V_{IL} = 0.2 V.

Appendix A
EPROM Programming

A.1 Introduction

This section describes programming of the EPROM.

A.2 Bootloader Mode

Table A-1. Operating Modes

$\overline{\text{RESET}}$	$\overline{\text{IRQ}}$	TCAP	Mode
	V_{SS} to V_{DD} V_{TST}	V_{SS} to V_{DD} V_{DD}	User Bootloader

Bootloader mode is entered upon the rising edge of $\overline{\text{RESET}}$ if the $\overline{\text{IRQ}}$ is at V_{TST} and the TCAP pin is at logic one. The bootloader code resides in the ROM from $3F00 to $3FEF. This program handles copying of user code from an external EPROM into the on-chip EPROM. The bootload function does not have to be done from an external EPROM, but it may be done from a host.

The user code must be a one-to-one correspondence with the internal EPROM addresses.

A.3 Bootloader Functions

Three pins are used to select various bootloader functions: PD5, PD4, and PD3. Two other pins, PC6 and PC7, are used to drive the PROG LED and the VERF LED, respectively. The programming modes are shown in Table A-2.

Table A-2. Bootloader Functions

PD5	PD4	PD3	Mode
0	0	0	Program/verify
0	0	1	Verify only
0	1	0	Load RAM and execute
1	X	X	Secure

Appendix B
M68HC05Cx Family Feature Comparisons

Refer to Table B-1 for a comparison of the features for all the M68HC05C Family members.

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