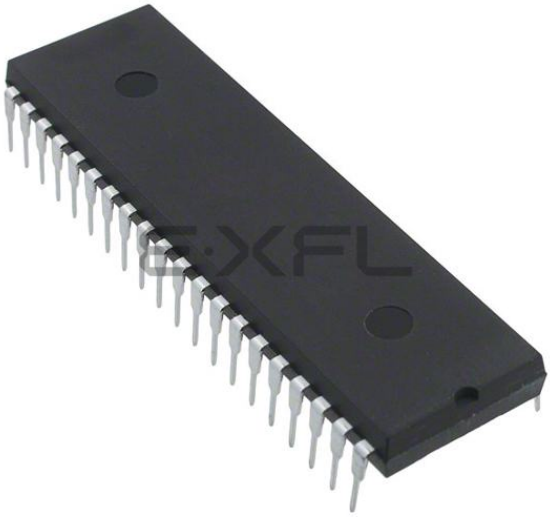

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC05
Core Size	8-Bit
Speed	2.1MHz
Connectivity	SCI, SPI
Peripherals	POR, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	352 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc705c9acpe

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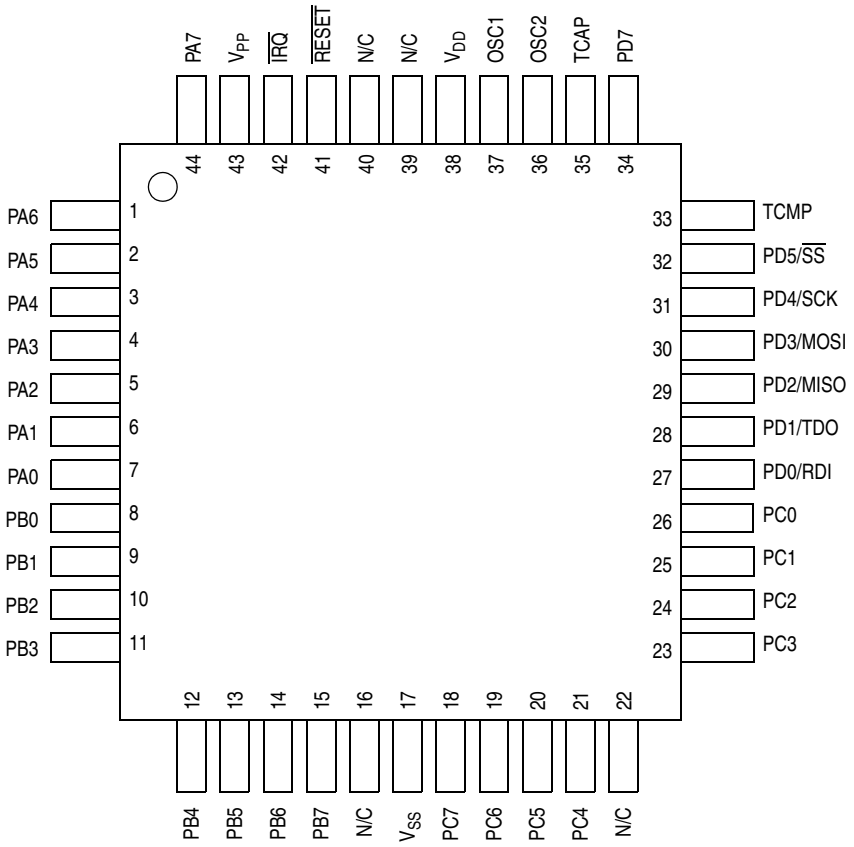


Figure 1-8. 44-Pin QFP Pin Assignments

1.6.1 V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is the positive supply and V_{SS} is ground.

1.6.2 V_{PP}

This pin provides the programming voltage to the EPROM array. For normal operation, V_{PP} should be tied to V_{DD}.

1.6.3 $\overline{IRQ}$

This interrupt pin has an option that provides two different choices of interrupt triggering sensitivity. The $\overline{IRQ}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to Chapter 4 Interrupts for more detail.

1.6.4 OSC1 andOSC2

These pins provide control input for an on-chip clock oscillator circuit. A crystal connected to these pins provides a system clock. The internal frequency is one-half the crystal frequency.

Chapter 3
Central Processor Unit (CPU)

3.1 Introduction

This section contains the basic programmers model and the registers contained in the CPU.

3.2 CPU Registers

The MCU contains five registers as shown in the programming model of Figure 3-1. The interrupt stacking order is shown in Figure 3-2.

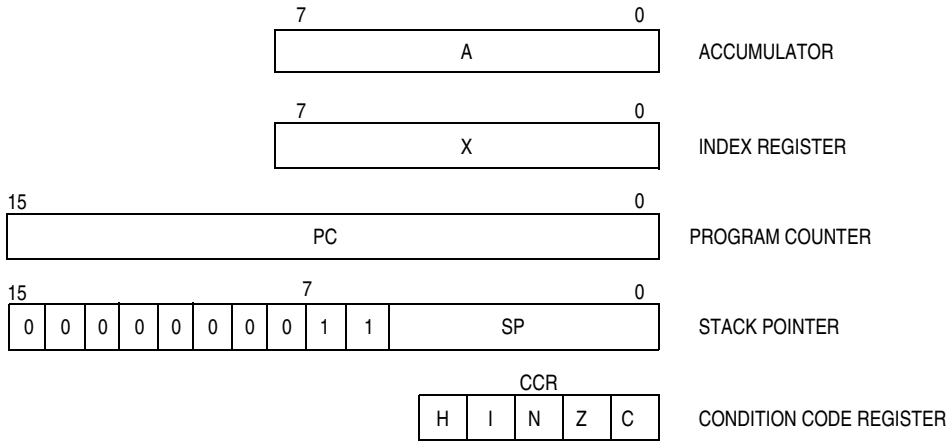


Figure 3-1. Programming Model

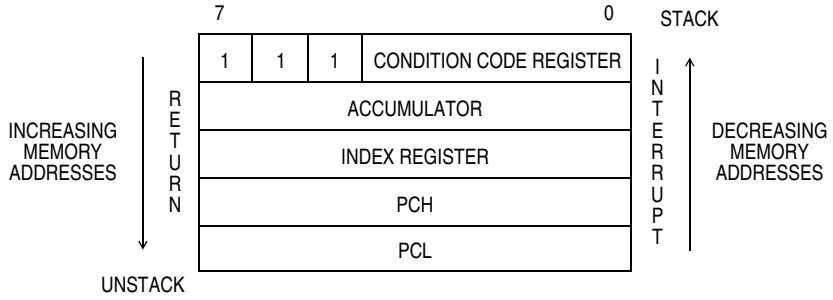


Figure 3-2. Interrupt Stacking Order

4.4 Timer Interrupt

Three different timer interrupt flags cause a timer interrupt whenever they are set and enabled. The interrupt flags are in the timer status register (TSR), and the enable bits are in the timer control register (TCR). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF8 and $3FF9.

4.5 SCI Interrupt

Five different SCI interrupt flags cause an SCI interrupt whenever they are set and enabled. The interrupt flags are in the SCI status register (SCSR), and the enable bits are in the SCI control register 2 (SCCR2). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF6 and $3FF7.

4.6 SPI Interrupt

Two different SPI interrupt flags cause an SPI interrupt whenever they are set and enabled. The interrupt flags are in the SPI status register (SPSR), and the enable bits are in the SPI control register (SPCR). Either of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF4 and $3FF5.

Chapter 8
Capture/Compare Timer

8.1 Introduction

This section describes the operation of the 16-bit capture/compare timer. Figure 8-1 shows the structure of the capture/compare subsystem.

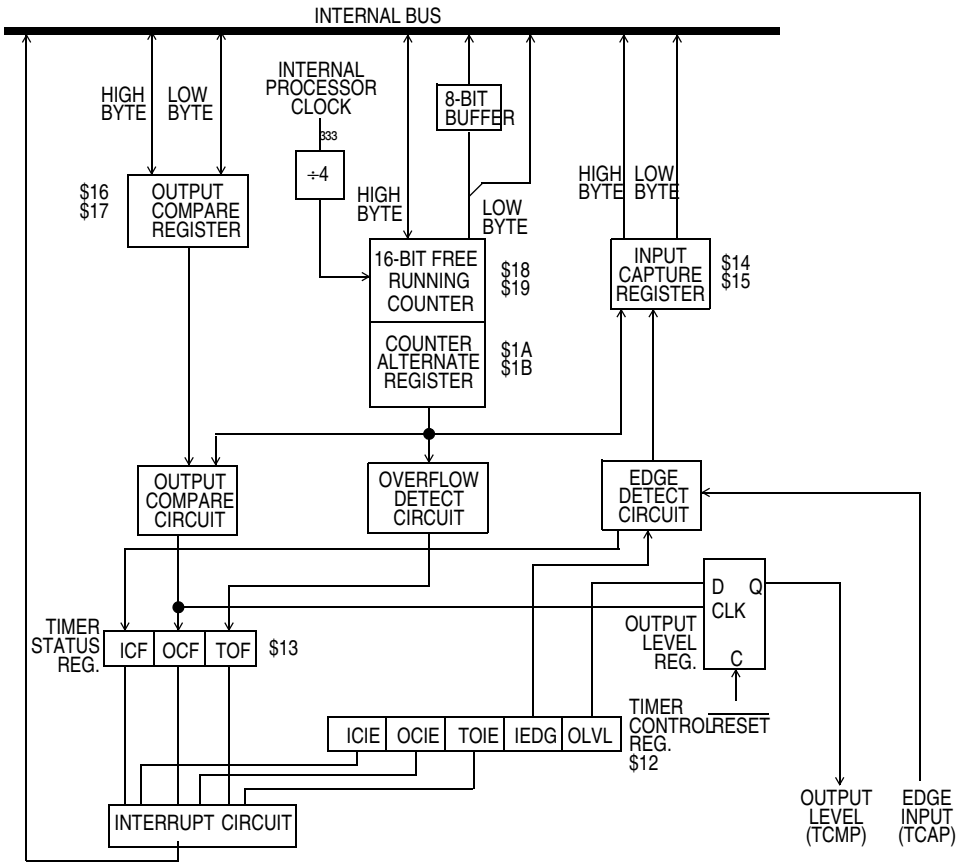


Figure 8-1. Capture/Compare Timer Block Diagram

To prevent OCF from being set between the time it is read and the time the output compare registers are updated, use this procedure:

1. Disable interrupts by setting the I bit in the condition code register.
2. Write to OCRH. Compares are now inhibited until OCRL is written.
3. Clear bit OCF by reading timer status register (TSR).
4. Enable the output compare function by writing to OCRL.
5. Enable interrupts by clearing the I bit in the condition code register.

8.4 Timer During Wait Mode

The CPU clock halts during the wait mode, but the timer remains active. If interrupts are enabled, a timer interrupt will cause the processor to exit the wait mode.

8.5 Timer During Stop Mode

In the stop mode, the timer stops counting and holds the last count value if STOP is exited by an interrupt. If STOP is exited by reset, the counters are forced to $FFFC. During STOP, if at least one valid input capture edge occurs at the TCAP pins, the input capture detect circuit is armed. This does not set any timer flags or wake up the MCU, but if an interrupt is used to exit stop mode, there is an active input capture flag and data from the first valid edge that occurred during the stop mode. If reset is used to exit stop mode, then no input capture flag or data remains, even if a valid input capture edge occurred.

9.9 Address Mark Wakeup

In address mark wakeup, the most significant bit (MSB) in a character is used to indicate whether it is an address (logic 1) or data (logic 0) character. Sleeping receivers will wake up whenever an address character is received. Systems using this method for wakeup would set the MSB of the first character of each message and leave it clear for all other characters in the message. Idle periods may be present within messages and no idle time is required between messages for this wakeup method.

9.10 Receive Data In (RDI)

Receive data is the serial data that is applied through the input line and the SCI to the internal bus. The receiver circuitry clocks the input at a rate equal to 16 times the baud rate. This time is referred to as the RT rate in Figure 9-4 and as the receiver clock in Figure 9-6.

The receiver clock generator is controlled by the baud rate register; however, the SCI is synchronized by the start bit, independent of the transmitter.

Once a valid start bit is detected, the start bit, each data bit, and the stop bit are sampled three times at RT intervals 8 RT, 9 RT, and 10 RT
(1 RT is the position where the bit is expected to start), as shown in Figure 9-5. The value of the bit is determined by voting logic which takes the value of the majority of the samples. A noise flag is set when all three samples on a valid start bit or data bit or the stop bit do not agree.

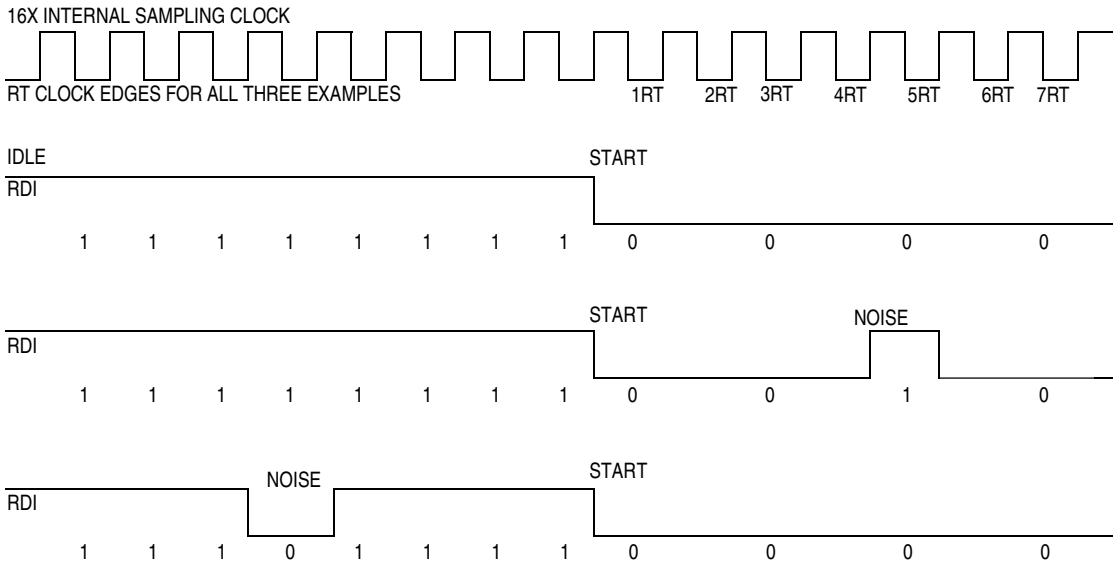


Figure 9-4. SCI Examples of Start Bit Sampling Techniques

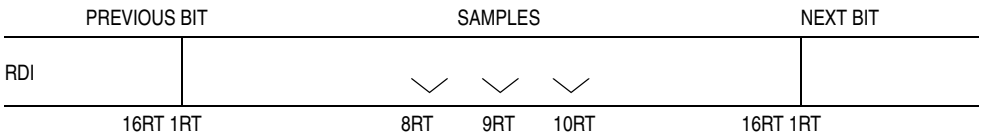


Figure 9-5. SCI Sampling Technique Used on All Bits

T8 — Bit 8 (Transmitted)

When the SCI is transmitting 9-bit characters, T8 is the ninth bit of the transmitted character. T8 is loaded into the transmit shift register at the same time that the SCDR is loaded into the transmit register. Resets have no effect on the T8 bit.

M — Character Length Bit

This read/write bit determines whether SCI characters are 8 bits long or 9 bits long. The ninth bit can be used as an extra stop bit, as a receiver wakeup signal, or as a mark or space parity bit. Resets have no effect on the M bit.

1 = 9-bit SCI characters
0 = 8-bit SCI characters

WAKE — Wakeup Method Bit

This read/write bit determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit (MSB) position of a received character or an idle condition on the PD0/RDI pin. Resets have no effect on the WAKE bit.

1 = Address mark wakeup
0 = Idle line wakeup

9.13.3 SCI Control Register 2

SCI control register 2 (SCCR2), shown in Figure 9-10, has these functions:

- Enables the SCI receiver and SCI receiver interrupts
- Enables the SCI transmitter and SCI transmitter interrupts
- Enables SCI receiver idle interrupts
- Enables SCI transmission complete interrupts
- Enables SCI wakeup
- Transmits SCI break characters

$000F	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset:	0	0	0	0	0	0	0	0

Figure 9-10. SCI Control Register 2 (SCCR2)

TIE — Transmit Interrupt Enable Bit

This read/write bit enables SCI interrupt requests when the TDRE flag becomes set. Resets clear the TIE bit.

1 = TDRE interrupt requests enabled
0 = TDRE interrupt requests disabled

TCIE — Transmission Complete Interrupt Enable Bit

This read/write bit enables SCI interrupt requests when the TC flag becomes set. Resets clear the TCIE bit.

1 = TC interrupt requests enabled
0 = TC interrupt requests disabled

$0010	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	
Write:								
Reset:	1	1	0	0	0	0	0	—

= Unimplemented

Figure 9-11. SCI Status Register (SCSR)

TDRE — Transmit Data Register Empty Flag

This clearable, read-only flag is set when the data in the SCDR transfers to the transmit shift register. TDRE generates an interrupt request if the TIE bit in SCCR2 is also set. Clear the TDRE bit by reading the SCSR with TDRE set and then writing to the SCDR. Reset sets the TDRE bit. Software must initialize the TDRE bit to logic 0 to avoid an instant interrupt request when turning the transmitter on.

1 = SCDR data transferred to transmit shift register
0 = SCDR data not transferred to transmit shift register

TC — Transmission Complete Flag

This clearable, read-only flag is set when the TDRE bit is set, and no data, preamble, or break character is being transmitted. TDRE generates an interrupt request if the TCIE bit in SCCR2 is also set. Clear the TC bit by reading the SCSR with TC set, and then writing to the SCDR. Reset sets the TC bit. Software must initialize the TC bit to logic 0 to avoid an instant interrupt request when turning the transmitter on.

1 = No transmission in progress
0 = Transmission in progress

RDRF — Receive Data Register Full Flag

This clearable, read-only flag is set when the data in the receive shift register transfers to the SCI data register. RDRF generates an interrupt request if the RIE bit in the SCCR2 is also set. Clear the RDRF bit by reading the SCSR with RDRF set and then reading the SCDR.

1 = Received data available in SCDR
0 = Received data not available in SCDR

IDLE — Receiver Idle Flag

This clearable, read-only flag is set when 10 or 11 consecutive logic 1s appear on the receiver input. IDLE generates an interrupt request if the ILIE bit in the SCCR2 is also set. Clear the ILIE bit by reading the SCSR with IDLE set and then reading the SCDR.

1 = Receiver input idle
0 = Receiver input not idle

OR — Receiver Overrun Flag

This clearable, read-only flag is set if the SCDR is not read before the receive shift register receives the next word. OR generates an interrupt request if the RIE bit in the SCCR2 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading the SCSR with OR set and then reading the SCDR.

1 = Receive shift register full and RDRF = 1
0 = No receiver overrun

NF — Receiver Noise Flag

This clearable, read-only flag is set when noise is detected in data received in the SCI data register. Clear the NF bit by reading the SCSR and then reading the SCDR.

1 = Noise detected in SCDR
0 = No noise detected in SCDR

Chapter 10
Serial Peripheral Interface (SPI)

10.1 Introduction

The serial peripheral interface (SPI) is an interface built into the device which allows several MC68HC05 MCUs, or MC68HC05 MCU plus peripheral devices, to be interconnected within a single printed circuit board. In an SPI, separate wires are required for data and clock. In the SPI format, the clock is not included in the data stream and must be furnished as a separate signal. An SPI system may be configured in one containing one master MCU and several slave MCUs, or in a system in which an MCU is capable of being a master or a slave.

10.2 Features

Features include:

- Full-duplex, four-wire synchronous transfers
- Master or slave operation
- Bus frequency divided by 2 (maximum) master bit frequency
- Bus frequency (maximum) slave bit frequency
- Four programmable master bit rates
- Programmable clock polarity and phase
- End of transmission interrupt flag
- Write collision flag protection
- Master-master mode fault protection capability

10.3 SPI Signal Description

The four basic signals (MOSI, MISO, SCK, and $\overline{SS}$) are described in the following paragraphs. Each signal function is described for both the master and slave modes.

NOTE

In C9A mode, any SPI output line has to have its corresponding data direction register bit set. If this bit is clear, the line is disconnected from the SPI logic and becomes a general-purpose input line. When the SPI is enabled, any SPI input line is forced to act as an input regardless of what is in the corresponding data direction register bit.

Chapter 11
Instruction Set

11.1 Introduction

The microcontroller unit (MCU) instruction set has 62 instructions and uses eight addressing modes. The instructions include all those of the M146805 CMOS (complementary metal oxide silicon) Family plus one more: the unsigned multiply (MUL) instruction. The MUL instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is stored in the index register, and the low-order product is stored in the accumulator.

11.2 Addressing Modes

The central processor unit (CPU) uses eight addressing modes for flexibility in accessing data. The addressing modes provide eight different ways for the CPU to find the data required to execute an instruction. The eight addressing modes are:

- Inherent
- Immediate
- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset
- Relative

11.2.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no operand address and are one byte long.

11.2.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no operand address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

11.2.3 Direct

Direct instructions can access any of the first 256 memory locations with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses $00 as the high byte of the operand address.

Table 11-6. Instruction Set Summary (Sheet 3 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
CLR *opr* CLRA CLRX CLR *opr*,X CLR ,X	Clear Byte	M ← $00 A ← $00 X ← $00 M ← $00 M ← $00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff 	5 3 3 6 5
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff 	2 3 4 5 4 3
COM *opr* COMA COMX COM *opr*,X COM ,X	Complement Byte (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (A) X ← ($\overline{X}$) = $FF – (X) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	—	—	↕	↕	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff 	5 3 3 6 5
CPX #*opr* CPX *opr* CPX *opr* CPX *opr*,X CPX *opr*,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff 	2 3 4 5 4 3
DEC *opr* DECA DECX DEC *opr*,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff 	5 3 3 6 5
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff 	2 3 4 5 4 3
INC *opr* INCA INCX INC *opr*,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff 	5 3 3 6 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff 	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff 	5 6 7 6 5

Chapter 12
Electrical Specifications

12.1 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table below. Keep V_{In} and V_{Out} within the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage Normal operation Bootloader mode ($\overline{IRQ}$ pin only)	V_{In}	V_{SS} –0.3 to V_{DD} + 0.3 V_{SS} –0.3 to 2 x V_{DD} + 0.3	V
Current drain per pin (Excluding V_{DD} and V_{SS})	I	25	mA
Storage temperature range	T_{STG}	–65 to +150	°C

NOTE

This device is not guaranteed to operate properly at the maximum ratings. Refer to 12.5 5.0-Vdc Electrical Characteristics for guaranteed operating conditions.

12.2 Operating Temperature

Characteristic	Symbol	Value	Unit
Operating temperature range	T_A	–40 to +85	°C

12.3 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance plastic dual in-line (PDIP)	θ_{JA}	60	°C/W
Thermal resistance plastic leaded chip carrier (PLCC)	θ_{JA}	70	°C/W
Thermal resistance quad flat pack (QFP)	θ_{JA}	95	°C/W
Thermal resistance plastic shrink DIP (SDIP)	θ_{JA}	60	°C/W

12.6 3.3-Vdc Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	V_{OL} V_{OH}	— V_{DD} –0.1	— —	0.1 —	V
Output high voltage (I_{Load} = –0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP, PD7, PD0 (I_{Load} = –0.4 mA) PD5–PD1 (I_{Load} = –1.5 mA) PC7	V_{OH}	V_{DD} –0.3 V_{DD} –0.3 V_{DD} –0.3	— — —	— — —	V
Output low voltage (I_{Load} = 0.4mA) PA7–PA0, PB7–PB0, PC6–PC0, PD7, PD5–PD0, TCMP (I_{Load} = 6 mA) PC7	V_{OL}	— —	— —	0.3 0.3	V
Input high voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current (3.0–3.6 Vdc @ f_{OP} = 1.0 MHz) Run[3] Wait[4] Stop[5] 25°C –40 to 85°C	I_{DD}	 — — — —	 1.0 500 1.0 2.5	 1.6 900 8 20	 mA µA µA µA
I/O ports hi-Z leakage current PA7–PA0, PB7–PB0 (without pullup) PC7–PC0, PD7, PD5–PD0	I_{OZ}	—	—	10	µA
Input current $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5–PD0	I_{In}	—	—	1	µA
Input pullup current[6] PB7–PB0 (with pullup)	I_{In}	0.5	—	20	µA
Capacitance Ports (as input or output) $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5, PD0	C_{Out} C_{In}	— —	— —	12 8	pF

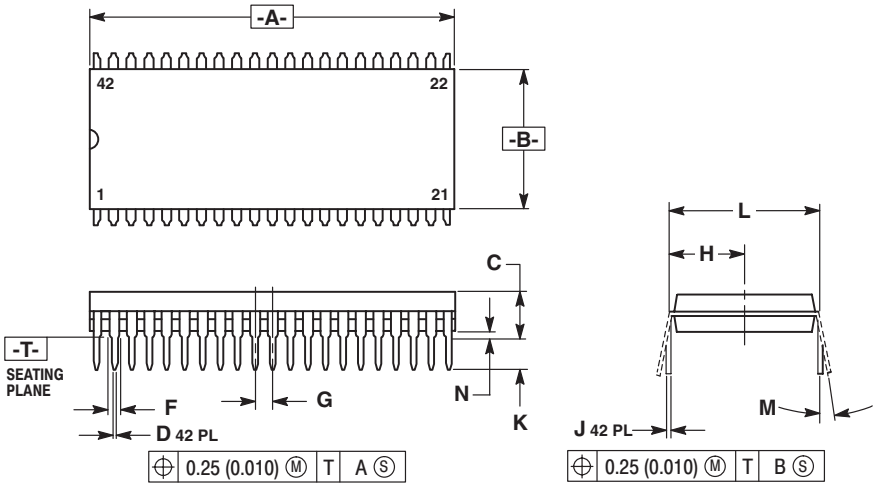
1. V_{DD} = 3.3 Vdc ± 0.3 Vdc, V_{SS} = 0 Vdc, T_A = –40 to +85 °C, unless otherwise noted
2. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.
5. Stop I_{DD} measured with OSC1 = 0.2 V; all I/O pins configured as inputs, port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V.
6. Input pullup current measured with V_{IL} = 0.2 V.

12.9 5.0-Vdc Serial Peripheral Interface Timing

No.	Characteristic[1]	Symbol	Min	Max	Unit
	Operating frequency Master Slave	 $f_{OP(M)}$ $f_{OP(S)}$	 dc dc	 0.5 2.1	f_{OP} MHz
1	Cycle time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 480	 — —	t_{CYC} ns
2	Enable lead time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 (2) 240	 — —	ns
3	Enable lag time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 (2) 720	 — —	ns
4	Clock (SCK) high time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 340 190	 — —	ns
5	Clock (SCK) low time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 340 190	 — —	ns
6	Data setup time (inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 100 100	 — —	ns
7	Data hold time (inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 100 100	 — —	ns
8	Slave access time (time to data active from high-impedance state)	t_A	0	120	ns
9	Slave disable time (hold time to high-impedance state)	t_{DIS}	—	240	ns
10	Data valid Master (before capture edge) Slave (after enable edge)[3]	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 240	 $t_{CYC(M)}$ ns
11	Data hold time (outputs) Master (after capture edge) slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
12	Rise time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI outputs (SCK, MOSI, and MISO) SPI inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 100 2.0	 ns µs
13	Fall time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI outputs (SCK, MOSI, and MISO) SPI inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 100 2.0	 ns µs

1. V_{DD} = 5.0 Vdc ± 10%; V_{SS} = 0 Vdc, T_A = –40 to +85°C, unless otherwise noted. Refer to Figure 12-9 and Figure 12-10.
2. Signal production depends on software.
3. Assumes 200 pF load on all SPI pins.

13.3 42-Pin Plastic Shrink Dual In-Line (SDIP) Package (Case 858-01)



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure 13-2. 42-Pin Plastic SDIP Package (Case 858-01)

Appendix A
EPROM Programming

A.1 Introduction

This section describes programming of the EPROM.

A.2 Bootloader Mode

Table A-1. Operating Modes

$\overline{\text{RESET}}$	$\overline{\text{IRQ}}$	TCAP	Mode
	V_{SS} to V_{DD} V_{TST}	V_{SS} to V_{DD} V_{DD}	User Bootloader

Bootloader mode is entered upon the rising edge of $\overline{\text{RESET}}$ if the $\overline{\text{IRQ}}$ is at V_{TST} and the TCAP pin is at logic one. The bootloader code resides in the ROM from $3F00 to $3FEF. This program handles copying of user code from an external EPROM into the on-chip EPROM. The bootload function does not have to be done from an external EPROM, but it may be done from a host.

The user code must be a one-to-one correspondence with the internal EPROM addresses.

A.3 Bootloader Functions

Three pins are used to select various bootloader functions: PD5, PD4, and PD3. Two other pins, PC6 and PC7, are used to drive the PROG LED and the VERF LED, respectively. The programming modes are shown in Table A-2.

Table A-2. Bootloader Functions

PD5	PD4	PD3	Mode
0	0	0	Program/verify
0	0	1	Verify only
0	1	0	Load RAM and execute
1	X	X	Secure