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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8255acvvmhbb

- — 32-bit address decodes with programmable bank size
- — Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
- — Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
- — Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - — Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - — Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - — Serial DMA channels for receive and transmit on all serial channels
  - — Parallel I/O registers with open-drain and interrupt capability
  - — Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - — Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
    - – 10/100-Mbit Ethernet/IEEE Std. 802.3® CDMA/CS interface through media independent interface (MII)
    - – ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
    - – Transparent
    - – HDLC—Up to T3 rates (clear channel)
  - — Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
    - – Each MCC handles 128 serial, full-duplex, 64-Kbps data channels.Each MCC can be split into four subgroups of 32 channels each.
    - – Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - — Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - – Ethernet/IEEE 802.3 CDMA/CS
    - – HDLC/SDLC and HDLC bus
    - – Universal asynchronous receiver transmitter (UART)
    - – Synchronous UART
    - – Binary synchronous (BISYNC) communications
    - – Transparent
  - — Two serial management controllers (SMCs), identical to those of the MPC860
    - – Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

- Coset removing (programmable by the user)

- Filtering idle/unassigned cells (programmable by the user)

- Performing HEC error detection and single bit error correction (programmable by user)

- Generating loss of cell delineation status/interrupt (LOC/LCD)

— Operates with FCC2 (UTOPIA 8)

— Provides serial loop back mode

— Cell echo mode is provided

— Supports both FCC transmit modes

   – External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.

   – Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.

— Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)

— Cell counters for performance monitoring

   – 16-bit counters count

     - HEC error cells

     - HEC single bit error and corrected cells

     - Idle/unassigned cells filtered

     - Idle/unassigned cells transmitted

     - Transmitted ATM cells

     - Received ATM cells

   – Maskable interrupt is sent to the host when a counter expires

— Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt

— May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported

- PCI bridge (MPC8265 and MPC8266 only)

— PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz

— On-chip arbitration

— Support for PCI to 60x memory and 60x memory to PCI streaming

— PCI Host Bridge or Peripheral capabilities

— Includes 4 DMA channels for the following transfers:

   – PCI-to-60x to 60x-to-PCI

   – 60x-to-PCI to PCI-to-60x

   – PCI-to-60x to PCI-to-60x

   – 60x-to-PCI to 60x-to-PCI

— Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265) required by the PCI standard as well as message and doorbell registers

— Supports the I$_2$O standard

— Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)

— Support for 66 MHz, 3.3 V specification

— 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port

— Makes use of the local bus signals, so there is no need for additional pins

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC826xA.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC826xA. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	–0.3 – 2.5	V
PLL supply voltage[2]	VCCSYN	–0.3 – 2.5	V
I/O supply voltage[3]	VDDH	–0.3 – 4.0	V
Input voltage[4]	VIN	GND(–0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(–55) – (+150)	°C

[1] Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

[2] **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

[3] **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

[4] **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA $\overline{CS}$[0-9] $\overline{CS}$(10)/$\overline{BCTL1}$ $\overline{CS}$(11)/$\overline{AP}$(0) BADDR[27–28] $\overline{ALE}$ $\overline{BCTL0}$ $\overline{PWE}$(0:7)/$\overline{PSDDQM}$(0:7)/$\overline{PBS}$(0:7) PSDA10/PGPL0 $\overline{PSDWE}$/PGPL1 $\overline{POE}$/$\overline{PSDRAS}$/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 $\overline{LWE}$[0–3]$\overline{LSDDQM}$[0–3]/$\overline{LBS}$[0–3]/PCI_CFG[0–3][3] LSDA10/LGPL0/PCI_MODCKH0[3] LSDWE/LGPL1/PCI_MODCKH1[3] $\overline{LOE}$/$\overline{LSDRAS}$/LGPL2/PCI_MODCKH2[3] LSDCAS/LGPL3/PCI_MODCKH3[3] LGTA/LUPMWAIT/LGPL4/$\overline{LPBS}$ LSDAMUX/LGPL5/PCI_MODCK[3] $\overline{LWR}$ MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2) I_{OL} = 3.2mA L_A14/PAR[3] L_A15/$\overline{FRAME}$[3]/$\overline{SMI}$ L_A16/$\overline{TRDY}$[3] L_A17/$\overline{IRDY}$[3]/CKSTP_OUT L_A18/$\overline{STOP}$[3] L_A19/$\overline{DEVSEL}$[3] L_A20/IDSEL[3] L_A21/$\overline{PERR}$[3] L_A22/$\overline{SERR}$[3] L_A23/$\overline{REQ0}$[3] L_A24/$\overline{REQ1}$[3]/HSEJSW[3] L_A25/$\overline{GNT0}$[3] L_A26/$\overline{GNT1}$[3]/HSLED[3] L_A27/$\overline{GNT2}$[3]/HSENUM[3] L_A28/$\overline{RST}$[3]/CORE_SRESET L_A29/$\overline{INTA}$[3] L_A30/$\overline{REQ2}$[3] L_A31 LCL_D(0-31)/AD(0-31)[3] LCL_DP(0-3)/C/$\overline{BE}$(0-3)[3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO	V_{OL}	—	0.4	V

[1] The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

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Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.
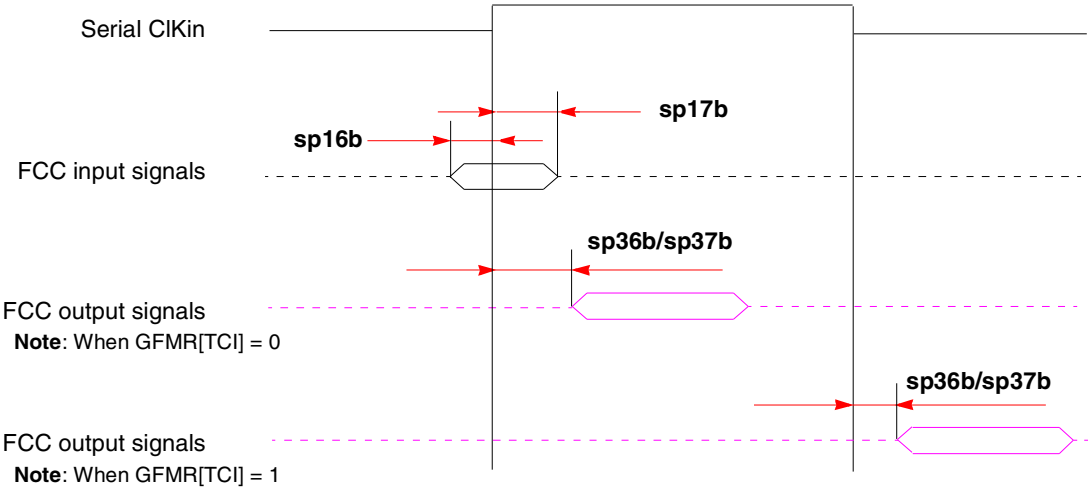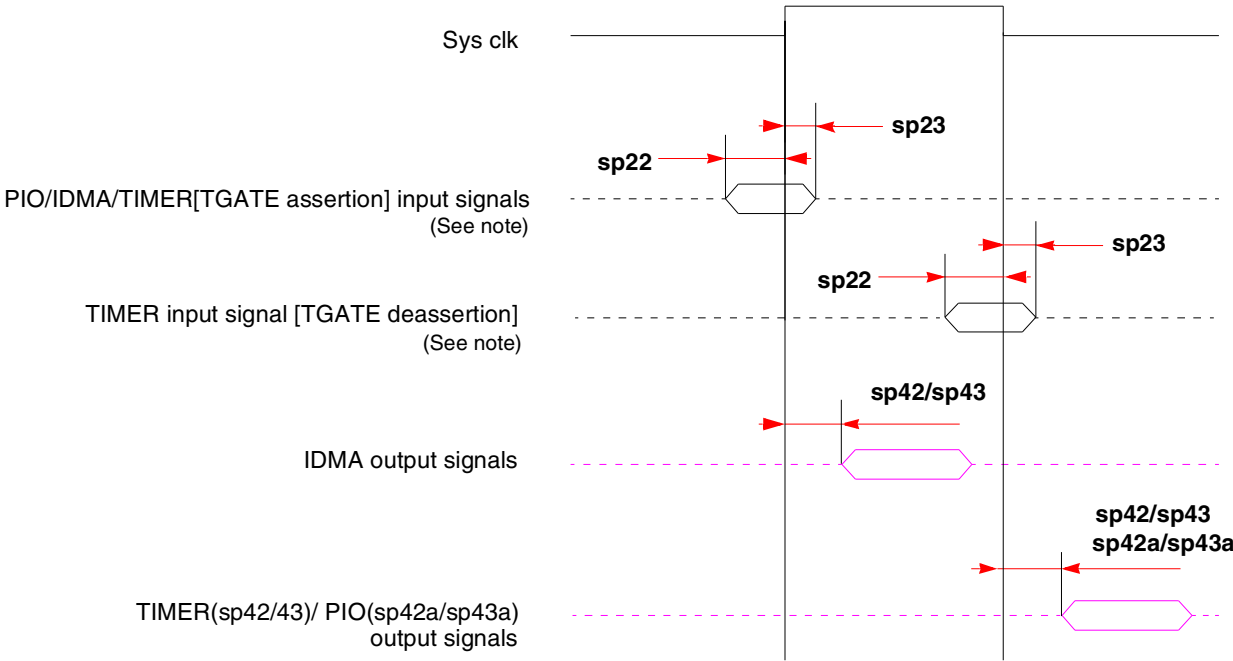
Figure 3 shows the FCC external clock.

Figure 3. FCC External Clock Diagram

Figure 8 shows PIO, timer, and DMA signals.

Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 10 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	AACK/ARTRY/TA/TS/TEA/DBG/BG/BR	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

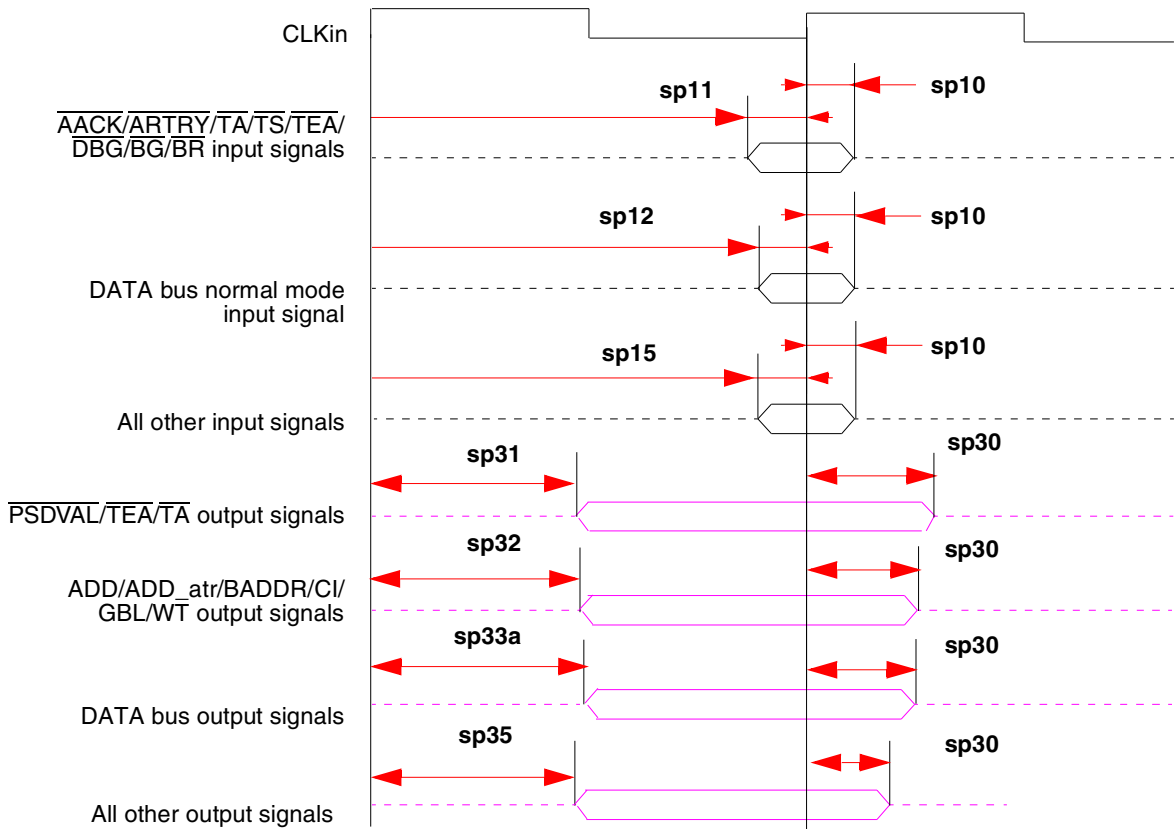Figure 9 shows the interaction of several bus signals.

Figure 9. Bus Signals

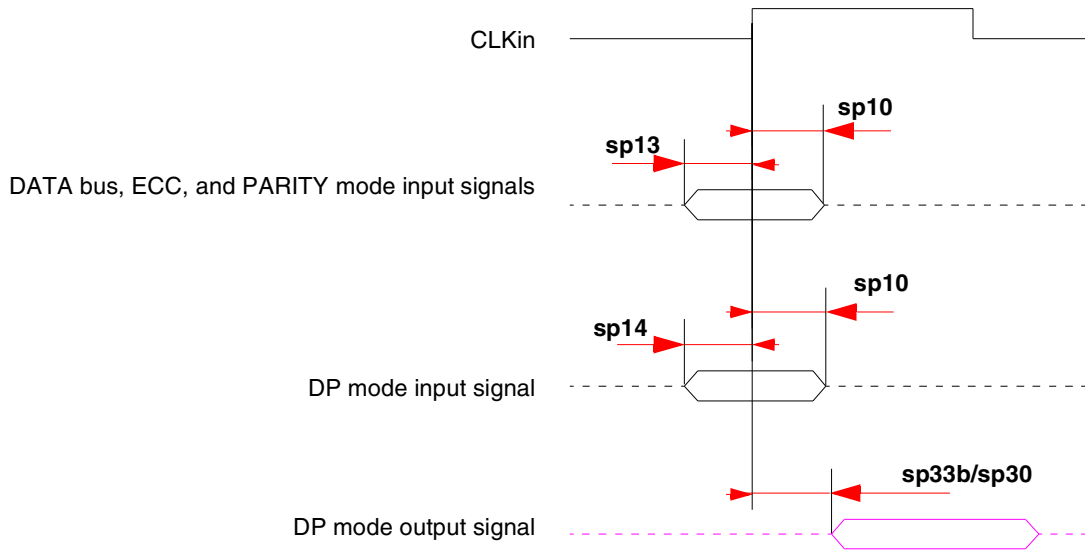Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

Figure 10. Parity Mode Diagram

Table 12 lists the JTAG timings.

Table 12. JTAG Timings[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	25	MHz	—
JTAG external clock cycle time	t_{JTG}	40	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	20	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	6
TRST assert time	t_{TRST}	25	—	ns	3, 6
Input setup times Boundary-scan data	t_{JTDVKH}	4	—	ns	4, 7
TMS, TDI	t_{JTIVKH}	4	—	ns	4, 7
Input hold times Boundary-scan data	t_{JTDXKH}	10	—	ns	4, 7
TMS, TDI	t_{JTIXKH}	10	—	ns	4, 7
Output valid times Boundary-scan data	t_{JTKLDV}	—	25	ns	5, 7
TDO	t_{JTKLOV}	—	25	ns	5. 7
Output hold times Boundary-scan data	t_{JTKLDX}	1	—	ns	5, 7
TDO	t_{JTKLOX}	1	—	ns	5, 7
JTAG external clock to output high impedance Boundary-scan data	t_{JTKLDZ}	1	25	ns	5, 6
TDO	t_{JTKLOZ}	1	25	ns	5, 6

[1] All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

[2] The symbols used for timing specifications herein follow the pattern of t(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t((first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

[3] TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

[4] Non-JTAG signal input timing with respect to t_{TCLK}.

[5] Non-JTAG signal output timing with respect to t_{TCLK}.

[6] Guaranteed by design.

[7] Guaranteed by design and device characterization.

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000) (continued)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

[1] Assumes MODCK_HI = 0000.
[2] The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.
[3] Core frequency = (60x bus frequency)(core multiplication factor)
[4] Bus frequency = CPM frequency/bus division factor

Table 19 describes all possible clock configurations when using the MPC8265 or the MPC8266's internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	**150 MHz**	3	180 MHz	2.5	**60 MHz**
0010_010	50/25 MHz	3/6	**150 MHz**	3.5	210 MHz	2.5	**60 MHz**
0010_011	50/25 MHz	3/6	**150 MHz**	4	240 MHz	2.5	**60 MHz**
0010_100	50/25 MHz	3/6	**150 MHz**	4.5	270 MHz	2.5	**60 MHz**
0011_000	66/33 MHz	2/4	**133 MHz**	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	**133 MHz**	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	**133 MHz**	3.5	154 MHz	3	**44 MHz**
0011_011	66/33 MHz	2/4	**133 MHz**	4	176MHz	3	**44 MHz**
0011_100	66/33 MHz	2/4	**133 MHz**	4.5	198 MHz	3	**44 MHz**
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	**3**	66 MHz
0100_001	66/33 MHz	3/6	**200 MHz**	3	200 MHz	**3**	**66 MHz**
0100_010	66/33 MHz	3/6	**200 MHz**	3.5	233 MHz	**3**	**66 MHz**
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**

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Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

[1] The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.

[2] Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

[3] Core frequency = (60x bus frequency)(core multiplication factor)

[4] Bus frequency = CPM frequency/bus division factor

[5] In this mode, PCI_MODCK must be "1".

4 Pinout

This section provides the pin assignments and pinout list for the MPC826xA.

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC826xA's 480 TBGA package as viewed from the top surface.

Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

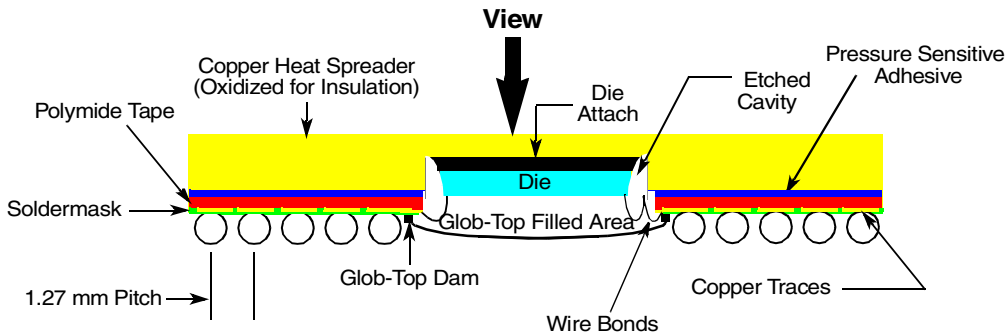Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

Table 21. Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2

Table 21. Pinout List (continued)

Pin Name	Ball
$\overline{\text{IRQ3}}$/DP3/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	D21
$\overline{\text{IRQ4}}$/DP4/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	C21
$\overline{\text{IRQ5}}$/DP5/$\overline{\text{TBEN}}$/$\overline{\text{EXT\_DBG3}}$	B21
$\overline{\text{IRQ6}}$/DP6/CSE0	A21
$\overline{\text{IRQ7}}$/DP7/CSE1	E20
PSDVAL	V3
TA	C22
TEA	V5
GBL/IRQ1	W1
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	U2
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$	U3
L2_HIT/IRQ4	Y4
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
$\overline{\text{CS10}}$/BCTL1	F29
$\overline{\text{CS11}}$/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24

Table 21. Pinout List (continued)

Pin Name	Ball
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
$\overline{\text{PSDWE}}$/PGPL1	B24
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2	A24
$\overline{\text{PSDCAS}}$/PGPL3	B23
$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/$\overline{\text{LBS0}}$/PCI_CFG0[1]	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1[1]	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2[1]	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3[1]	G29
LSDA10/LGPL0/PCI_MODCKH0[1]	D27
$\overline{\text{LSDWE}}$/LGPL1/PCI_MODCKH1[1]	C28
$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$/LGPL2/PCI_MODCKH2[1]	E26
$\overline{\text{LSDCAS}}$/LGPL3/PCI_MODCKH3[1]	D25
$\overline{\text{LGTA}}$/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$	C26
LGPL5/LSDAMUX/PCI_MODCK[1]	B27
LWR	D28
L_A14/PAR[1]	N27
L_A15/$\overline{\text{FRAME}}$[1]/$\overline{\text{SMI}}$	T29
L_A16/$\overline{\text{TRDY}}$[1]	R27
L_A17/$\overline{\text{IRDY}}$[1]/$\overline{\text{CKSTP\_OUT}}$	R26
L_A18/$\overline{\text{STOP}}$[1]	R29
L_A19/$\overline{\text{DEVSEL}}$[1]	R28
L_A20/IDSEL[1]	W29
L_A21/$\overline{\text{PERR}}$[1]	P28
L_A22/$\overline{\text{SERR}}$[1]	N26
L_A23/$\overline{\text{REQ0}}$[1]	AA27
L_A24/$\overline{\text{REQ1}}$[1]/HSEJSW[1]	P29
L_A25/$\overline{\text{GNT0}}$[1]	AA26
L_A26/$\overline{\text{GNT1}}$[1]/HSLED[1]	N25
L_A27/$\overline{\text{GNT2}}$[1]/$\overline{\text{HSENUM}}$[1]	AA25

Table 21. Pinout List (continued)

Pin Name	Ball
LCL_D31/AD31[1]	AA28
LCL_DP0/C0[1]/$\overline{BE0}$[1]	L28
LCL_DP1/C1[1]/$\overline{BE1}$[1]	N28
LCL_DP2/C2[1]/$\overline{BE2}$[1]	T28
LCL_DP3/C3[1]/$\overline{BE3}$[1]	W28
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
$\overline{TRST}$	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
$\overline{PORESET}$	AG6
$\overline{HRESET}$	AH5
$\overline{SRESET}$	AF6
$\overline{QREQ}$	AA3
$\overline{RSTCONF}$	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{RESTART1}$/DREQ3/FCC2_UTM_TXADDR2	AC29[2]
PA1/$\overline{REJECT1}$/FCC2_UTM_TXADDR1/$\overline{DONE3}$	AC25[2]
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{DACK3}$	AE28[2]
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{DACK4}$/L1RXD1A2	AG29[2]
PA4/$\overline{REJECT2}$/FCC2_UTM_RXADDR1/$\overline{DONE4}$	AG28[2]
PA5/$\overline{RESTART2}$/DREQ4/FCC2_UTM_RXADDR2	AG26[2]
PA6/L1RSYNCA1	AE24[2]
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2/L1TXD0A1	AH23[2]
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22[2]
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22[2]

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Table 21. Pinout List (continued)

Pin Name	Ball
PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14[2]
PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13[2]
PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12[2]
PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2/L1TXD2A1	AH11[2]
PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_TXD/L1RXD1A1/L1RXDD2	AH16[2]
PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1TXDD2	AE15[2]
PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2	AJ9[2]
PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9[2]
PB26/FCC2_MII_CRS/FCC2_UT8_TXD1/L1RXDC2	AJ7[2]
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6[2]
PB28/FCC2_MII_RX_ER/$\overline{FCC2\_RTS}$/L1TSYNCB2/L1GNTB2/TXD1	AE3[2]
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/FCC2_MII_TX_EN	AE2[2]
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2	AC5[2]
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4[2]
PC0/DREQ1/BRGO7/$\overline{SMSYN2}$/L1CLKOA2	AB26[2]
PC1/DREQ2/BRGO6/$\overline{L1RQA2}$	AD29[2]
PC2/$\overline{FCC3\_CD}$/FCC2_UT8_TXD3/$\overline{DONE2}$	AE29[2]
PC3/$\overline{FCC3\_CTS}$/FCC2_UT8_TXD2/$\overline{DACK2}$/$\overline{CTS4}$	AE27[2]
PC4/$\overline{FCC2\_UTM\_RXENB}$/$\overline{FCC2\_UTS\_RXENB}$/SI2_L1ST4/$\overline{FCC2\_CD}$	AF27[2]
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/$\overline{FCC2\_CTS}$	AF24[2]
PC6/$\overline{FCC1\_CD}$/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR/FCC1_UTM_RXCLAV1	AJ26[2]
PC7/$\overline{FCC1\_CTS}$/L1RQC1/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/FCC1_UTM_TXCLAV1	AJ25[2]
PC8/$\overline{CD4}$/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/$\overline{CTS3}$	AF22[2]
PC9/$\overline{CTS4}$/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21[2]
PC10/$\overline{CD3}$/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AF20[2]
PC11/$\overline{CTS3}$/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19[2]
PC12/$\overline{CD2}$/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18[2]
PC13/$\overline{CTS2}$/CLSN2/$\overline{L1RQD1}$/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18[2]
PC14/$\overline{CD1}$/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17[2]
PC15/$\overline{CTS1}$/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16[2]

Table 21. Pinout List (continued)

Pin Name	Ball
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13[2]
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12[2]
PD23/$\overline{\text{RTS3}}$/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12[2]
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10[2]
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9[2]
PD26/$\overline{\text{RTS2}}$/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8[2]
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7[2]
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4[2]
PD29/$\overline{\text{RTS1}}$/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4	AG1[2]
PD30/$\overline{\text{FCC2\_UTM\_TXENB}}$/$\overline{\text{FCC2\_UTS\_TXENB}}$/TXD1	AD4[2]
PD31/RXD1	AD2[2]
VCCSYN	AB3
VCCSYN1	B9
GNDSYN	AB1
CLKIN2[1,3]	AE11
SPARE4[4]	U5
$\overline{\text{PCI\_MODE}}$[1,5]	AF25
SPARE6[4]	V4
THERMAL0[6]	AA1
THERMAL1[6]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 MPC8265 and MPC8266 only.

2 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC826xA. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.
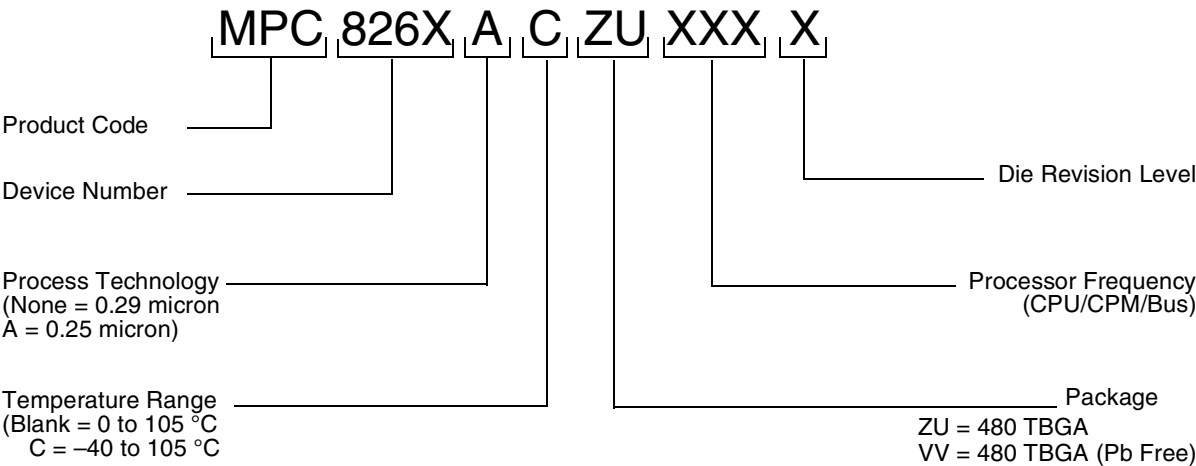
Figure 16. Freescale Part Number Key

7 Document Revision History

Table 23 lists significant changes in each revision of this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
2	06/2009	• Updated package values in Figure 16.
1.1	02/2006	• Addition of Table 12.
1.0	9/2005	• Document template update

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