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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	200MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8260aczumibb

  - PowerPC architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPs/MHz without inlining and 1.90 Dhrystones MIPS/MHz with
  - Supports bus snooping for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge (MPC8265 and MPC8266 only)
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE Std. 1149.1™ standard JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation

  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
    - 10/100-Mbit Ethernet/IEEE Std. 802.3® CDMA/CS interface through media independent interface (MII)
    - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
    - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels.Each MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

- Coset removing (programmable by the user)
- Filtering idle/unassigned cells (programmable by the user)
- Performing HEC error detection and single bit error correction (programmable by user)
- Generating loss of cell delineation status/interrupt (LOC/LCD)

— Operates with FCC2 (UTOPIA 8)
— Provides serial loop back mode
— Cell echo mode is provided
— Supports both FCC transmit modes
  – External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
  – Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.
— Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
— Cell counters for performance monitoring
  – 16-bit counters count
    - HEC error cells
    - HEC single bit error and corrected cells
    - Idle/unassigned cells filtered
    - Idle/unassigned cells transmitted
    - Transmitted ATM cells
    - Received ATM cells
  – Maskable interrupt is sent to the host when a counter expires
— Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
— May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported

- PCI bridge (MPC8265 and MPC8266 only)
  — PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  — On-chip arbitration
  — Support for PCI to 60x memory and 60x memory to PCI streaming
  — PCI Host Bridge or Peripheral capabilities
  — Includes 4 DMA channels for the following transfers:
    – PCI-to-60x to 60x-to-PCI
    – 60x-to-PCI to PCI-to-60x
    – PCI-to-60x to PCI-to-60x
    – 60x-to-PCI to 60x-to-PCI
  — Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265) required by the PCI standard as well as message and doorbell registers
  — Supports the I_2O standard

— Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
— Support for 66 MHz, 3.3 V specification
— 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
— Makes use of the local bus signals, so there is no need for additional pins

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC826xA.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC826xA. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	–0.3 – 2.5	V
PLL supply voltage[2]	VCCSYN	–0.3 – 2.5	V
I/O supply voltage[3]	VDDH	–0.3 – 4.0	V
Input voltage[4]	VIN	GND(–0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(–55) – (+150)	°C

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.
2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.
3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.
4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions[1]

Rating	Symbol	Value			Unit
Core supply voltage	VDD	1.7 – 1.9[2]	1.7–2.1[3]	1.9 –2.2[4]	V
PLL supply voltage	VCCSYN	1.7 – 1.9[2]	1.7–2.1[3]	1.9–2.2[4]	V
I/O supply voltage	VDDH	3.135 – 3.465			V
Input voltage	VIN	GND (–0.3) – 3.465			V
Junction temperature (maximum)	T_j	105[5]			°C
Ambient temperature	T_A	0–70[5]			°C

1 **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.
2 CPU frequency less than or equal to 200 MHz.
3 CPU frequency greater than 200 MHz but less than 233 MHz.
4 CPU frequency greater than or equal to 233 MHz.
5 Note that for extended temperature parts the range is $(-40)_{T_A} – 105_{T_j}$.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (–5% and –0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

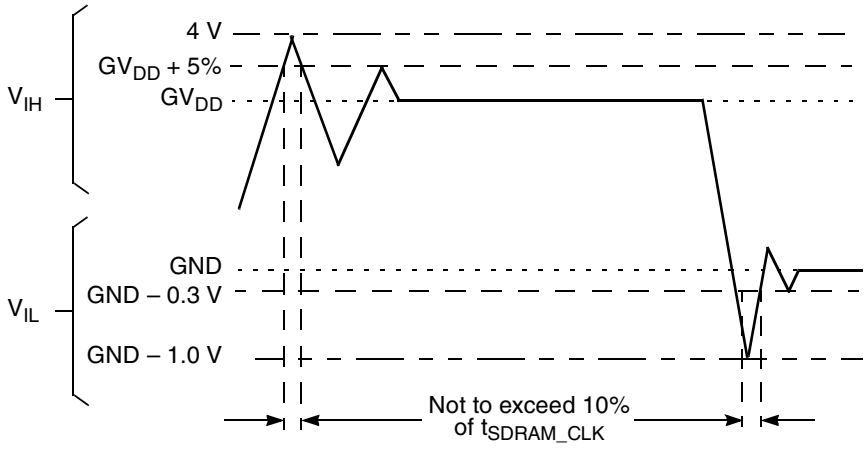


Figure 2. Overshoot/Undershoot Voltage

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3][3] LSDA10/LGPL0/PCI_MODCKH0[3] LSDWE/LGPL1/PCI_MODCKH1[3] LOE/LSDRAS/LGPL2/PCI_MODCKH2[3] LSDCAS/LGPL3/PCI_MODCKH3[3] LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK[3] LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2)	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR[3] L_A15/FRAME[3]/SMI L_A16/TRDY[3] L_A17/IRDY[3]/CKSTP_OUT L_A18/STOP[3] L_A19/DEVSEL[3] L_A20/IDSEL[3] L_A21/PERR[3] L_A22/SERR[3] L_A23/REQ0[3] L_A24/REQ1[3]/HSEJSW[3] L_A25/GNT0[3] L_A26/GNT1[3]/HSLED[3] L_A27/GNT2[3]/HSENUM[3] L_A28/RST[3]/CORE_SRESET L_A29/INTA[3] L_A30/REQ2[3] L_A31 LCL_D(0-31)/AD(0-31)[3] LCL_DP(0-3)/C/BE(0-3)[3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO				

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

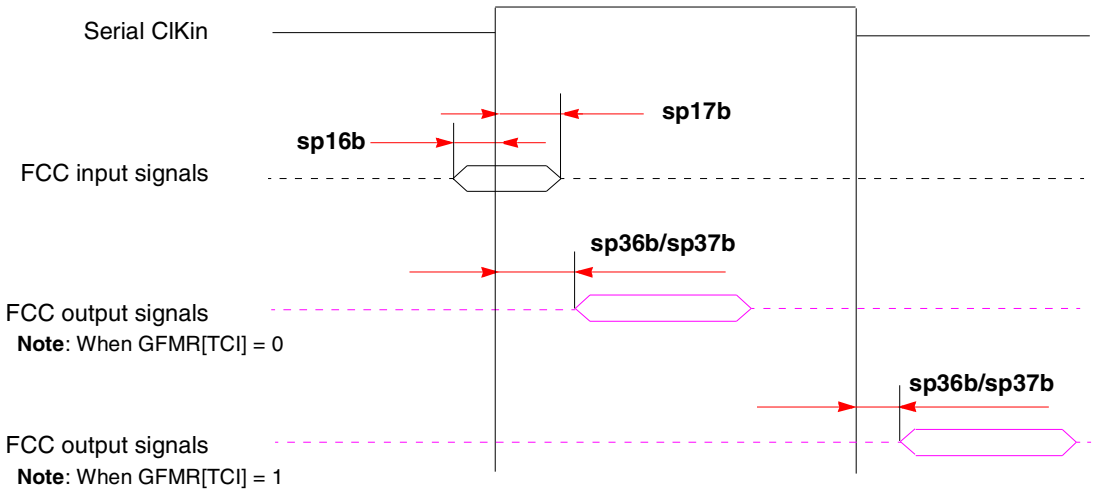
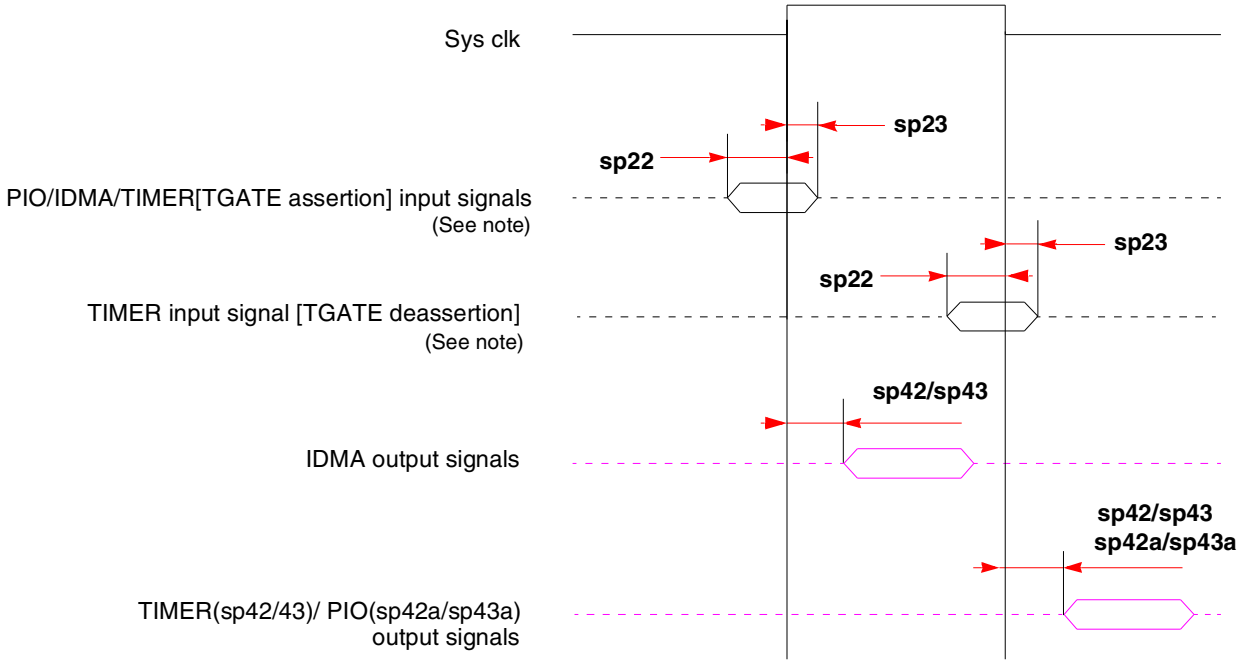


Figure 3. FCC External Clock Diagram

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 10 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	$\overline{\text{AACK}}/\overline{\text{ARTRY}}/\overline{\text{TA}}/\overline{\text{TS}}/\overline{\text{TEA}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}$	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 11 shows signal behavior in MEMC mode.

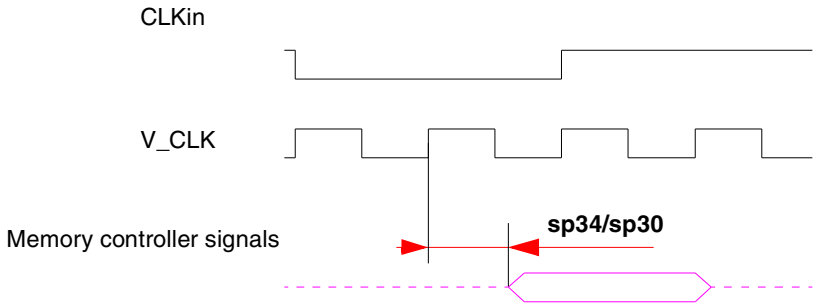


Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC826xA bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 12 is a graphical representation of Table 11.

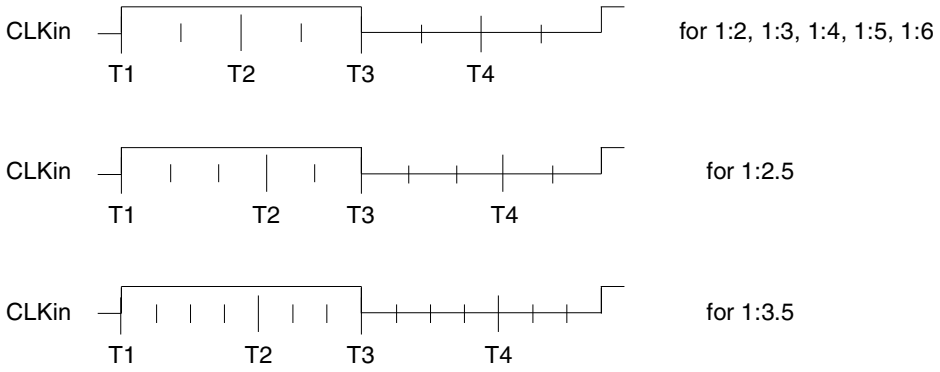


Figure 12. Internal Tick Spacing for Memory Controller Signals

Table 14. Clock Configuration Modes[1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	**33 MHz**	**4**	**133 MHz**	**4**	**133 MHz**
0010_011	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					

3.2.1 PCI Host Mode

The frequencies listed in Table 16 and Table 17 are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 16. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

1 Assumes MODCK_HI = 0000.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to Table 15.

Table 17 describes all possible clock configurations when using the MPC8265's or the MPC8266's internal PCI bridge in host mode.

Table 17. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**	**4/8**	**33**/16 **MHz**
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000[3]	33 MHz	5	166 MHz	5	166 MHz	5	**33 MHz**
0011_001[3]	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz
0011_010[3]	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000[5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

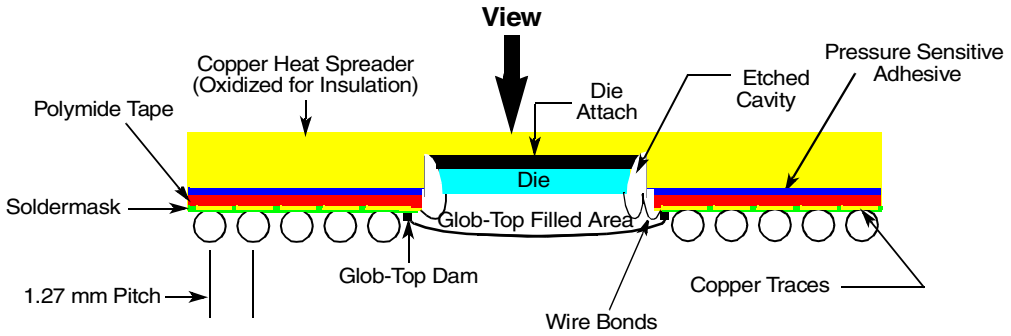


Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

Table 21. Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2

Table 21. Pinout List (continued)

Pin Name	Ball
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	E21

Table 21. Pinout List (continued)

Pin Name	Ball
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
$\overline{\text{PSDWE}}$/PGPL1	B24
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2	A24
$\overline{\text{PSDCAS}}$/PGPL3	B23
$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/$\overline{\text{LBS0}}$/PCI_CFG0[1]	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1[1]	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2[1]	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3[1]	G29
LSDA10/LGPL0/PCI_MODCKH0[1]	D27
$\overline{\text{LSDWE}}$/LGPL1/PCI_MODCKH1[1]	C28
$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$/LGPL2/PCI_MODCKH2[1]	E26
$\overline{\text{LSDCAS}}$/LGPL3/PCI_MODCKH3[1]	D25
$\overline{\text{LGTA}}$/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$	C26
LGPL5/LSDAMUX/PCI_MODCK[1]	B27
LWR	D28
L_A14/PAR[1]	N27
L_A15/$\overline{\text{FRAME}}$[1]/$\overline{\text{SMI}}$	T29
L_A16/$\overline{\text{TRDY}}$[1]	R27
L_A17/$\overline{\text{IRDY}}$[1]/$\overline{\text{CKSTP\_OUT}}$	R26
L_A18/$\overline{\text{STOP}}$[1]	R29
L_A19/$\overline{\text{DEVSEL}}$[1]	R28
L_A20/IDSEL[1]	W29
L_A21/$\overline{\text{PERR}}$[1]	P28
L_A22/$\overline{\text{SERR}}$[1]	N26
L_A23/$\overline{\text{REQ0}}$[1]	AA27
L_A24/$\overline{\text{REQ1}}$[1]/HSEJSW[1]	P29
L_A25/$\overline{\text{GNT0}}$[1]	AA26
L_A26/$\overline{\text{GNT1}}$[1]/HSLED[1]	N25
L_A27/$\overline{\text{GNT2}}$[1]/$\overline{\text{HSENUM}}$[1]	AA25

Table 21. Pinout List (continued)

Pin Name	Ball
L_A28/$\overline{\text{RST}}$[1]/$\overline{\text{CORE\_SRESET}}$	AB29
L_A29/$\overline{\text{INTA}}$[1]	AB28
L_A30/$\overline{\text{REQ2}}$[1]	P25
L_A31/DLLOUT[1]	AB27
LCL_D0/AD0[1]	H29
LCL_D1/AD1[1]	J29
LCL_D2/AD2[1]	J28
LCL_D3/AD3[1]	J27
LCL_D4/AD4[1]	J26
LCL_D5/AD5[1]	J25
LCL_D6/AD6[1]	K25
LCL_D7/AD7[1]	L29
LCL_D8/AD8[1]	L27
LCL_D9/AD9[1]	L26
LCL_D10/AD10[1]	L25
LCL_D11/AD11[1]	M29
LCL_D12/AD12[1]	M28
LCL_D13/AD13[1]	M27
LCL_D14/AD14[1]	M26
LCL_D15/AD15[1]	N29
LCL_D16/AD16[1]	T25
LCL_D17/AD17[1]	U27
LCL_D18/AD18[1]	U26
LCL_D19/AD19[1]	U25
LCL_D20/AD20[1]	V29
LCL_D21/AD21[1]	V28
LCL_D22/AD22[1]	V27
LCL_D23/AD23[1]	V26
LCL_D24/AD24[1]	W27
LCL_D25/AD25[1]	W26
LCL_D26/AD26[1]	W25
LCL_D27/AD27[1]	Y29
LCL_D28/AD28[1]	Y28
LCL_D29/AD29[1]	Y25
LCL_D30/AD30[1]	AA29

Table 21. Pinout List (continued)

Pin Name	Ball
LCL_D31/AD31[1]	AA28
LCL_DP0/C0[1]/$\overline{\text{BE0}}$[1]	L28
LCL_DP1/C1[1]/$\overline{\text{BE1}}$[1]	N28
LCL_DP2/C2[1]/$\overline{\text{BE2}}$[1]	T28
LCL_DP3/C3[1]/$\overline{\text{BE3}}$[1]	W28
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3/FCC2_UTM_TXADDR2	AC29[2]
PA1/$\overline{\text{REJECT1}}$/FCC2_UTM_TXADDR1/$\overline{\text{DONE3}}$	AC25[2]
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{\text{DACK3}}$	AE28[2]
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{\text{DACK4}}$/L1RXD1A2	AG29[2]
PA4/$\overline{\text{REJECT2}}$/FCC2_UTM_RXADDR1/$\overline{\text{DONE4}}$	AG28[2]
PA5/$\overline{\text{RESTART2}}$/DREQ4/FCC2_UTM_RXADDR2	AG26[2]
PA6/L1RSYNCA1	AE24[2]
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2/L1TXD0A1	AH23[2]
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22[2]
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22[2]

Table 21. Pinout List (continued)

Pin Name	Ball
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21[2]
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20[2]
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19[2]
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18[2]
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17[2]
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16[2]
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16[2]
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15[2]
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13[2]
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13[2]
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12[2]
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11[2]
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9[2]
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8[2]
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7[2]
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7[2]
PA28/$\overline{\text{FCC1\_UTM\_RXENB}}$/$\overline{\text{FCC1\_UTS\_RXENB}}$/FCC1_MII_TX_EN	AD5[2]
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1[2]
PA30/$\overline{\text{FCC1\_UTM\_TXCLAV}}$/FCC1_UTS_TXCLAV/FCC1_MII_CRS/ $\overline{\text{FCC1\_RTS}}$	AD3[2]
PA31/$\overline{\text{FCC1\_UTM\_TXENB}}$/$\overline{\text{FCC1\_UTS\_TXENB}}$/FCC1_MII_COL	AB5[2]
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	AD28[2]
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26[2]
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25[2]
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26[2]
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27[2]
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24[2]
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24[2]
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22[2]
PB13/FCC3_MII_COL/$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21[2]
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19[2]
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18[2]
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17[2]

Table 21. Pinout List (continued)

Pin Name	Ball
PC16/CLK16/TIN4	AF15[2]
PC17/CLK15/TIN3/BRGO8	AJ15[2]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[2]
PC19/CLK13/BRGO7/SPICLK	AG13[2]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[2]
PC21/CLK11/BRGO6	AJ11[2]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[2]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[2]
PC24/FCC2_UT8_TXD3/CLK8/$\overline{\text{TOUT4}}$	AF9[2]
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8[2]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[2]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[2]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[2]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[2]
PC30/FCC2_UT8_TXD3/CLK2/$\overline{\text{TOUT1}}$	AE1[2]
PC31/CLK1/BRGO1	AD1[2]
PD4/BRGO8/L1TSYNCD1/L1GNTD1/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[2]
PD5/FCC1_UT16_TXD3/$\overline{\text{DONE1}}$	AD27[2]
PD6/FCC1_UT16_TXD4/$\overline{\text{DACK1}}$	AF29[2]
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4/FCC1_TXCLAV2	AF28[2]
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25[2]
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26[2]
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27[2]
PD11/$\overline{\text{L1RQB2}}$/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23[2]
PD12/SI1_L1ST2/L1RXDB1	AG23[2]
PD13/SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20[2]
PD15/FCC1_UT16_RXD1/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[2]
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18[2]
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17[2]
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/FCC2_UTM_RXADDR3/SPICLK	AF16[2]
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/FCC2_UTM_TXADDR3/SPISEL/BRGO1	AH15[2]
PD20/$\overline{\text{RTS4}}$/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14[2]