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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Obsolete
PowerPC G2
1 Core, 32-Bit
200MHz
Communications; RISC CPM
DRAM, SDRAM
No
-
10/100Mbps (3)
-
-
3.3V
-40°C ~ 105°C (TA)
-
480-LBGA Exposed Pad
480-TBGA (37.5x37.5)
https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8265aczumibc

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#### Features

Figure 1 shows the block diagram for the MPC8266, the HiP4 superset device. Shaded portions indicate functionality that is not available on all devices; refer to the notes.



#### Figure 1. MPC8266 Block Diagram

## **1** Features

The major features of the MPC826xA family are as follows:

- Dual-issue integer core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 150-300 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm



Features

- 32-bit address decodes with programmable bank size
- Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
- Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
- Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
    - 10/100-Mbit Ethernet/IEEE Std. 802.3® CDMA/CS interface through media independent interface (MII)
    - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
    - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels.Each MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in timedivision-multiplexed (TDM) channels



Features

- Coset removing (programmable by the user)
- Filtering idle/unassigned cells (programmable by the user)
- Performing HEC error detection and single bit error correction (programmable by user)
- Generating loss of cell delineation status/interrupt (LOC/LCD)
- Operates with FCC2 (UTOPIA 8)
- Provides serial loop back mode
- Cell echo mode is provided
- Supports both FCC transmit modes
  - External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
  - Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.
- Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
- Cell counters for performance monitoring
  - 16-bit counters count
    - HEC error cells
    - HEC single bit error and corrected cells
    - Idle/unassigned cells filtered
    - Idle/unassigned cells transmitted
    - Transmitted ATM cells
    - Received ATM cells
  - Maskable interrupt is sent to the host when a counter expires
- Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
- May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported
- PCI bridge (MPC8265 and MPC8266 only)
  - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  - On-chip arbitration
  - Support for PCI to 60x memory and 60x memory to PCI streaming
  - PCI Host Bridge or Peripheral capabilities
  - Includes 4 DMA channels for the following transfers:
    - PCI-to-60x to 60x-to-PCI
    - 60x-to-PCI to PCI-to-60x
    - PCI-to-60x to PCI-to-60x
    - 60x-to-PCI to 60x-to-PCI
  - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265) required by the PCI standard as well as message and doorbell registers
  - Supports the I<sub>2</sub>O standard



#### **Electrical and Thermal Characteristics**

Table 2 lists recommended operational voltage conditions.

Rating	Symbol		Value				
Core supply voltage	VDD	1.7 – 1.9 <sup>2</sup>	1.7–2.1 <sup>3</sup>	1.9 –2.2 <sup>4</sup>	V		
PLL supply voltage	VCCSYN	1.7 – 1.9 <sup>2</sup>	1.7–2.1 <sup>3</sup>	1.9–2.2 <sup>4</sup>	V		
I/O supply voltage	VDDH		V				
Input voltage	VIN	G	GND (-0.3) - 3.465				
Junction temperature (maximum)	Тj		°C				
Ambient temperature	T <sub>A</sub>		°C				

Table 2. Recommended Operating Conditions<sup>1</sup>

<sup>1</sup> **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

<sup>2</sup> CPU frequency less than or equal to 200 MHz.

<sup>3</sup> CPU frequency greater than 200 MHz but less than 233 MHz.

<sup>4</sup> CPU frequency greater than or equal to 233 MHz.

<sup>5</sup> Note that for extended temperature parts the range is  $(-40)_{T_{\Delta}} - 105_{T_{i}}$ .

#### NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (-5% and -0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or  $V_{CC}$ ).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.



Figure 2. Overshoot/Undershoot Voltage



Characteristic	Symbol	Min	Max	Unit
I <sub>OL</sub> = 7.0 mA	V <sub>OI</sub>		0.4	V
BR	02			
BG				
ABB/IRQ2				
TS				
A[0-31]				
TT[0-4]				
TBST				
TSIZE[0-3]				
AACK				
ARTRY				
DBG				
DBB/IRQ3				
DP(4)/IRQ3/EXT_DR3/CRSTF_001				
DP(5)/TBEN/IBO5/EXT_DBG3				
$DP(6)/CSE(0)/\overline{IBO6}$				
DP(7)/CSE(1)/IBQ7				
PSDVAL				
TA				
TEA				
GBL/IRQ1				
CI/BADDR29/IRQ2				
WT/BADDR30/IRQ3				
L2_HIT/IRQ4				
CPU_BG/BADDR31/IRQ5				
CPU_DBG				
CPU_BR				
IRQ0/NMI_OUT				
IRQ7/INT_OUT/APE				
PORESET				
HRESET				
SRESET				
RSTCONF				
QREQ				

## Table 3. DC Electrical Characteristics<sup>1</sup> (continued)



Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3 \text{mA}$	Vol	_	0.4	V
<u>ČŠ</u> [0-9]	0L			
CS(10)/BCTL1				
CS(11)/AP(0)				
BADDR[27-28]				
ALE				
BCTLO				
PWE(0:7)/PSDDQM(0:7)/PBS(0:7)				
PSDA10/PGPL0				
PSDWE/PGPL1				
POE/PSDRAS/PGPL2				
PSDCAS/PGPL3				
PGTA/PUPMWAIT/PGPL4/PPBS				
PSDAMUX/PGPL5				
LWE[0-3]LSDDQM[0-3]/LBS[0-3]/PCI_CFG[0-3] <sup>3</sup>				
LSDA10/LGPL0/PCI MODCKH03				
LSDWE/LGPL1/PCI_MODCKH1 <sup>3</sup>				
LOE/LSDRAS/LGPL2/PCI MODCKH23				
LSDCAS/LGPL3/PCI_MODCKH3 <sup>3</sup>				
LGTA/LUPMWAIT/LGPL4/LPBS				
LSDAMUX/LGPL5/PCI MODCK <sup>3</sup>				
MODCK1/AP(1)/TC(0)/BNKSEL(0)				
MODCK2/AP(2)/TC(1)/BNKSEL(1)				
MODCK3/AP(3)/TC(2)/BNKSEL(2)				
$I_{OL} = 3.2 \text{mA}$				
L_A14/ <u>PAR<sup>3</sup></u>				
L_A15/ <u>FRAM</u> E <sup>3</sup> /SMI				
L_A16/ <u>TRDY</u> <sup>3</sup>				
L_A17/IRDY <sup>3</sup> /CKSTP_OUT				
L_A18/STOP <sup>3</sup>				
L_A19/DEVSEL <sup>3</sup>				
L_A20/IDSEL <sup>3</sup>				
L_A21/ <u>PERR<sup>3</sup></u>				
L_A22/ <u>SERR</u> <sup>3</sup>				
L_A23/ <u>REQ0</u> <sup>3</sup>				
L_A24/ <u>REQ1</u> 3/HSEJSW3				
L_A25/ <u>GNT03</u>				
L_A26/ <u>GNT1<sup>°</sup>/HSLED<sup>°</sup></u>				
L_A27/GNT2 <sup>3</sup> /HSENUM <sup>3</sup>				
L_A28/ <u>RST</u> <sup>v</sup> /CORE_SRESET				
L_A29/ <u>INTA3</u>				
L_A30/REQ2 <sup>3</sup>				
L_A31				
LCL_D(0-31)/AD <u>(0-</u> 31) <sup>3</sup>				
LCL_DP(0-3)/C/BE(0-3) <sup>3</sup>				
PA[0-31]				
PB[4–31]				
PC[0-31]				
PD[4–31]				
TDO				

## Table 3. DC Electrical Characteristics<sup>1</sup> (continued)

<sup>1</sup> The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.



Table 10 lists SIU output characteristics.

Spec N	Number	Charactariatia	Max De	Max Delay (ns)		Min Delay (ns)	
Мах	Min		66 MHz	83 MHz	66 MHz	83 MHz	
sp31	sp30	PSDVAL/TEA/TA	7	6	0.5	0.5	
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5	
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5	
sp33b	sp30	DP	8	7	0.5	0.5	
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5	
sp35	sp30	All other signals	6	5.5	0.5	0.5	

#### Table 10. AC Characteristics for SIU Outputs<sup>1</sup>

<sup>1</sup> Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

#### NOTE

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.



#### **Electrical and Thermal Characteristics**

#### Table 12 lists the JTAG timings.

Table 12. JTAG Timings<sup>1</sup>

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f <sub>JTG</sub>	0	25	MHz	—
JTAG external clock cycle time	t <sub>JTG</sub>	40	_	ns	—
JTAG external clock pulse width measured at 1.4V	t <sub>JTKHKL</sub>	20	-	ns	—
JTAG external clock rise and fall times	t <sub>JTGR</sub> and t <sub>JTGF</sub>	0	5	ns	6
TRST assert time	t <sub>TRST</sub>	25	_	ns	3, 6
Input setup times Boundary-scan data TMS, TDI	t <sub>JTDVKH</sub> t <sub>JTIVKH</sub>	4 4		ns ns	4, 7 4, 7
Input hold times Boundary-scan data TMS, TDI	t <sub>JTDXKH</sub> t <sub>JTIXKH</sub>	10 10		ns ns	4, 7 4, 7
Output valid times Boundary-scan data TDO	t <sub>JTKLDV</sub> t <sub>JTKLOV</sub>		25 25	ns ns	5, 7 5. 7
Output hold times Boundary-scan data TDO	t <sub>JTKLDX</sub> t <sub>JTKLOX</sub>	1	_	ns ns	5, 7 5, 7
JTAG external clock to output high impedance Boundary-scan data TDO	t <sub>JTKLDZ</sub> t <sub>JTKLOZ</sub>	1	25 25	ns ns	5, 6 5, 6

<sup>1</sup> All outputs are measured from the midpoint voltage of the falling/rising edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50- $\Omega$  load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

<sup>2</sup> The symbols used for timing specifications herein follow the pattern of t<sub>(first two letters of functional block)(signal)(state)</sub> (reference)(state) for inputs and t((first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t<sub>JTDVKH</sub> symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>JTDXKH</sub> symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>JTDXKH</sub> symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

- <sup>3</sup> TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- <sup>4</sup> Non-JTAG signal input timing with respect to t<sub>TCLK</sub>.
- <sup>5</sup> Non-JTAG signal output timing with respect to t<sub>TCLK</sub>.
- <sup>6</sup> Guaranteed by design.
- <sup>7</sup> Guaranteed by design and device characterization.

#### NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.



MODCK_H-MODCK[1-3]	Input Clock Frequency <sup>2,3</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency <sup>2</sup>	Core Multiplication Factor <sup>2</sup>	Core Frequency <sup>2</sup>
0100_111			Reserved		
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	66 MHz	2	133 MHz	2.5	166 MHz
0101_111	66 MHz	2	133 MHz	3	200 MHz
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
	1				
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	66 MHz	2.5	166 MHz	2.5	166 MHz
0110_101	66 MHz	2.5	166 MHz	3	200 MHz
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
			•		
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz

## Table 14. Clock Configuration Modes<sup>1</sup> (continued)

**Clock Configuration Modes** 

MODCK_H-MODCK[1-3]	Input Clock Frequency <sup>2,3</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency <sup>2</sup>	Core Multiplication Factor <sup>2</sup>	Core Frequency <sup>2</sup>
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

<sup>1</sup> Because of speed dependencies, not all of the possible configurations in Table 14 are applicable.

<sup>2</sup> The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than 150 MHz and the CPM ranges between 66–233 MHz.

<sup>3</sup> Input clock frequency is given only for the purpose of reference. The user should set MODCK\_H–MODCK\_L so that the resulting configuration does not exceed the frequency rating of the user's part.

## 3.2 PCI Mode

The MPC8265 and the MPC8266 have three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI\_MODE, PCI\_CFG[0], PCI\_MODCK—as shown in Table 15.

	Pins		Clocking Mode	PCI Clock
PCI_MODE	PCI_CFG[0]	PCI_MODCK		(MHZ)
1	_	_	Local bus	—
0	0	0	PCI host	50–66
0	0	1		25–50
0	1	0	PCI agent	50–66
0	1	1		25–50

 Table 15. MPC8265 and MPC8266 Clocking Modes

In addition, note the following:

#### NOTE: PCI\_MODCK

In PCI mode only, PCI\_MODCK comes from the LGPL5 pin and MODCK\_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

### NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI\_MODCK = 1, and the minimum Tval = 1 when PCI\_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

#### NOTE

Clock configurations change only after  $\overline{POR}$  is asserted.



## 3.2.1 PCI Host Mode

The frequencies listed in Table 16 and Table 17 are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

MODCK[1-3] <sup>1</sup>	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor <sup>2</sup>	PCI Frequency <sup>2</sup>
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

Table 16. Clock Default Configurations in PCI Host Mode (MODCK\_HI = 0000)

<sup>1</sup> Assumes MODCK\_HI = 0000.

<sup>2</sup> The frequency depends on the value of PCI\_MODCK. If PCI\_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to Table 15.

Table 17 describes all possible clock configurations when using the MPC8265's or the MPC8266's internal PCI bridge in host mode.

MODCK_H – MODCK[1–3]	Input Clock Frequency <sup>1</sup> (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor <sup>2</sup>	PCI Frequency <sup>2</sup>
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	33 MHz	4	133 MHz	5	166 MHz	4/8	<b>33</b> /16 MHz
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000 <sup>3</sup>	33 MHz	5	166 MHz	5	166 MHz	5	33 MHz
0011_001 <sup>3</sup>	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz
0011_010 <sup>3</sup>	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz

Table 17. Clock Configuration Modes in PCI Host Mode



**Clock Configuration Modes** 

MODCK_H – MODCK[1–3]	Input Clock Frequency <sup>1</sup> (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor <sup>2</sup>	PCI Frequency <sup>2</sup>
0011_011 <sup>3</sup>	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
		L	1		I	L	
0100_000 <sup>3</sup>	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001 <sup>3</sup>	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010 <sup>3</sup>	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011 <sup>3</sup>	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
		·					
0101_000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
0101_001	66 MHz	2	133 MHz	3	200 MHz	<b>2</b> /4	66/33 MHz
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	66 MHz	2.5	166 MHz	2.5	166 MHz	3/6	55/28 MHz
0110_001	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
				1			
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
				1			
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
			1	1	1	I	1
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency <sup>1</sup> (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor <sup>2</sup>	PCI Frequency <sup>2</sup>
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

<sup>1</sup> Input clock frequency is given only for the purpose of reference. User should set MODCK\_H–MODCK\_L so that the resulting configuration does not exceed the frequency rating of the user's part.

<sup>2</sup> The frequency depends on the value of PCI\_MODCK. If PCI\_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to Table 15.

<sup>3</sup> In this mode, PCI\_MODCK must be "0".

## 3.2.2 PCI Agent Mode

The frequencies listed in Table 18 and Table 19 are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

MODCK[1–3] <sup>1</sup>	Input Clock Frequency (PCI) <sup>2</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency	Core Multiplication Factor	Core Frequency <sup>3</sup>	Bus Division Factor	60x Bus Frequency <sup>4</sup>
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK\_HI = 0000)

**Clock Configuration Modes** 

MODCK[1-3] <sup>1</sup>	Input Clock Frequency (PCI) <sup>2</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency	Core Multiplication Factor	Core Frequency <sup>3</sup>	Bus Division Factor	60x Bus Frequency <sup>4</sup>
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK\_HI = 0000) (continued)

<sup>1</sup> Assumes MODCK\_HI = 0000.

<sup>2</sup> The frequency depends on the value of PCI\_MODCK. If PCI\_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.

<sup>3</sup> Core frequency = (60x bus frequency)(core multiplication factor)

<sup>4</sup> Bus frequency = CPM frequency/bus division factor

Table 19 describes all possible clock configurations when using the MPC8265 or the MPC8266's internal PCI bridge in agent mode.

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) <sup>1,2</sup>	CPM Multiplication Factor <sup>1</sup>	CPM Frequency	Core Multiplication Factor	Core Frequency <sup>3</sup>	Bus Division Factor	60x Bus Frequency <sup>4</sup>
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	150 MHz	3	180 MHz	2.5	60 MHz
0010_010	50/25 MHz	3/6	150 MHz	3.5	210 MHz	2.5	60 MHz
0010_011	50/25 MHz	3/6	150 MHz	4	240 MHz	2.5	60 MHz
0010_100	50/25 MHz	3/6	150 MHz	4.5	270 MHz	2.5	60 MHz
0011_000	66/33 MHz	2/4	133 MHz	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	133 MHz	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	133 MHz	3.5	154 MHz	3	44 MHz
0011_011	66/33 MHz	2/4	133 MHz	4	176MHz	3	44 MHz
0011_100	66/33 MHz	2/4	133 MHz	4.5	198 MHz	3	44 MHz
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	3	66 MHz
0100_001	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
0100_010	66/33 MHz	3/6	200 MHz	3.5	233 MHz	3	66 MHz
0100_011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode



MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) <sup>1,2</sup>	CPM Multiplication Factor <sup>1</sup>	CPM Frequency	Core Multiplication Factor	Core Frequency <sup>3</sup>	Bus Division Factor	60x Bus Frequency <sup>4</sup>
0100_100	66/33 MHz	3/6	200 MHz	4.5	300 MHz	3	66 MHz
0101_000 <sup>5</sup>	33 MHz	5	166 MHz	2.5	166 MHz	2.5	66 MHz
0101_001 <sup>5</sup>	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010 <sup>5</sup>	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011 <sup>5</sup>	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100 <sup>5</sup>	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Pinout

Pin Name	Ball
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	В7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6

### Table 21. Pinout List (continued)



Pin Name	Ball
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/RSRV/EXT_BR2	B22
IRQ1/DP1/EXT_BG2	A22
IRQ2/DP2/TLBISYNC/EXT_DBG2	E21



### Table 21. Pinout List (continued)

Pin Name	Ball
L_A28/RST <sup>1</sup> /CORE_SRESET	AB29
L_A29/INTA <sup>1</sup>	AB28
L_A30/REQ2 <sup>1</sup>	P25
L_A31/DLLOUT <sup>1</sup>	AB27
LCL_D0/AD0 <sup>1</sup>	H29
LCL_D1/AD1 <sup>1</sup>	J29
LCL_D2/AD2 <sup>1</sup>	J28
LCL_D3/AD3 <sup>1</sup>	J27
LCL_D4/AD4 <sup>1</sup>	J26
LCL_D5/AD5 <sup>1</sup>	J25
LCL_D6/AD6 <sup>1</sup>	К25
LCL_D7/AD7 <sup>1</sup>	L29
LCL_D8/AD8 <sup>1</sup>	L27
LCL_D9/AD9 <sup>1</sup>	L26
LCL_D10/AD10 <sup>1</sup>	L25
LCL_D11/AD11 <sup>1</sup>	M29
LCL_D12/AD12 <sup>1</sup>	M28
LCL_D13/AD13 <sup>1</sup>	M27
LCL_D14/AD14 <sup>1</sup>	M26
LCL_D15/AD15 <sup>1</sup>	N29
LCL_D16/AD16 <sup>1</sup>	T25
LCL_D17/AD17 <sup>1</sup>	U27
LCL_D18/AD18 <sup>1</sup>	U26
LCL_D19/AD19 <sup>1</sup>	U25
LCL_D20/AD20 <sup>1</sup>	V29
LCL_D21/AD21 <sup>1</sup>	V28
LCL_D22/AD22 <sup>1</sup>	V27
LCL_D23/AD23 <sup>1</sup>	V26
LCL_D24/AD24 <sup>1</sup>	W27
LCL_D25/AD25 <sup>1</sup>	W26
LCL_D26/AD26 <sup>1</sup>	W25
LCL_D27/AD27 <sup>1</sup>	Y29
LCL_D28/AD28 <sup>1</sup>	Y28
LCL_D29/AD29 <sup>1</sup>	Y25
LCL_D30/AD30 <sup>1</sup>	AA29



#### Package Description

- <sup>3</sup> On PCI devices (MPC8265 and MPC8266) this pin should be used as CLKIN2. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled down or left floating.
- <sup>4</sup> Must be pulled down or left floating.
- <sup>5</sup> On PCI devices (MPC8265 and MPC8266) this pin should be asserted if the PCI function is desired or pulled up or left floating if PCI is not desired. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled up or left floating.
- <sup>6</sup> For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com.

# 5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC826xA.

## 5.1 Package Parameters

Package parameters are provided in Table 22. The package type is a  $37.5 \times 37.5$  mm, 480-lead TBGA.

Parameter	Value
Package Outline	$37.5 \times 37.5 \text{ mm}$
Interconnects	480 (29 $ imes$ 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

Table 22. Package Parameters



## 5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature