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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Active
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	<a href="https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc8255acvvmhbb">https://www.e-xfl.com/pro/item?MUrl=&amp;PartUrl=mpc8255acvvmhbb</a>

- 32-bit address decodes with programmable bank size
- Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
- Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
- Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
    - 10/100-Mbit Ethernet/IEEE Std. 802.3@ CDMA/CS interface through media independent interface (MII)
    - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
    - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

- Transparent
- UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I<sup>2</sup>C) controller (identical to the MPC860 I<sup>2</sup>C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8255)
  - Supports two groups of four TDM channels for a total of eight TDMs
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

Additional features of the MPC826xA family are as follows:

- CPM
  - 32-Kbyte dual-port RAM
  - Additional MCC host commands
  - Eight transfer transmission convergence (TC) layers between the TDMs and FCC2 to support inverse multiplexing for ATM capabilities (IMA) (MPC8264 and MPC8266 only)
- CPM multiplexing
  - FCC2 can also be connected to the TC layer.
- TC layer (MPC8264 and MPC8266 only)
  - Each of the 8 TDM channels is routed in hardware to a TC layer block
    - Protocol-specific overhead bits may be discarded or routed to other controllers by the SI
    - Performing ATM TC layer functions (according to ITU-T I.432)
      - Transmit (Tx) updates
        - Cell HEC generation
        - Payload scrambling using self synchronizing scrambler (programmable by the user)
        - Coset generation (programmable by the user)
        - Cell rate by inserting idle/unassigned cells
      - Receive (Rx) updates
        - Cell delineation using bit by bit HEC checking and programmable ALPHA and DELTA parameters for the delineation state machine
        - Payload descrambling using self synchronizing scrambler (programmable by the user)

Table 2 lists recommended operational voltage conditions.

**Table 2. Recommended Operating Conditions<sup>1</sup>**

Rating	Symbol	Value			Unit
Core supply voltage	VDD	1.7 – 1.9 <sup>2</sup>	1.7–2.1 <sup>3</sup>	1.9 – 2.2 <sup>4</sup>	V
PLL supply voltage	VCCSYN	1.7 – 1.9 <sup>2</sup>	1.7–2.1 <sup>3</sup>	1.9–2.2 <sup>4</sup>	V
I/O supply voltage	VDDH	3.135 – 3.465			V
Input voltage	VIN	GND (–0.3) – 3.465			V
Junction temperature (maximum)	T <sub>j</sub>	105 <sup>5</sup>			°C
Ambient temperature	T <sub>A</sub>	0–70 <sup>5</sup>			°C

<sup>1</sup> **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

<sup>2</sup> CPU frequency less than or equal to 200 MHz.

<sup>3</sup> CPU frequency greater than 200 MHz but less than 233 MHz.

<sup>4</sup> CPU frequency greater than or equal to 233 MHz.

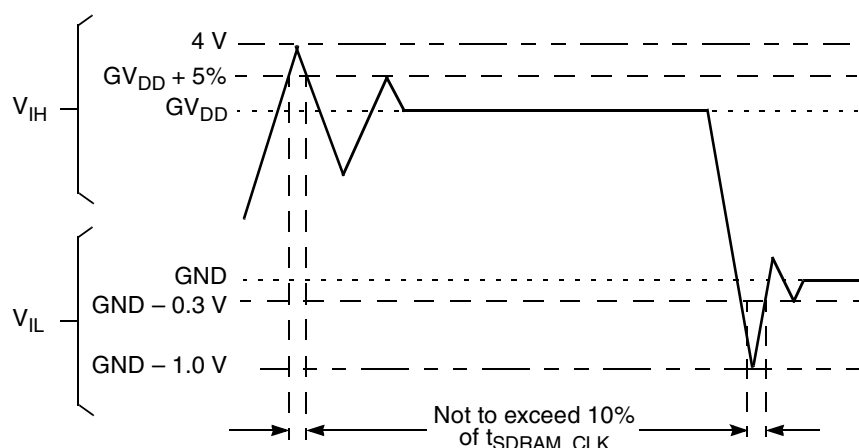
<sup>5</sup> Note that for extended temperature parts the range is (–40)<sub>T<sub>A</sub></sub> – 105<sub>T<sub>j</sub></sub>.

**NOTE: Core, PLL, and I/O Supply Voltages**

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (–5% and –0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V<sub>CC</sub>).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.



**Figure 2. Overshoot/Undershoot Voltage**

Table 3. DC Electrical Characteristics<sup>1</sup> (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 7.0 \text{ mA}$ $\overline{BR}$ $\overline{BG}$ $\overline{ABB/IRQ2}$ $\overline{TS}$ $A[0-31]$ $TT[0-4]$ $\overline{TBST}$ $TSIZE[0-3]$ $\overline{AACK}$ $\overline{ARTRY}$ $\overline{DBG}$ $\overline{DBB/IRQ3}$ $D[0-63]$ $DP(0)/\overline{RSRV/EXT\_BR2}$ $DP(1)/\overline{IRQ1/EXT\_BG2}$ $DP(2)/\overline{TLBISYNC/IRQ2/EXT\_DBG2}$ $DP(3)/\overline{IRQ3/EXT\_BR3/CKSTP\_OUT}$ $DP(4)/\overline{IRQ4/EXT\_BG3/CORE\_SREST}$ $DP(5)/\overline{TBEN/IRQ5/EXT\_DBG3}$ $DP(6)/\overline{CSE(0)/IRQ6}$ $DP(7)/\overline{CSE(1)/IRQ7}$ $\overline{PSDVAL}$ $\overline{TA}$ $\overline{TEA}$ $\overline{GBL/IRQ1}$ $\overline{CI/BADDR29/IRQ2}$ $\overline{WT/BADDR30/IRQ3}$ $\overline{L2\_HIT/IRQ4}$ $\overline{CPU\_BG/BADDR31/IRQ5}$ $\overline{CPU\_DBG}$ $\overline{CPU\_BR}$ $\overline{IRQ0/NMI\_OUT}$ $\overline{IRQ7/INT\_OUT/APE}$ $\overline{PORESET}$ $\overline{HRESET}$ $\overline{SRESET}$ $\overline{RSTCONF}$ $\overline{QREQ}$	$V_{OL}$	—	0.4	V

## 2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC826xA device. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in Table 6.

**Table 6. Output Buffer Impedances<sup>1</sup>**

Output Buffers	Typical Impedance ( $\Omega$ )
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

<sup>1</sup> These are typical values at 65° C. The impedance may vary by  $\pm 25\%$  with process and temperature.

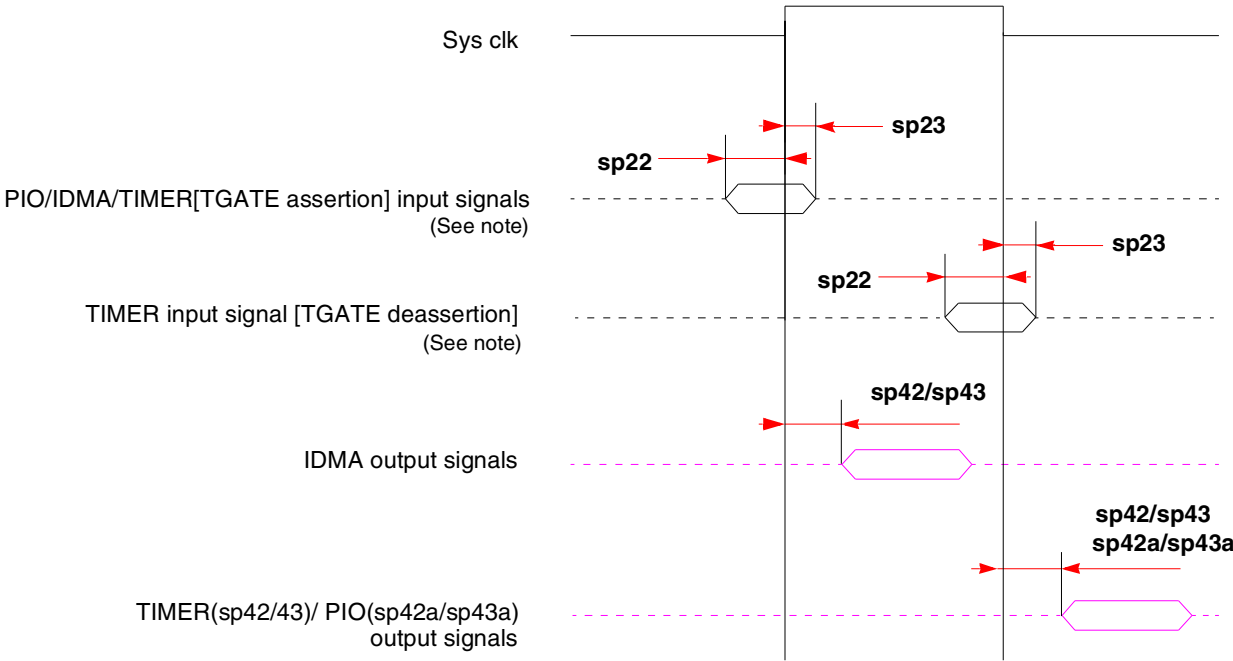
Table 7 lists CPM output characteristics.

**Table 7. AC Characteristics for CPM Outputs<sup>1</sup>**

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

<sup>1</sup> Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Figure 8 shows PIO, timer, and DMA signals.



**Note:** TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

**Figure 8. PIO, Timer, and DMA Signal Diagram**

Table 10 lists SIU input characteristics.

**Table 9. AC Characteristics for SIU Inputs<sup>1</sup>**

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	AACK/ARTRY/T $\overline{\text{A}}$ /TS/TEA/DBG/BG/BR	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

<sup>1</sup> Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 12 lists the JTAG timings.

**Table 12. JTAG Timings<sup>1</sup>**

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock frequency of operation	$f_{JTG}$	0	25	MHz	—
JTAG external clock cycle time	$t_{JTG}$	40	—	ns	—
JTAG external clock pulse width measured at 1.4V	$t_{JTKHKL}$	20	—	ns	—
JTAG external clock rise and fall times	$t_{JTGR}$ and $t_{JTGF}$	0	5	ns	6
TRST assert time	$t_{TRST}$	25	—	ns	3, 6
Input setup times	Boundary-scan data	$t_{JTDVKH}$	4	ns	4, 7
	TMS, TDI	$t_{JTIVKH}$	4	ns	4, 7
Input hold times	Boundary-scan data	$t_{JTDXKH}$	10	ns	4, 7
	TMS, TDI	$t_{JTIXKH}$	10	ns	4, 7
Output valid times	Boundary-scan data	$t_{JTKLDV}$	—	ns	5, 7
	TDO	$t_{JTKLOV}$	25	ns	5, 7
Output hold times	Boundary-scan data	$t_{JTKLDX}$	1	ns	5, 7
	TDO	$t_{JTKLOX}$	1	ns	5, 7
JTAG external clock to output high impedance	Boundary-scan data	$t_{JTKLDZ}$	1	ns	5, 6
	TDO	$t_{JTKLOZ}$	1	ns	5, 6

<sup>1</sup> All outputs are measured from the midpoint voltage of the falling/rising edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

<sup>2</sup> The symbols used for timing specifications herein follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$  (reference)(state) for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{JTDVKH}$  symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{JTDXKH}$  symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

<sup>3</sup> TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

<sup>4</sup> Non-JTAG signal input timing with respect to  $t_{TCLK}$ .

<sup>5</sup> Non-JTAG signal output timing with respect to  $t_{TCLK}$ .

<sup>6</sup> Guaranteed by design.

<sup>7</sup> Guaranteed by design and device characterization.

#### NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.



Table 14. Clock Configuration Modes<sup>1</sup> (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency <sup>2,3</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency <sup>2</sup>	Core Multiplication Factor <sup>2</sup>	Core Frequency <sup>2</sup>
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	<b>33 MHz</b>	<b>4</b>	<b>133 MHz</b>	<b>4</b>	<b>133 MHz</b>
0010_011	<b>33 MHz</b>	<b>4</b>	<b>133 MHz</b>	<b>5</b>	<b>166 MHz</b>
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					

Table 14. Clock Configuration Modes<sup>1</sup> (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency <sup>2,3</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency <sup>2</sup>	Core Multiplication Factor <sup>2</sup>	Core Frequency <sup>2</sup>
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	<b>66 MHz</b>	<b>2</b>	<b>133 MHz</b>	<b>2.5</b>	<b>166 MHz</b>
0101_111	<b>66 MHz</b>	<b>2</b>	<b>133 MHz</b>	<b>3</b>	<b>200 MHz</b>
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	<b>66 MHz</b>	<b>2.5</b>	<b>166 MHz</b>	<b>2.5</b>	<b>166 MHz</b>
0110_101	<b>66 MHz</b>	<b>2.5</b>	<b>166 MHz</b>	<b>3</b>	<b>200 MHz</b>
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency <sup>1</sup> (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor <sup>2</sup>	PCI Frequency <sup>2</sup>
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

<sup>1</sup> Input clock frequency is given only for the purpose of reference. User should set MODCK\_H–MODCK\_L so that the resulting configuration does not exceed the frequency rating of the user's part.

<sup>2</sup> The frequency depends on the value of PCI\_MODCK. If PCI\_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to [Table 15](#).

<sup>3</sup> In this mode, PCI\_MODCK must be "0".

### 3.2.2 PCI Agent Mode

The frequencies listed in [Table 18](#) and [Table 19](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK\_HI = 0000)

MODCK[1–3] <sup>1</sup>	Input Clock Frequency (PCI) <sup>2</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency	Core Multiplication Factor	Core Frequency <sup>3</sup>	Bus Division Factor	60x Bus Frequency <sup>4</sup>
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

**Table 18. Clock Default Configurations in PCI Agent Mode (MODCK\_HI = 0000) (continued)**

MODCK[1–3] <sup>1</sup>	Input Clock Frequency (PCI) <sup>2</sup>	CPM Multiplication Factor <sup>2</sup>	CPM Frequency	Core Multiplication Factor	Core Frequency <sup>3</sup>	Bus Division Factor	60x Bus Frequency <sup>4</sup>
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

<sup>1</sup> Assumes MODCK\_HI = 0000.

<sup>2</sup> The frequency depends on the value of PCI\_MODCK. If PCI\_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to [Table 15](#).

<sup>3</sup> Core frequency = (60x bus frequency)(core multiplication factor)

<sup>4</sup> Bus frequency = CPM frequency/bus division factor

[Table 19](#) describes all possible clock configurations when using the MPC8265 or the MPC8266's internal PCI bridge in agent mode.

**Table 19. Clock Configuration Modes in PCI Agent Mode**

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) <sup>1,2</sup>	CPM Multiplication Factor <sup>1</sup>	CPM Frequency	Core Multiplication Factor	Core Frequency <sup>3</sup>	Bus Division Factor	60x Bus Frequency <sup>4</sup>
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	<b>150 MHz</b>	3	180 MHz	2.5	<b>60 MHz</b>
0010_010	50/25 MHz	3/6	<b>150 MHz</b>	3.5	210 MHz	2.5	<b>60 MHz</b>
0010_011	50/25 MHz	3/6	<b>150 MHz</b>	4	240 MHz	2.5	<b>60 MHz</b>
0010_100	50/25 MHz	3/6	<b>150 MHz</b>	4.5	270 MHz	2.5	<b>60 MHz</b>
0011_000	66/33 MHz	2/4	<b>133 MHz</b>	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	<b>133 MHz</b>	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	<b>133 MHz</b>	3.5	154 MHz	3	<b>44 MHz</b>
0011_011	66/33 MHz	2/4	<b>133 MHz</b>	4	176MHz	3	<b>44 MHz</b>
0011_100	66/33 MHz	2/4	<b>133 MHz</b>	4.5	198 MHz	3	<b>44 MHz</b>
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	<b>3</b>	66 MHz
0100_001	66/33 MHz	3/6	<b>200 MHz</b>	3	200 MHz	<b>3</b>	<b>66 MHz</b>
0100_010	66/33 MHz	3/6	<b>200 MHz</b>	3.5	233 MHz	<b>3</b>	<b>66 MHz</b>
0100_011	66/33 MHz	3/6	<b>200 MHz</b>	4	266 MHz	<b>3</b>	<b>66 MHz</b>

**Table 19. Clock Configuration Modes in PCI Agent Mode (continued)**

<b>MODCK_H – MODCK[1–3]</b>	<b>Input Clock Frequency (PCI)<sup>1,2</sup></b>	<b>CPM Multiplication Factor<sup>1</sup></b>	<b>CPM Frequency</b>	<b>Core Multiplication Factor</b>	<b>Core Frequency<sup>3</sup></b>	<b>Bus Division Factor</b>	<b>60x Bus Frequency<sup>4</sup></b>
0100_100	66/33 MHz	3/6	<b>200 MHz</b>	4.5	300 MHz	<b>3</b>	<b>66 MHz</b>
0101_000 <sup>5</sup>	33 MHz	5	166 MHz	2.5	166 MHz	2.5	<b>66 MHz</b>
0101_001 <sup>5</sup>	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010 <sup>5</sup>	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011 <sup>5</sup>	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100 <sup>5</sup>	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

**Table 19. Clock Configuration Modes in PCI Agent Mode (continued)**

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) <sup>1,2</sup>	CPM Multiplication Factor <sup>1</sup>	CPM Frequency	Core Multiplication Factor	Core Frequency <sup>3</sup>	Bus Division Factor	60x Bus Frequency <sup>4</sup>
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

- <sup>1</sup> The frequency depends on the value of PCI\_MODCK. If PCI\_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to [Table 15](#).
- <sup>2</sup> Input clock frequency is given only for the purpose of reference. User should set MODCK\_H–MODCK\_L so that the resulting configuration does not exceed the frequency rating of the user's part.
- <sup>3</sup> Core frequency = (60x bus frequency)(core multiplication factor)
- <sup>4</sup> Bus frequency = CPM frequency/bus division factor
- <sup>5</sup> In this mode, PCI\_MODCK must be "1".

# 4 Pinout

This section provides the pin assignments and pinout list for the MPC826xA.

## 4.1 Pin Assignments

Figure 13 shows the pinout of the MPC826xA's 480 TBGA package as viewed from the top surface.

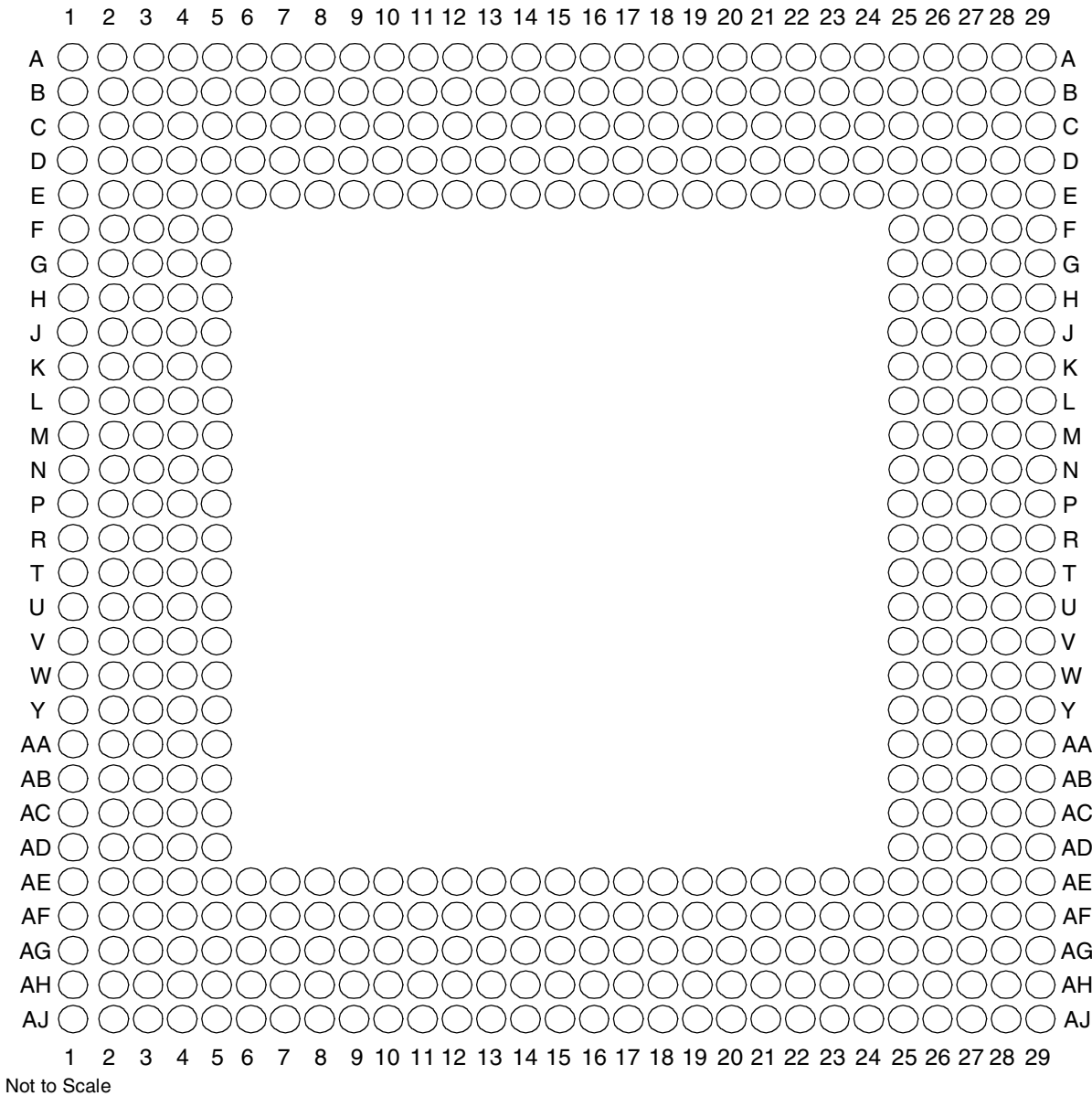


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

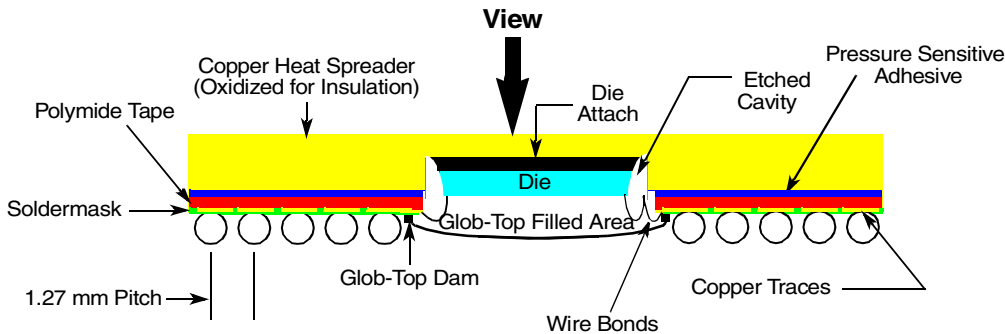


Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$ , are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

Table 21. Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2



Table 21. Pinout List (continued)

Pin Name	Ball
IRQ3/DP3/CKSTP_OUT/EXT_BR3	D21
IRQ4/DP4/CORE_SRESET/EXT_BG3	C21
IRQ5/DP5/TBEN/EXT_DBG3	B21
IRQ6/DP6/CSE0	A21
IRQ7/DP7/CSE1	E20
PSDVAL	V3
TA	C22
TEA	V5
GBL/IRQ1	W1
C1/BADDR29/IRQ2	U2
WT/BADDR30/IRQ3	U3
L2_HIT/IRQ4	Y4
CPU_BG/BADDR31/IRQ5	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
CS10/BCTL1	F29
CS11/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24

Table 21. Pinout List (continued)

Pin Name	Ball
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/LBS0/PCI_CFG0 <sup>1</sup>	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1 <sup>1</sup>	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2 <sup>1</sup>	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3 <sup>1</sup>	G29
LSDA10/LGPL0/PCI_MODCKH0 <sup>1</sup>	D27
LSDWE/LGPL1/PCI_MODCKH1 <sup>1</sup>	C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2 <sup>1</sup>	E26
LSDCAS/LGPL3/PCI_MODCKH3 <sup>1</sup>	D25
LGTA/LUPMWAIT/LGPL4/LPBS	C26
LGPL5/LSDAMUX/PCI_MODCK <sup>1</sup>	B27
LWR	D28
L_A14/PAR <sup>1</sup>	N27
L_A15/FRAME <sup>1</sup> /SMI	T29
L_A16/TRDY <sup>1</sup>	R27
L_A17/IRDY <sup>1</sup> /CKSTP_OUT	R26
L_A18/STOP <sup>1</sup>	R29
L_A19/DEVSEL <sup>1</sup>	R28
L_A20/IDSEL <sup>1</sup>	W29
L_A21/PERR <sup>1</sup>	P28
L_A22/SERR <sup>1</sup>	N26
L_A23/REQ0 <sup>1</sup>	AA27
L_A24/REQ1 <sup>1</sup> /HSEJSW <sup>1</sup>	P29
L_A25/GNT0 <sup>1</sup>	AA26
L_A26/GNT1 <sup>1</sup> /HSLED <sup>1</sup>	N25
L_A27/GNT2 <sup>1</sup> /HSENUM <sup>1</sup>	AA25

Table 21. Pinout List (continued)

Pin Name	Ball
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21 <sup>2</sup>
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20 <sup>2</sup>
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19 <sup>2</sup>
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18 <sup>2</sup>
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17 <sup>2</sup>
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16 <sup>2</sup>
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16 <sup>2</sup>
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15 <sup>2</sup>
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13 <sup>2</sup>
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13 <sup>2</sup>
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12 <sup>2</sup>
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11 <sup>2</sup>
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9 <sup>2</sup>
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8 <sup>2</sup>
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7 <sup>2</sup>
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7 <sup>2</sup>
PA28/FCC1_UTM_RXENB/FCC1_UTS_RXENB/FCC1_MII_TX_EN	AD5 <sup>2</sup>
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1 <sup>2</sup>
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/ FCC1_RTS	AD3 <sup>2</sup>
PA31/FCC1_UTM_TXENB/FCC1_UTS_TXENB/FCC1_MII_COL	AB5 <sup>2</sup>
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/FCC3_RTS	AD28 <sup>2</sup>
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26 <sup>2</sup>
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25 <sup>2</sup>
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26 <sup>2</sup>
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27 <sup>2</sup>
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24 <sup>2</sup>
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24 <sup>2</sup>
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24 <sup>2</sup>
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22 <sup>2</sup>
PB13/FCC3_MII_COL/L1RQB1/L1TSYNCC1/L1GNTE1/L1TXD1A2	AH21 <sup>2</sup>
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20 <sup>2</sup>
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19 <sup>2</sup>
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18 <sup>2</sup>
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17 <sup>2</sup>

Table 21. Pinout List (continued)

Pin Name	Ball
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13 <sup>2</sup>
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12 <sup>2</sup>
PD23/ $\overline{\text{RTS3}}$ /TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12 <sup>2</sup>
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10 <sup>2</sup>
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9 <sup>2</sup>
PD26/ $\overline{\text{RTS2}}$ /TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8 <sup>2</sup>
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7 <sup>2</sup>
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4 <sup>2</sup>
PD29/ $\overline{\text{RTS1}}$ /TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4	AG1 <sup>2</sup>
PD30/ $\overline{\text{FCC2\_UTM\_TXENB}}$ /FCC2_UTS_TXENB/TXD1	AD4 <sup>2</sup>
PD31/RXD1	AD2 <sup>2</sup>
VCCSYN	AB3
VCCSYN1	B9
GNDSYN	AB1
CLKIN2 <sup>1,3</sup>	AE11
SPARE4 <sup>4</sup>	U5
$\overline{\text{PCI\_MODE}}$ <sup>1,5</sup>	AF25
SPARE6 <sup>4</sup>	V4
THERMAL0 <sup>6</sup>	AA1
THERMAL1 <sup>6</sup>	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

<sup>1</sup> MPC8265 and MPC8266 only.

<sup>2</sup> The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

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