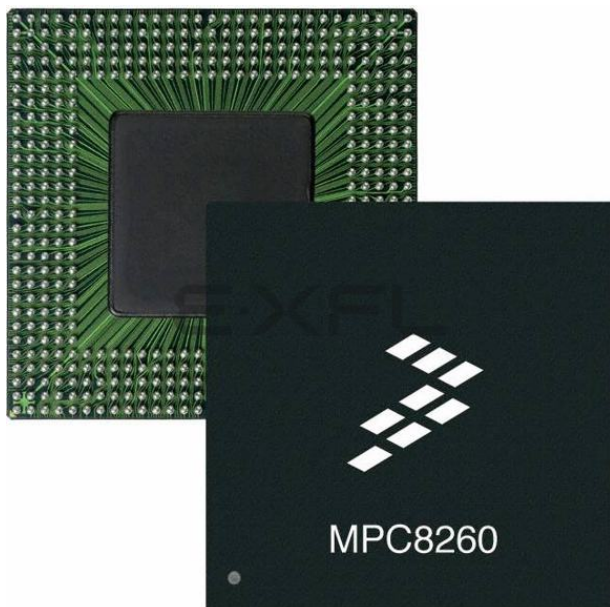




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8255aczumibb

- PowerPC architecture-compliant memory management unit (MMU)
- Common on-chip processor (COP) test interface
- High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPS/MHz without inlining and 1.90 Dhrystones MIPS/MHz with
- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
 - G2 core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
 - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge (MPC8265 and MPC8266 only)
 - Programmable host bridge and agent
 - 32-bit data bus, 66 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE Std. 1149.1™ standard JTAG test access port
- Twelve-bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
 - Byte write enables and selectable parity generation

- 32-bit address decodes with programmable bank size
- Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
- Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
- Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
 - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
 - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
 - Serial DMA channels for receive and transmit on all serial channels
 - Parallel I/O registers with open-drain and interrupt capability
 - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
 - Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
 - 10/100-Mbit Ethernet/IEEE Std. 802.3® CDMA/CS interface through media independent interface (MII)
 - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
 - Transparent
 - HDLC—Up to T3 rates (clear channel)
 - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
 - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels. Each MCC can be split into four subgroups of 32 channels each.
 - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
 - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
 - Ethernet/IEEE 802.3 CDMA/CS
 - HDLC/SDLC and HDLC bus
 - Universal asynchronous receiver transmitter (UART)
 - Synchronous UART
 - Binary synchronous (BISYNC) communications
 - Transparent
 - Two serial management controllers (SMCs), identical to those of the MPC860
 - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

- Coset removing (programmable by the user)
- Filtering idle/unassigned cells (programmable by the user)
- Performing HEC error detection and single bit error correction (programmable by user)
- Generating loss of cell delineation status/interrupt (LOC/LCD)
- Operates with FCC2 (UTOPIA 8)
- Provides serial loop back mode
- Cell echo mode is provided
- Supports both FCC transmit modes
 - External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
 - Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.
- Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
- Cell counters for performance monitoring
 - 16-bit counters count
 - HEC error cells
 - HEC single bit error and corrected cells
 - Idle/unassigned cells filtered
 - Idle/unassigned cells transmitted
 - Transmitted ATM cells
 - Received ATM cells
 - Maskable interrupt is sent to the host when a counter expires
- Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
- May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported
- PCI bridge (MPC8265 and MPC8266 only)
 - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI to 60x memory and 60x memory to PCI streaming
 - PCI Host Bridge or Peripheral capabilities
 - Includes 4 DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - PCI-to-60x to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI
 - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265) required by the PCI standard as well as message and doorbell registers
 - Supports the I₂O standard

Table 3 shows DC electrical characteristics.

Table 3. DC Electrical Characteristics¹

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs except CLKIN	V_{IH}	2.0	3.465	V
Input low voltage	V_{IL}	GND	0.8	V
CLKIN input high voltage	V_{IHC}	2.4	3.465	V
CLKIN input low voltage	V_{ILC}	GND	0.4	V
Input leakage current, $V_{IN} = V_{DDH}^2$	I_{IN}	—	10	μA
Hi-Z (off state) leakage current, $V_{IN} = V_{DDH}^2$	I_{OZ}	—	10	μA
Signal low input current, $V_{IL} = 0.8$ V	I_L	—	1	μA
Signal high input current, $V_{IH} = 2.0$ V	I_H	—	1	μA
Output high voltage, $I_{OH} = -2$ mA except XFC, UTOPIA mode, and open drain pins In UTOPIA mode: $I_{OH} = -8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OH}	2.4	—	V
In UTOPIA mode: $I_{OL} = 8.0$ mA PA[0-31] PB[4-31] PC[0-31] PD[4-31]	V_{OL}	—	0.5	V

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ $\overline{ALE}$ $\overline{BCTL0}$ $\overline{PWE}(0:7)/\overline{PSDDQM}(0:7)/\overline{PBS}(0:7)$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0-3]/\overline{LBS}[0-3]/\overline{PCI_CFG}[0-3]^3$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI_MODCKH0}^3$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI_MODCKH1}^3$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI_MODCKH2}^3$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI_MODCKH3}^3$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI_MODCK}^3$ $\overline{LWR}$ $\overline{MODCK1}/\overline{AP}(1)/\overline{TC}(0)/\overline{BNKSEL}(0)$ $\overline{MODCK2}/\overline{AP}(2)/\overline{TC}(1)/\overline{BNKSEL}(1)$ $\overline{MODCK3}/\overline{AP}(3)/\overline{TC}(2)/\overline{BNKSEL}(2)$ $I_{OL} = 3.2\text{mA}$ $\overline{L_A14}/\overline{PAR}^3$ $\overline{L_A15}/\overline{FRAME}^3/\overline{SMI}$ $\overline{L_A16}/\overline{TRDY}^3$ $\overline{L_A17}/\overline{IRDY}^3/\overline{CKSTP_OUT}$ $\overline{L_A18}/\overline{STOP}^3$ $\overline{L_A19}/\overline{DEVSEL}^3$ $\overline{L_A20}/\overline{IDSEL}^3$ $\overline{L_A21}/\overline{PERR}^3$ $\overline{L_A22}/\overline{SERR}^3$ $\overline{L_A23}/\overline{REQ0}^3$ $\overline{L_A24}/\overline{REQ1}^3/\overline{HSEJSW}^3$ $\overline{L_A25}/\overline{GNT0}^3$ $\overline{L_A26}/\overline{GNT1}^3/\overline{HSLED}^3$ $\overline{L_A27}/\overline{GNT2}^3/\overline{HSENUM}^3$ $\overline{L_A28}/\overline{RST}^3/\overline{CORE_SRESET}$ $\overline{L_A29}/\overline{INTA}^3$ $\overline{L_A30}/\overline{REQ2}^3$ $\overline{L_A31}$ $\overline{LCL_D}(0-31)/\overline{AD}(0-31)^3$ $\overline{LCL_DP}(0-3)/\overline{C}/\overline{BE}(0-3)^3$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ $\overline{TDO}$	V_{OL}	—	0.4	V

¹ The default configuration of the CPM pins ($\overline{PA}[0-31]$, $\overline{PB}[4-31]$, $\overline{PC}[0-31]$, $\overline{PD}[4-31]$) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs¹

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

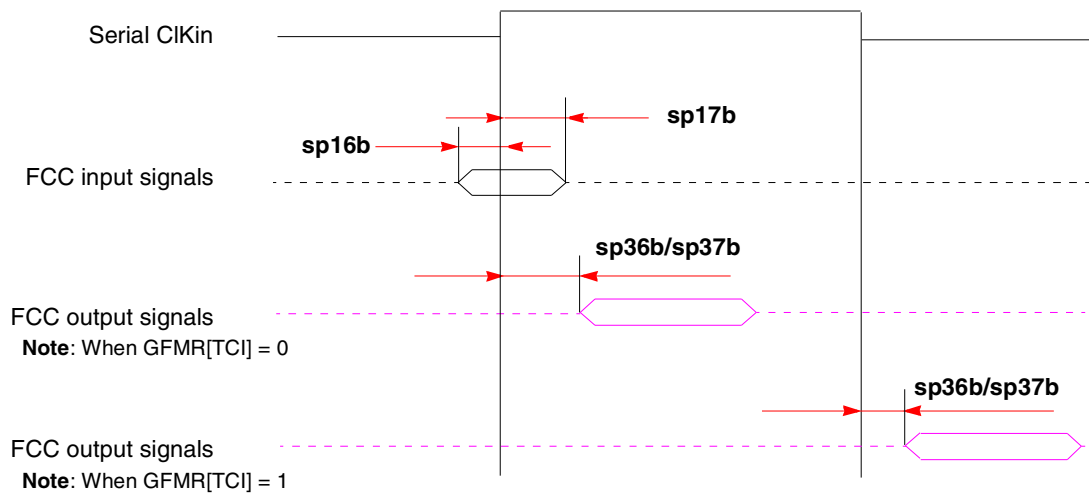


Figure 3. FCC External Clock Diagram

Table 12 lists the JTAG timings.

Table 12. JTAG Timings¹

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	25	MHz	—
JTAG external clock cycle time	t_{JTG}	40	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	20	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	6
TRST assert time	t_{TRST}	25	—	ns	3, 6
Input setup times	Boundary-scan data	t_{JTDVKH}	4	ns	4, 7
	TMS, TDI	t_{JTIVKH}	4	ns	4, 7
Input hold times	Boundary-scan data	t_{JTDXKH}	10	ns	4, 7
	TMS, TDI	t_{JTIXKH}	10	ns	4, 7
Output valid times	Boundary-scan data	t_{JTKLDV}	—	ns	5, 7
	TDO	t_{JTKLOV}	25	ns	5, 7
Output hold times	Boundary-scan data	t_{JTKLDX}	1	ns	5, 7
	TDO	t_{JTKLOX}	1	ns	5, 7
JTAG external clock to output high impedance	Boundary-scan data	t_{JTKLDZ}	1	ns	5, 6
	TDO	t_{JTKLOZ}	1	ns	5, 6

¹ All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

² The symbols used for timing specifications herein follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)}$ (reference)(state) for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

³ TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

⁴ Non-JTAG signal input timing with respect to t_{TCLK} .

⁵ Non-JTAG signal output timing with respect to t_{TCLK} .

⁶ Guaranteed by design.

⁷ Guaranteed by design and device characterization.

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

Table 14. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3}	CPM Multiplication Factor ²	CPM Frequency ²	Core Multiplication Factor ²	Core Frequency ²
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	33 MHz	4	133 MHz	4	133 MHz
0010_011	33 MHz	4	133 MHz	5	166 MHz
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					

Table 14. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3}	CPM Multiplication Factor ²	CPM Frequency ²	Core Multiplication Factor ²	Core Frequency ²
1000_001	66 MHz	3.5	233 MHz	3	200 MHz
1000_010	66 MHz	3.5	233 MHz	3.5	233 MHz
1000_011	66 MHz	3.5	233 MHz	4	266 MHz
1000_100	66 MHz	3.5	233 MHz	4.5	300 MHz

¹ Because of speed dependencies, not all of the possible configurations in Table 14 are applicable.

² The user should choose the input clock frequency and the multiplication factors such that the frequency of the CPU is equal to or greater than 150 MHz and the CPM ranges between 66–233 MHz.

³ Input clock frequency is given only for the purpose of reference. The user should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

3.2 PCI Mode

The MPC8265 and the MPC8266 have three clocking modes: local, PCI host, and PCI agent. The clocking mode is set according to three input pins—PCI_MODE, PCI_CFG[0], PCI_MODCK—as shown in Table 15.

Table 15. MPC8265 and MPC8266 Clocking Modes

Pins			Clocking Mode	PCI Clock Frequency Range (MHz)
PCI_MODE	PCI_CFG[0]	PCI_MODCK		
1	—	—	Local bus	—
0	0	0	PCI host	50–66
0	0	1		25–50
0	1	0	PCI agent	50–66
0	1	1		25–50

In addition, note the following:

NOTE: PCI_MODCK

In PCI mode only, PCI_MODCK comes from the LGPL5 pin and MODCK_H[0–3] comes from {LGPL0, LGPL1, LGPL2, LGPL3}.

NOTE: Tval (Output Hold)

The minimum Tval = 2 when PCI_MODCK = 1, and the minimum Tval = 1 when PCI_MODCK = 0. Therefore, designers should use clock configurations that fit this condition to achieve PCI-compliant AC timing.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.2.1 PCI Host Mode

The frequencies listed in [Table 16](#) and [Table 17](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 16. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3] ¹	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

¹ Assumes MODCK_HI = 0000.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to [Table 15](#).

[Table 17](#) describes all possible clock configurations when using the MPC8265's or the MPC8266's internal PCI bridge in host mode.

Table 17. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency ¹ (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	33 MHz	4	133 MHz	5	166 MHz	4/8	33/16 MHz
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000 ³	33 MHz	5	166 MHz	5	166 MHz	5	33 MHz
0011_001 ³	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz
0011_010 ³	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency ¹ (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

¹ Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to [Table 15](#).

³ In this mode, PCI_MODCK must be "0".

3.2.2 PCI Agent Mode

The frequencies listed in [Table 18](#) and [Table 19](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

MODCK[1–3] ¹	Input Clock Frequency (PCI) ²	CPM Multiplication Factor ²	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000) (continued)

MODCK[1–3] ¹	Input Clock Frequency (PCI) ²	CPM Multiplication Factor ²	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

¹ Assumes MODCK_HI = 0000.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to [Table 15](#).

³ Core frequency = (60x bus frequency)(core multiplication factor)

⁴ Bus frequency = CPM frequency/bus division factor

[Table 19](#) describes all possible clock configurations when using the MPC8265 or the MPC8266's internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) ^{1,2}	CPM Multiplication Factor ¹	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	150 MHz	3	180 MHz	2.5	60 MHz
0010_010	50/25 MHz	3/6	150 MHz	3.5	210 MHz	2.5	60 MHz
0010_011	50/25 MHz	3/6	150 MHz	4	240 MHz	2.5	60 MHz
0010_100	50/25 MHz	3/6	150 MHz	4.5	270 MHz	2.5	60 MHz
0011_000	66/33 MHz	2/4	133 MHz	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	133 MHz	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	133 MHz	3.5	154 MHz	3	44 MHz
0011_011	66/33 MHz	2/4	133 MHz	4	176MHz	3	44 MHz
0011_100	66/33 MHz	2/4	133 MHz	4.5	198 MHz	3	44 MHz
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	3	66 MHz
0100_001	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
0100_010	66/33 MHz	3/6	200 MHz	3.5	233 MHz	3	66 MHz
0100_011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)^{1,2}	CPM Multiplication Factor¹	CPM Frequency	Core Multiplication Factor	Core Frequency³	Bus Division Factor	60x Bus Frequency⁴
0100_100	66/33 MHz	3/6	200 MHz	4.5	300 MHz	3	66 MHz
0101_000 ⁵	33 MHz	5	166 MHz	2.5	166 MHz	2.5	66 MHz
0101_001 ⁵	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010 ⁵	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011 ⁵	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100 ⁵	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) ^{1,2}	CPM Multiplication Factor ¹	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

- ¹ The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to [Table 15](#).
- ² Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.
- ³ Core frequency = (60x bus frequency)(core multiplication factor)
- ⁴ Bus frequency = CPM frequency/bus division factor
- ⁵ In this mode, PCI_MODCK must be "1".

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

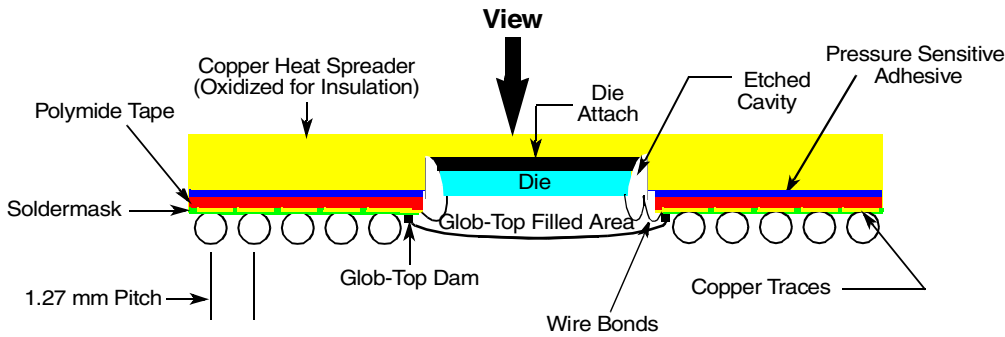


Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

Table 21. Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2

Table 21. Pinout List (continued)

Pin Name	Ball
L_A28/RST ¹ /CORE_SRESET	AB29
L_A29/INTA ¹	AB28
L_A30/REQ2 ¹	P25
L_A31/DLLOUT ¹	AB27
LCL_D0/AD0 ¹	H29
LCL_D1/AD1 ¹	J29
LCL_D2/AD2 ¹	J28
LCL_D3/AD3 ¹	J27
LCL_D4/AD4 ¹	J26
LCL_D5/AD5 ¹	J25
LCL_D6/AD6 ¹	K25
LCL_D7/AD7 ¹	L29
LCL_D8/AD8 ¹	L27
LCL_D9/AD9 ¹	L26
LCL_D10/AD10 ¹	L25
LCL_D11/AD11 ¹	M29
LCL_D12/AD12 ¹	M28
LCL_D13/AD13 ¹	M27
LCL_D14/AD14 ¹	M26
LCL_D15/AD15 ¹	N29
LCL_D16/AD16 ¹	T25
LCL_D17/AD17 ¹	U27
LCL_D18/AD18 ¹	U26
LCL_D19/AD19 ¹	U25
LCL_D20/AD20 ¹	V29
LCL_D21/AD21 ¹	V28
LCL_D22/AD22 ¹	V27
LCL_D23/AD23 ¹	V26
LCL_D24/AD24 ¹	W27
LCL_D25/AD25 ¹	W26
LCL_D26/AD26 ¹	W25
LCL_D27/AD27 ¹	Y29
LCL_D28/AD28 ¹	Y28
LCL_D29/AD29 ¹	Y25
LCL_D30/AD30 ¹	AA29

Table 21. Pinout List (continued)

Pin Name	Ball
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21 ²
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20 ²
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19 ²
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18 ²
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17 ²
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16 ²
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16 ²
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15 ²
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13 ²
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13 ²
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12 ²
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11 ²
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9 ²
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8 ²
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7 ²
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7 ²
PA28/FCC1_UTM_RXENB/FCC1_UTS_RXENB/FCC1_MII_TX_EN	AD5 ²
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1 ²
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/ FCC1_RTS	AD3 ²
PA31/FCC1_UTM_TXENB/FCC1_UTS_TXENB/FCC1_MII_COL	AB5 ²
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/FCC3_RTS	AD28 ²
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26 ²
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25 ²
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26 ²
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27 ²
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24 ²
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24 ²
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24 ²
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22 ²
PB13/FCC3_MII_COL/L1RQB1/L1TSYNCC1/L1GNTE1/L1TXD1A2	AH21 ²
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20 ²
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19 ²
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18 ²
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17 ²

Table 21. Pinout List (continued)

Pin Name	Ball
PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14 ²
PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13 ²
PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12 ²
PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2/L1TXD2A1	AH11 ²
PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_TXD/L1RXD1A1/L1RXDD2	AH16 ²
PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1TXDD2	AE15 ²
PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2	AJ9 ²
PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9 ²
PB26/FCC2_MII_CRD/FCC2_UT8_TXD1/L1RXDC2	AJ7 ²
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6 ²
PB28/FCC2_MII_RX_ER/FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1	AE3 ²
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/FCC2_MII_TX_EN	AE2 ²
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2	AC5 ²
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4 ²
PC0/DREQ1/BRGO7/SMSYN2/L1CLKOA2	AB26 ²
PC1/DREQ2/BRGO6/L1RQA2	AD29 ²
PC2/FCC3_CD/FCC2_UT8_TXD3/DONE2	AE29 ²
PC3/FCC3_CTS/FCC2_UT8_TXD2/DACK2/CTS4	AE27 ²
PC4/FCC2_UTM_RXENB/FCC2_UTS_RXENB/SI2_L1ST4/FCC2_CD	AF27 ²
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/FCC2_CTS	AF24 ²
PC6/FCC1_CD/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR/FCC1_UTM_RXCLAV1	AJ26 ²
PC7/FCC1_CTS/L1RQC1/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/FCC1_UTM_TXCLAV1	AJ25 ²
PC8/CD4/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/CTS3	AF22 ²
PC9/CTS4/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21 ²
PC10/CD3/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AF20 ²
PC11/CTS3/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19 ²
PC12/CD2/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18 ²
PC13/CTS2/CLSN2/L1RQD1/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18 ²
PC14/CD1/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17 ²
PC15/CTS1/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16 ²

Table 21. Pinout List (continued)

Pin Name	Ball
PC16/CLK16/TIN4	AF15 ²
PC17/CLK15/TIN3/BRGO8	AJ15 ²
PC18/CLK14/ $\overline{\text{TGATE2}}$	AH14 ²
PC19/CLK13/BRGO7/SPICLK	AG13 ²
PC20/CLK12/ $\overline{\text{TGATE1}}$	AH12 ²
PC21/CLK11/BRGO6	AJ11 ²
PC22/CLK10/ $\overline{\text{DONE1}}$	AG10 ²
PC23/CLK9/BRGO5/ $\overline{\text{DACK1}}$	AE10 ²
PC24/FCC2_UT8_TXD3/CLK8/ $\overline{\text{TOUT4}}$	AF9 ²
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8 ²
PC26/CLK6/ $\overline{\text{TOUT3}}$ /TMCLK	AJ6 ²
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2 ²
PC28/CLK4/TIN1/ $\overline{\text{TOUT2}}$ / $\overline{\text{CTS2}}$ /CLSN2	AF3 ²
PC29/CLK3/TIN2/BRGO2/ $\overline{\text{CTS1}}$ /CLSN1	AF2 ²
PC30/FCC2_UT8_TXD3/CLK2/ $\overline{\text{TOUT1}}$	AE1 ²
PC31/CLK1/BRGO1	AD1 ²
PD4/BRGO8/L1TSYNCD1/L1GNTD1/ $\overline{\text{FCC3_RTS}}$ /SMRXD2	AC28 ²
PD5/FCC1_UT16_TXD3/ $\overline{\text{DONE1}}$	AD27 ²
PD6/FCC1_UT16_TXD4/ $\overline{\text{DACK1}}$	AF29 ²
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4/FCC1_TXCLAV2	AF28 ²
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25 ²
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26 ²
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27 ²
PD11/ $\overline{\text{L1RQB2}}$ /FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23 ²
PD12/SI1_L1ST2/L1RXDB1	AG23 ²
PD13/SI1_L1ST1/L1TXDB1	AJ22 ²
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20 ²
PD15/FCC1_UT16_RXD1/ $\overline{\text{L1RQC2}}$ /I2CSDA	AJ20 ²
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18 ²
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17 ²
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/FCC2_UTM_RXADDR3/SPICLK	AF16 ²
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/FCC2_UTM_TXADDR3/SPISEL/BRGO1	AH15 ²
PD20/ $\overline{\text{RTS4}}$ /TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14 ²

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