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Understanding Embedded - Microprocessors

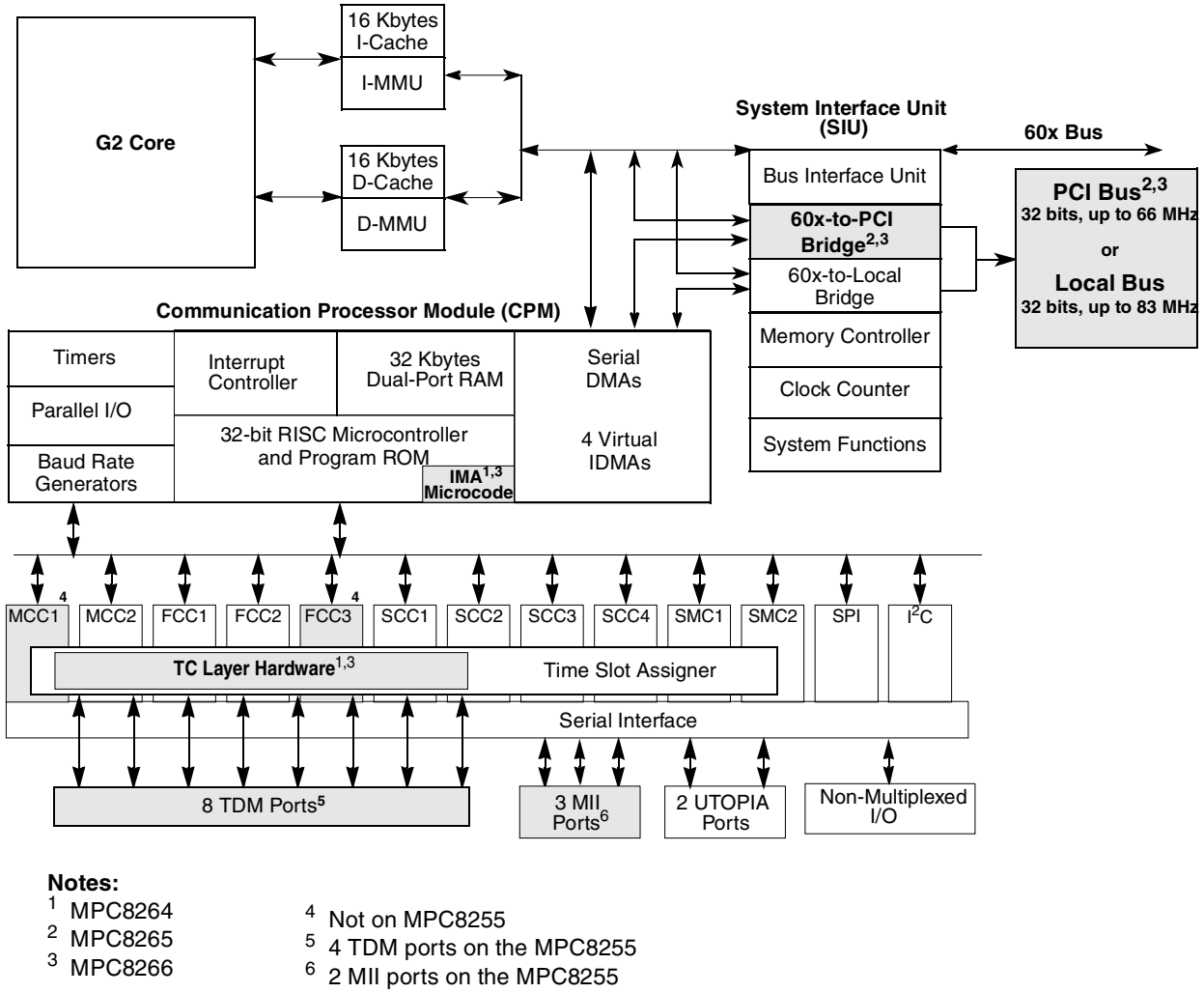
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8260aczumhbb

Figure 1 shows the block diagram for the MPC8266, the HiP4 superset device. Shaded portions indicate functionality that is not available on all devices; refer to the notes.



Notes:
1 MPC8264
2 MPC8265
3 MPC8266
4 Not on MPC8255
5 4 TDM ports on the MPC8255
6 2 MII ports on the MPC8255

Figure 1. MPC8266 Block Diagram

1 Features

The major features of the MPC826xA family are as follows:

- Dual-issue integer core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 150–300 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm

  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
    - 10/100-Mbit Ethernet/IEEE Std. 802.3® CDMA/CS interface through media independent interface (MII)
    - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
    - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels.Each MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

- Coset removing (programmable by the user)
- Filtering idle/unassigned cells (programmable by the user)
- Performing HEC error detection and single bit error correction (programmable by user)
- Generating loss of cell delineation status/interrupt (LOC/LCD)

— Operates with FCC2 (UTOPIA 8)
— Provides serial loop back mode
— Cell echo mode is provided
— Supports both FCC transmit modes
  – External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
  – Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.
— Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
— Cell counters for performance monitoring
  – 16-bit counters count
    - HEC error cells
    - HEC single bit error and corrected cells
    - Idle/unassigned cells filtered
    - Idle/unassigned cells transmitted
    - Transmitted ATM cells
    - Received ATM cells
  – Maskable interrupt is sent to the host when a counter expires
— Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
— May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported

- PCI bridge (MPC8265 and MPC8266 only)
  — PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
  — On-chip arbitration
  — Support for PCI to 60x memory and 60x memory to PCI streaming
  — PCI Host Bridge or Peripheral capabilities
  — Includes 4 DMA channels for the following transfers:
    – PCI-to-60x to 60x-to-PCI
    – 60x-to-PCI to PCI-to-60x
    – PCI-to-60x to PCI-to-60x
    – 60x-to-PCI to 60x-to-PCI
  — Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265) required by the PCI standard as well as message and doorbell registers
  — Supports the I_2O standard

— Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
— Support for 66 MHz, 3.3 V specification
— 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
— Makes use of the local bus signals, so there is no need for additional pins

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC826xA.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC826xA. Table 1 shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings[1]

Rating	Symbol	Value	Unit
Core supply voltage[2]	VDD	–0.3 – 2.5	V
PLL supply voltage[2]	VCCSYN	–0.3 – 2.5	V
I/O supply voltage[3]	VDDH	–0.3 – 4.0	V
Input voltage[4]	VIN	GND(–0.3) – 3.6	V
Junction temperature	T_j	120	°C
Storage temperature range	T_{STG}	(–55) – (+150)	°C

1 Absolute maximum ratings are stress ratings only; functional operation (see Table 2) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.
2 **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.
3 **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.
4 **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3][3] LSDA10/LGPL0/PCI_MODCKH0[3] LSDWE/LGPL1/PCI_MODCKH1[3] LOE/LSDRAS/LGPL2/PCI_MODCKH2[3] LSDCAS/LGPL3/PCI_MODCKH3[3] LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK[3] LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2)	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR[3] L_A15/FRAME[3]/SMI L_A16/TRDY[3] L_A17/IRDY[3]/CKSTP_OUT L_A18/STOP[3] L_A19/DEVSEL[3] L_A20/IDSEL[3] L_A21/PERR[3] L_A22/SERR[3] L_A23/REQ0[3] L_A24/REQ1[3]/HSEJSW[3] L_A25/GNT0[3] L_A26/GNT1[3]/HSLED[3] L_A27/GNT2[3]/HSENUM[3] L_A28/RST[3]/CORE_SRESET L_A29/INTA[3] L_A30/REQ2[3] L_A31 LCL_D(0-31)/AD(0-31)[3] LCL_DP(0-3)/C/BE(0-3)[3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO				

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2 The leakage current is measured for nominal VDD, VCCSYN, and VDD.
3 MPC8265 and MPC8266 only.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics for 480 TBGA Package

Characteristics	Symbol	Value	Unit	Air Flow
Junction to ambient	θ_{JA}	13[1]	°C/W	NC[2]
		10[1]		1 m/s
		11[3]		NC
		8[3]		1 m/s
Junction to board[4]	θ_{JB}	4	°C/W	—
Junction to case[5]	θ_{JC}	1.1	°C/W	—

1 Assumes a single layer board with no thermal vias
2 Natural convection
3 Assumes a four layer board
4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K/(T_J + 273° C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273° C) + \theta_{JA} \times P_D^2 \quad (3)$$

Figure 4 shows the FCC internal clock.

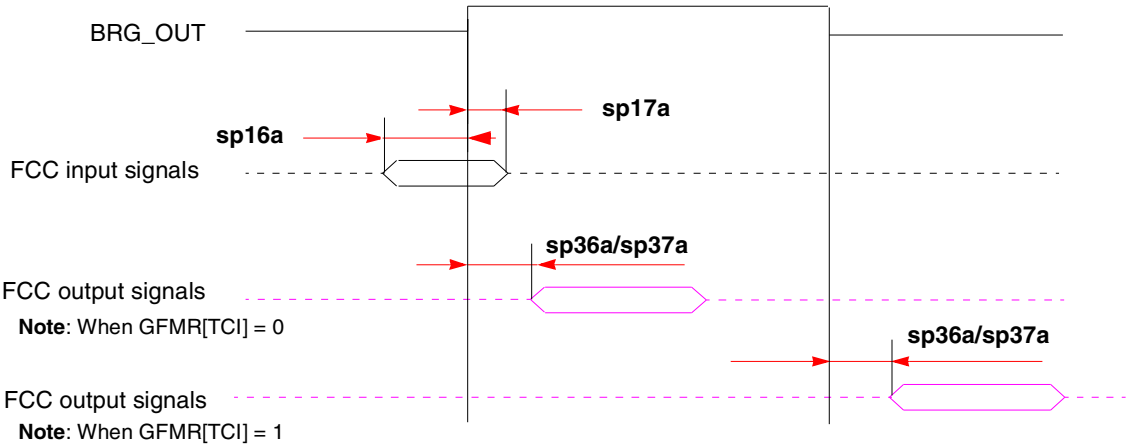
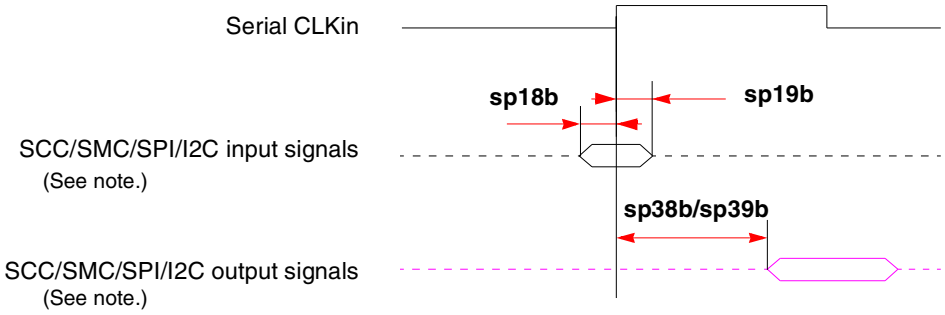


Figure 4. FCC Internal Clock Diagram

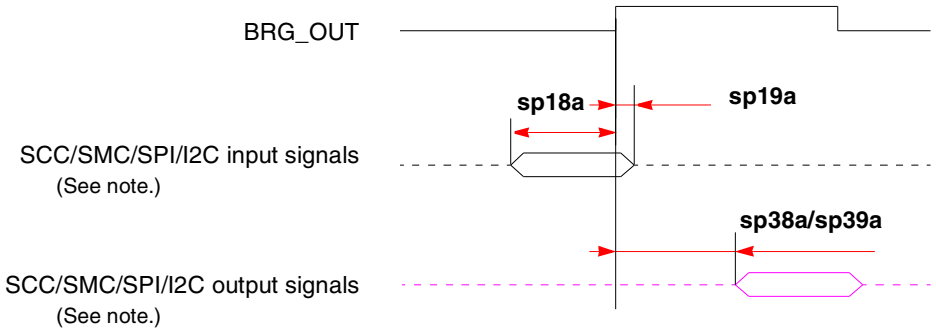
Figure 5 shows the SCC/SMC/SPI/I^2C external clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^2C External Clock Diagram

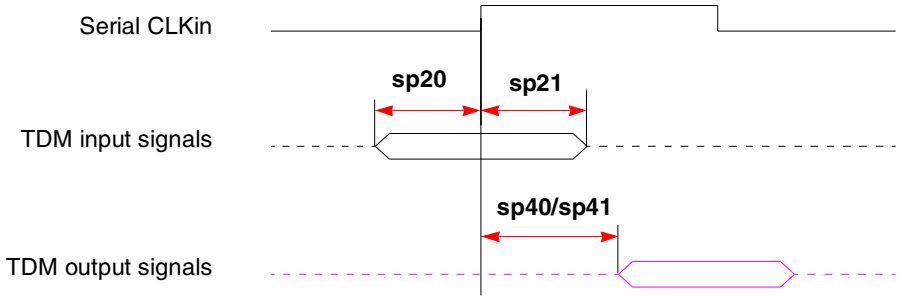
Figure 6 shows the SCC/SMC/SPI/I^{2}C internal clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I^{2}C Internal Clock Diagram

Figure 7 shows TDM input and output signals.



Note: There are four possible TDM timing conditions:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

Table 12 lists the JTAG timings.

Table 12. JTAG Timings[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	25	MHz	—
JTAG external clock cycle time	t_{JTG}	40	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	20	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	6
TRST assert time	t_{TRST}	25	—	ns	3, 6
Input setup times Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	 ns ns	 4, 7 4, 7
Input hold times Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	 ns ns	 4, 7 4, 7
Output valid times Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 — —	 25 25	 ns ns	 5, 7 5. 7
Output hold times Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 1 1	 — —	 ns ns	 5, 7 5, 7
JTAG external clock to output high impedance Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 1 1	 25 25	 ns ns	 5, 6 5, 6

1 All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{((first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to t_{TCLK}.

5 Non-JTAG signal output timing with respect to t_{TCLK}.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin's rising edge.

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 13 lists the eight basic configuration modes. Table 14 lists the other modes that are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four bits from hardware configuration word on the data bus.

Note that the MPC8265 and the MPC8266 have two additional clocking modes—PCI agent and PCI host. Refer to Section 3.2, “PCI Mode” on page 26 for information.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 13 describes default clock modes for the MPC826xA.

Table 13. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note that basic modes are shown in boldface type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

Table 14. Clock Configuration Modes[1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

Table 14. Clock Configuration Modes[1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	**33 MHz**	**4**	**133 MHz**	**4**	**133 MHz**
0010_011	**33 MHz**	**4**	**133 MHz**	**5**	**166 MHz**
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

1 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to Table 15.

3 In this mode, PCI_MODCK must be "0".

3.2.2 PCI Agent Mode

The frequencies listed in Table 18 and Table 19 are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000[5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

1 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.

2 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user’s part.

3 Core frequency = (60x bus frequency)(core multiplication factor)

4 Bus frequency = CPM frequency/bus division factor

5 In this mode, PCI_MODCK must be “1”.

Table 21. Pinout List (continued)

Pin Name	Ball
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	E21

Table 21. Pinout List (continued)

Pin Name	Ball
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
$\overline{\text{PSDWE}}$/PGPL1	B24
$\overline{\text{POE}}$/$\overline{\text{PSDRAS}}$/PGPL2	A24
$\overline{\text{PSDCAS}}$/PGPL3	B23
$\overline{\text{PGTA}}$/PUPMWAIT/PGPL4/$\overline{\text{PPBS}}$	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/$\overline{\text{LBS0}}$/PCI_CFG0[1]	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1[1]	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2[1]	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3[1]	G29
LSDA10/LGPL0/PCI_MODCKH0[1]	D27
$\overline{\text{LSDWE}}$/LGPL1/PCI_MODCKH1[1]	C28
$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$/LGPL2/PCI_MODCKH2[1]	E26
$\overline{\text{LSDCAS}}$/LGPL3/PCI_MODCKH3[1]	D25
$\overline{\text{LGTA}}$/LUPMWAIT/LGPL4/$\overline{\text{LPBS}}$	C26
LGPL5/LSDAMUX/PCI_MODCK[1]	B27
LWR	D28
L_A14/PAR[1]	N27
L_A15/$\overline{\text{FRAME}}$[1]/$\overline{\text{SMI}}$	T29
L_A16/$\overline{\text{TRDY}}$[1]	R27
L_A17/$\overline{\text{IRDY}}$[1]/$\overline{\text{CKSTP\_OUT}}$	R26
L_A18/$\overline{\text{STOP}}$[1]	R29
L_A19/$\overline{\text{DEVSEL}}$[1]	R28
L_A20/IDSEL[1]	W29
L_A21/$\overline{\text{PERR}}$[1]	P28
L_A22/$\overline{\text{SERR}}$[1]	N26
L_A23/$\overline{\text{REQ0}}$[1]	AA27
L_A24/$\overline{\text{REQ1}}$[1]/HSEJSW[1]	P29
L_A25/$\overline{\text{GNT0}}$[1]	AA26
L_A26/$\overline{\text{GNT1}}$[1]/HSLED[1]	N25
L_A27/$\overline{\text{GNT2}}$[1]/$\overline{\text{HSENUM}}$[1]	AA25

Table 21. Pinout List (continued)

Pin Name	Ball
LCL_D31/AD31[1]	AA28
LCL_DP0/C0[1]/$\overline{\text{BE0}}$[1]	L28
LCL_DP1/C1[1]/$\overline{\text{BE1}}$[1]	N28
LCL_DP2/C2[1]/$\overline{\text{BE2}}$[1]	T28
LCL_DP3/C3[1]/$\overline{\text{BE3}}$[1]	W28
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3/FCC2_UTM_TXADDR2	AC29[2]
PA1/$\overline{\text{REJECT1}}$/FCC2_UTM_TXADDR1/$\overline{\text{DONE3}}$	AC25[2]
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{\text{DACK3}}$	AE28[2]
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{\text{DACK4}}$/L1RXD1A2	AG29[2]
PA4/$\overline{\text{REJECT2}}$/FCC2_UTM_RXADDR1/$\overline{\text{DONE4}}$	AG28[2]
PA5/$\overline{\text{RESTART2}}$/DREQ4/FCC2_UTM_RXADDR2	AG26[2]
PA6/L1RSYNCA1	AE24[2]
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2/L1TXD0A1	AH23[2]
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22[2]
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22[2]

Table 21. Pinout List (continued)

Pin Name	Ball
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21[2]
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20[2]
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19[2]
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18[2]
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17[2]
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16[2]
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16[2]
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15[2]
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13[2]
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13[2]
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12[2]
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11[2]
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9[2]
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8[2]
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7[2]
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7[2]
PA28/$\overline{\text{FCC1\_UTM\_RXENB}}$/$\overline{\text{FCC1\_UTS\_RXENB}}$/FCC1_MII_TX_EN	AD5[2]
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1[2]
PA30/$\overline{\text{FCC1\_UTM\_TXCLAV}}$/FCC1_UTS_TXCLAV/FCC1_MII_CRS/ $\overline{\text{FCC1\_RTS}}$	AD3[2]
PA31/$\overline{\text{FCC1\_UTM\_TXENB}}$/$\overline{\text{FCC1\_UTS\_TXENB}}$/FCC1_MII_COL	AB5[2]
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	AD28[2]
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26[2]
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25[2]
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26[2]
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27[2]
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24[2]
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24[2]
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22[2]
PB13/FCC3_MII_COL/$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21[2]
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19[2]
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18[2]
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17[2]

Table 21. Pinout List (continued)

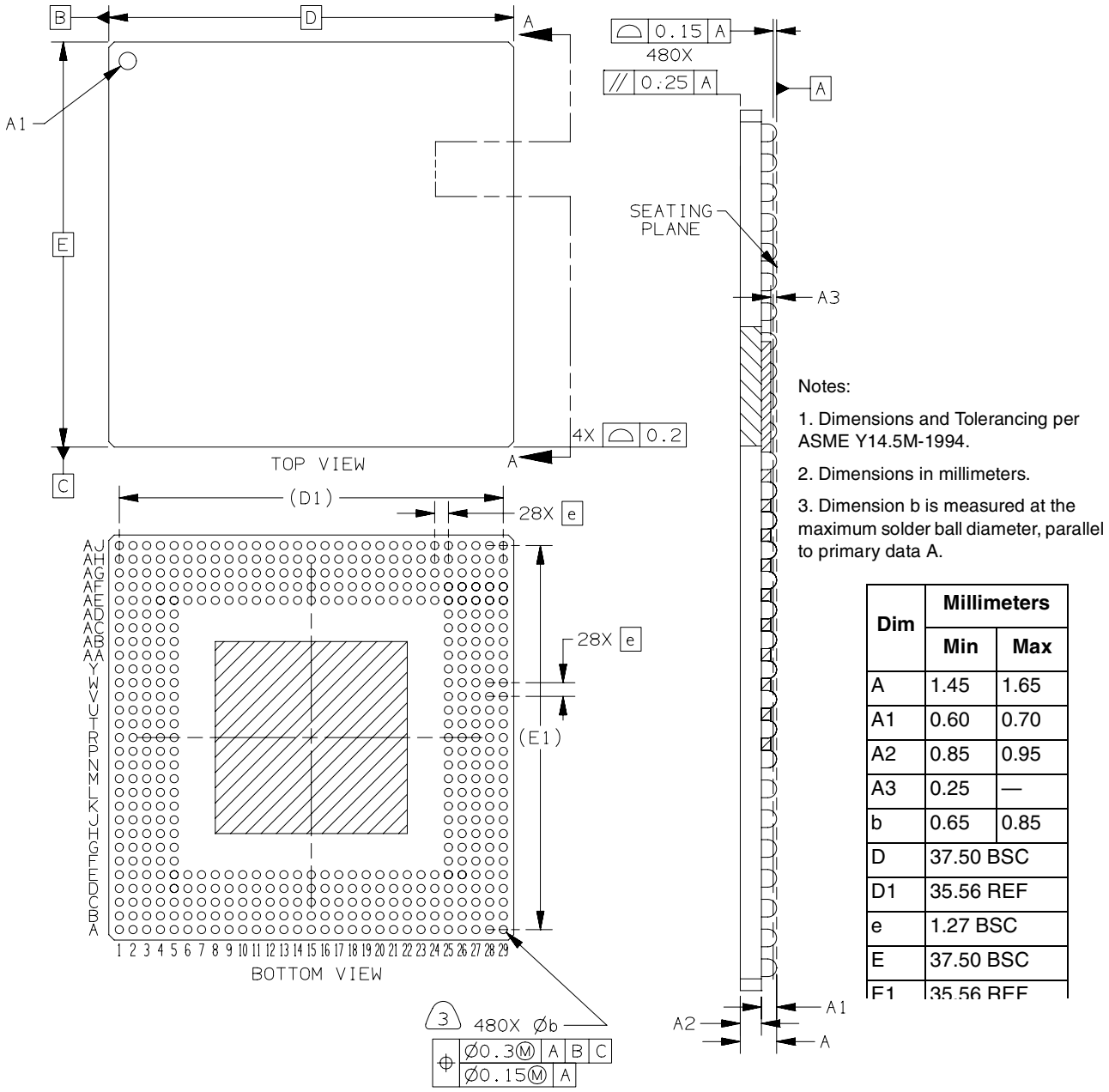
Pin Name	Ball
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13[2]
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12[2]
PD23/$\overline{\text{RTS3}}$/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12[2]
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10[2]
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9[2]
PD26/$\overline{\text{RTS2}}$/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8[2]
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7[2]
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4[2]
PD29/$\overline{\text{RTS1}}$/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4	AG1[2]
PD30/$\overline{\text{FCC2\_UTM\_TXENB}}$/$\overline{\text{FCC2\_UTS\_TXENB}}$/TXD1	AD4[2]
PD31/RXD1	AD2[2]
VCCSYN	AB3
VCCSYN1	B9
GNDSYN	AB1
CLKIN2[1,3]	AE11
SPARE4[4]	U5
$\overline{\text{PCI\_MODE}}$[1,5]	AF25
SPARE6[4]	V4
THERMAL0[6]	AA1
THERMAL1[6]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 MPC8265 and MPC8266 only.

2 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature