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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8260aczumibb

- — PowerPC architecture-compliant memory management unit (MMU)
- — Common on-chip processor (COP) test interface
- — High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPs/MHz without inlining and 1.90 Dhrystones MIPS/MHz with
- — Supports bus snooping for data cache coherency
- — Floating-point unit (FPU)

• Separate power supply for internal logic and for I/O

• Separate PLLs for G2 core and for the CPM
  - — G2 core and CPM can run at different frequencies for power/performance optimization
  - — Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - — Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios

• 64-bit data and 32-bit address 60x bus
  - — Bus supports multiple master designs
  - — Supports single- and four-beat burst transfers
  - — 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - — Supports data parity or ECC and address parity

• 32-bit data and 18-bit address local bus
  - — Single-master bus, supports external slaves
  - — Eight-beat burst transfers
  - — 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller

• 60x-to-PCI bridge (MPC8265 and MPC8266 only)
  - — Programmable host bridge and agent
  - — 32-bit data bus, 66 MHz, 3.3 V
  - — Synchronous and asynchronous 60x and PCI clock modes
  - — All internal address space available to external PCI host
  - — DMA for memory block transfers
  - — PCI-to-60x address remapping

• System interface unit (SIU)
  - — Clock synthesizer
  - — Reset controller
  - — Real-time clock (RTC) register
  - — Periodic interrupt timer
  - — Hardware bus monitor and software watchdog timer
  - — IEEE Std. 1149.1™ standard JTAG test access port

• Twelve-bank memory controller
  - — Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - — Byte write enables and selectable parity generation

  - Coset removing (programmable by the user)
  - Filtering idle/unassigned cells (programmable by the user)
  - Performing HEC error detection and single bit error correction (programmable by user)
  - Generating loss of cell delineation status/interrupt (LOC/LCD)
- — Operates with FCC2 (UTOPIA 8)
- — Provides serial loop back mode
- — Cell echo mode is provided
- — Supports both FCC transmit modes
  - – External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
  - – Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.
- — Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
- — Cell counters for performance monitoring
  - – 16-bit counters count
    - HEC error cells
    - HEC single bit error and corrected cells
    - Idle/unassigned cells filtered
    - Idle/unassigned cells transmitted
    - Transmitted ATM cells
    - Received ATM cells
  - – Maskable interrupt is sent to the host when a counter expires
- — Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
- — May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported

• PCI bridge (MPC8265 and MPC8266 only)
- — PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
- — On-chip arbitration
- — Support for PCI to 60x memory and 60x memory to PCI streaming
- — PCI Host Bridge or Peripheral capabilities
- — Includes 4 DMA channels for the following transfers:
  - – PCI-to-60x to 60x-to-PCI
  - – 60x-to-PCI to PCI-to-60x
  - – PCI-to-60x to PCI-to-60x
  - – 60x-to-PCI to 60x-to-PCI
- — Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265) required by the PCI standard as well as message and doorbell registers
- — Supports the I_2O standard

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0 mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3][3] LSDA10/LGPL0/PCI_MODCKH0[3] LSDWE/LGPL1/PCI_MODCKH1[3] LOE/LSDRAS/LGPL2/PCI_MODCKH2[3] LSDCAS/LGPL3/PCI_MODCKH3[3] LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK[3] LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2) I_{OL} = 3.2mA L_A14/PAR[3] L_A15/FRAME[3]/SMI L_A16/TRDY[3] L_A17/IRDY[3]/CKSTP_OUT L_A18/STOP[3] L_A19/DEVSEL[3] L_A20/IDSEL[3] L_A21/PERR[3] L_A22/SERR[3] L_A23/REQ0[3] L_A24/REQ1[3]/HSEJSW[3] L_A25/GNT0[3] L_A26/GNT1[3]/HSLED[3] L_A27/GNT2[3]/HSENUM[3] L_A28/RST[3]/CORE_SRESET L_A29/INTA[3] L_A30/REQ2[3] L_A31 LCL_D(0-31)/AD(0-31)[3] LCL_DP(0-3)/C/BE(0-3)[3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO	V_{OL}	—	0.4	V

[1] The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

[2] The leakage current is measured for nominal VDD, VCCSYN, and VDD.
[3] MPC8265 and MPC8266 only.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics for 480 TBGA Package

Characteristics	Symbol	Value	Unit	Air Flow
Junction to ambient	θ_{JA}	13[1]	°C/W	NC[2]
		10[1]		1 m/s
		11[3]		NC
		8[3]		1 m/s
Junction to board[4]	θ_{JB}	4	°C/W	—
Junction to case[5]	θ_{JC}	1.1	°C/W	—

[1] Assumes a single layer board with no thermal vias
[2] Natural convection
[3] Assumes a four layer board
[4] Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K/(T_J + 273° C) \qquad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273° C) + \theta_{JA} \times P_D^2 \qquad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC826xA have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3 W (when the ambient temperature is 70 °C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W)[2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

1 Test temperature = room temperature (25° C)

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC826xA device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

Table 6. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

[1] These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

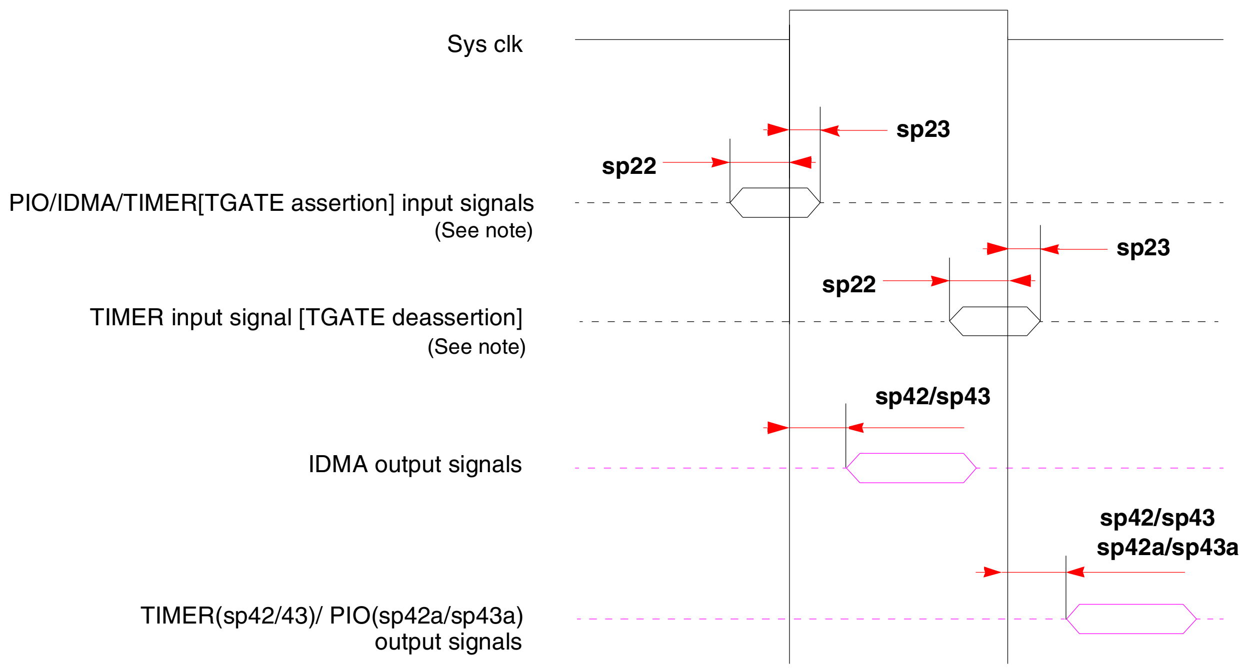
Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs[1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

[1] Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 10 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	$\overline{AACK}/\overline{ARTRY}/\overline{TA}/\overline{TS}/\overline{TEA}/\overline{DBG}/\overline{BG}/\overline{BR}$	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

[1] Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Figure 11 shows signal behavior in MEMC mode.

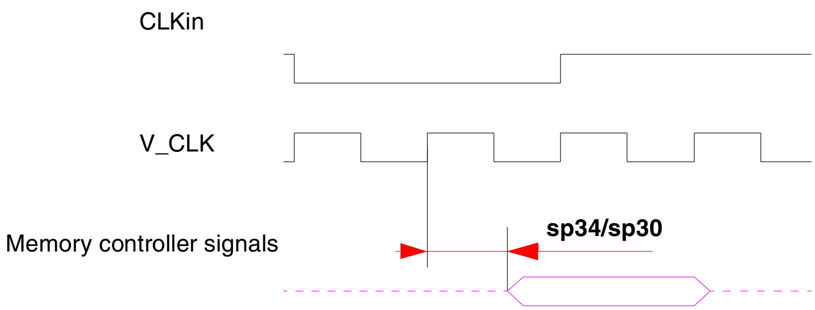


Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC826xA bus and system output signals are driven from the rising edge of the input clock (CLKin). Memory controller signals, however, trigger on four points within a CLKin cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKin. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKin)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKin	1/2 CLKin	3/4 CLKin
1:2.5	3/10 CLKin	1/2 CLKin	8/10 CLKin
1:3.5	4/14 CLKin	1/2 CLKin	11/14 CLKin

Figure 12 is a graphical representation of Table 11.

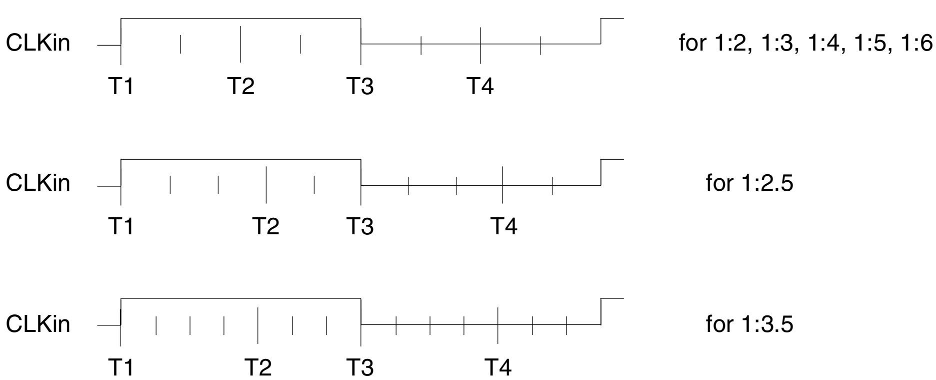


Figure 12. Internal Tick Spacing for Memory Controller Signals

Table 12 lists the JTAG timings.

Table 12. JTAG Timings[1]

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	25	MHz	—
JTAG external clock cycle time	t_{JTG}	40	—	ns	—
JTAG external clock pulse width measured at 1.4V	t_{JTKHKL}	20	—	ns	—
JTAG external clock rise and fall times	t_{JTGR} and t_{JTGF}	0	5	ns	6
TRST assert time	t_{TRST}	25	—	ns	3, 6
Input setup times					
Boundary-scan data	t_{JTDVKH}	4	—	ns	4, 7
TMS, TDI	t_{JTIVKH}	4	—	ns	4, 7
Input hold times					
Boundary-scan data	t_{JTDXKH}	10	—	ns	4, 7
TMS, TDI	t_{JTIXKH}	10	—	ns	4, 7
Output valid times					
Boundary-scan data	t_{JTKLDV}	—	25	ns	5, 7
TDO	t_{JTKLOV}	—	25	ns	5. 7
Output hold times					
Boundary-scan data	t_{JTKLDX}	1	—	ns	5, 7
TDO	t_{JTKLOX}	1	—	ns	5, 7
JTAG external clock to output high impedance					
Boundary-scan data	t_{JTKLDZ}	1	25	ns	5, 6
TDO	t_{JTKLOZ}	1	25	ns	5, 6

1 All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2 The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{((first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

3 TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4 Non-JTAG signal input timing with respect to t_{TCLK}.

5 Non-JTAG signal output timing with respect to t_{TCLK}.

6 Guaranteed by design.

7 Guaranteed by design and device characterization.

NOTE

The UPM machine outputs change on the internal tick determined by the memory controller programming; the AC specifications are relative to the internal tick. Note that SDRAM and GPCM machine outputs change on CLKin’s rising edge.

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while HRESET is asserted. Table 13 lists the eight basic configuration modes. Table 14 lists the other modes that are available by using the configuration pin (RSTCONF) and driving four bits from hardware configuration word on the data bus.

Note that the MPC8265 and the MPC8266 have two additional clocking modes—PCI agent and PCI host. Refer to Section 3.2, “PCI Mode” on page 26 for information.

NOTE

Clock configurations change only after POR is asserted.

3.1 Local Bus Mode

Table 13 describes default clock modes for the MPC826xA.

Table 13. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note that basic modes are shown in boldface type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

Table 14. Clock Configuration Modes[1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2**/4	**66**/33 **MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	3/6	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000) (continued)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

1 Assumes MODCK_HI = 0000.
2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.
3 Core frequency = (60x bus frequency)(core multiplication factor)
4 Bus frequency = CPM frequency/bus division factor

Table 19 describes all possible clock configurations when using the MPC8265 or the MPC8266’s internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	**150 MHz**	3	180 MHz	2.5	**60 MHz**
0010_010	50/25 MHz	3/6	**150 MHz**	3.5	210 MHz	2.5	**60 MHz**
0010_011	50/25 MHz	3/6	**150 MHz**	4	240 MHz	2.5	**60 MHz**
0010_100	50/25 MHz	3/6	**150 MHz**	4.5	270 MHz	2.5	**60 MHz**
0011_000	66/33 MHz	2/4	**133 MHz**	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	**133 MHz**	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	**133 MHz**	3.5	154 MHz	3	**44 MHz**
0011_011	66/33 MHz	2/4	**133 MHz**	4	176MHz	3	**44 MHz**
0011_100	66/33 MHz	2/4	**133 MHz**	4.5	198 MHz	3	**44 MHz**
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	**3**	66 MHz
0100_001	66/33 MHz	3/6	**200 MHz**	3	200 MHz	**3**	**66 MHz**
0100_010	66/33 MHz	3/6	**200 MHz**	3.5	233 MHz	**3**	**66 MHz**
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000[5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

1 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.

2 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user’s part.

3 Core frequency = (60x bus frequency)(core multiplication factor)

4 Bus frequency = CPM frequency/bus division factor

5 In this mode, PCI_MODCK must be “1”.

4 Pinout

This section provides the pin assignments and pinout list for the MPC826xA.

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC826xA's 480 TBGA package as viewed from the top surface.

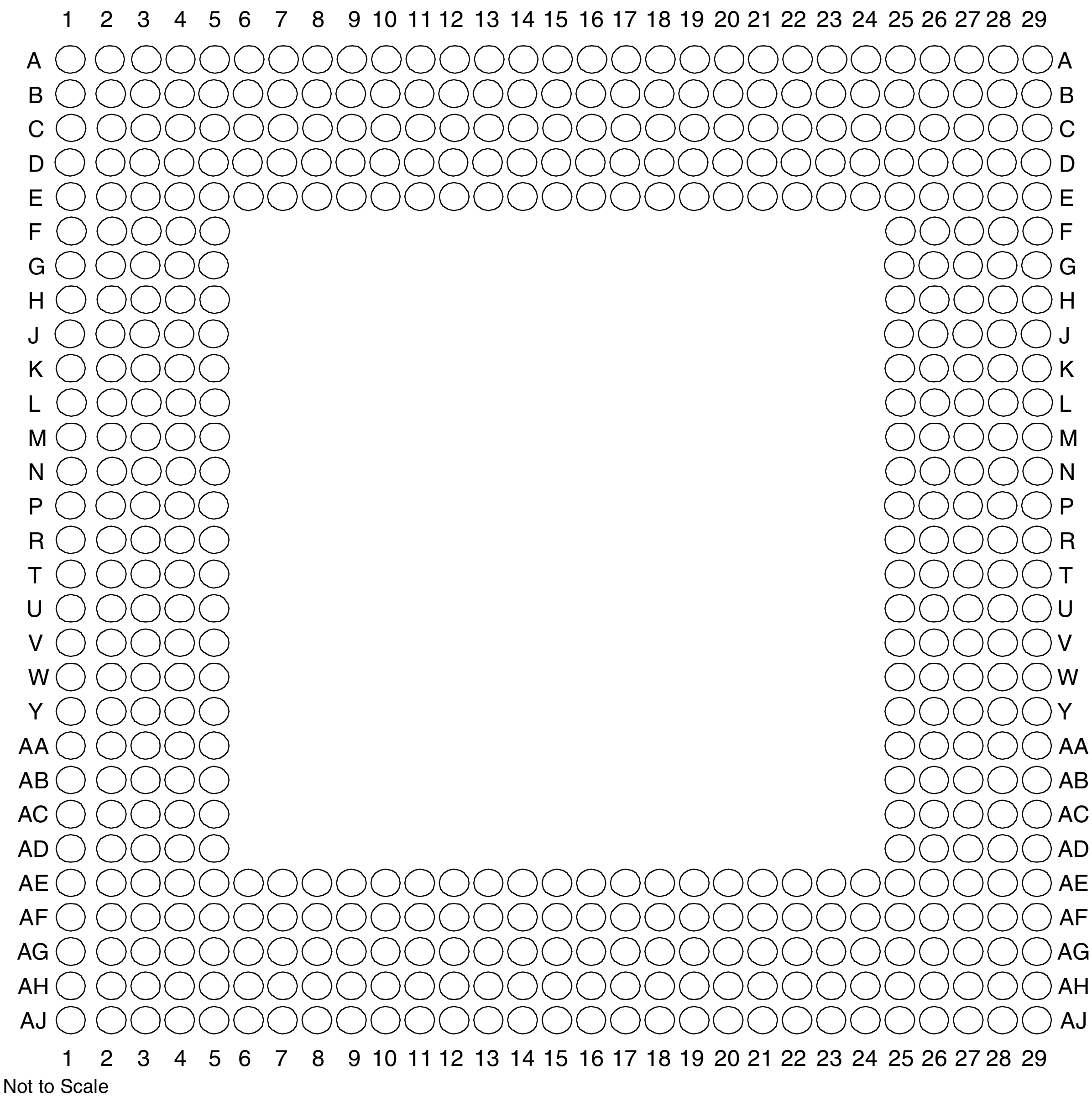


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Table 21. Pinout List (continued)

Pin Name	Ball
IRQ3/DP3/CKSTP_OUT/EXT_BR3	D21
IRQ4/DP4/CORE_SRESET/EXT_BG3	C21
IRQ5/DP5/TBEN/EXT_DBG3	B21
IRQ6/DP6/CSE0	A21
IRQ7/DP7/CSE1	E20
PSDVAL	V3
TA	C22
TEA	V5
GBL/IRQ1	W1
CI/BADDR29/IRQ2	U2
WT/BADDR30/IRQ3	U3
L2_HIT/IRQ4	Y4
CPU_BG/BADDR31/IRQ5	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
CS10/BCTL1	F29
CS11/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24

Table 21. Pinout List (continued)

Pin Name	Ball
LCL_D31/AD31[1]	AA28
LCL_DP0/C0[1]/BE0[1]	L28
LCL_DP1/C1[1]/BE1[1]	N28
LCL_DP2/C2[1]/BE2[1]	T28
LCL_DP3/C3[1]/BE3[1]	W28
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/RESTART1/DREQ3/FCC2_UTM_TXADDR2	AC29[2]
PA1/REJECT1/FCC2_UTM_TXADDR1/DONE3	AC25[2]
PA2/CLK20/FCC2_UTM_TXADDR0/DACK3	AE28[2]
PA3/CLK19/FCC2_UTM_RXADDR0/DACK4/L1RXD1A2	AG29[2]
PA4/REJECT2/FCC2_UTM_RXADDR1/DONE4	AG28[2]
PA5/RESTART2/DREQ4/FCC2_UTM_RXADDR2	AG26[2]
PA6/L1RSYNCA1	AE24[2]
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2/L1TXD0A1	AH23[2]
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22[2]
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22[2]

[3] On PCI devices (MPC8265 and MPC8266) this pin should be used as CLKIN2. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled down or left floating.
[4] Must be pulled down or left floating.
[5] On PCI devices (MPC8265 and MPC8266) this pin should be asserted if the PCI function is desired or pulled up or left floating if PCI is not desired. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled up or left floating.
[6] For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com.

5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC826xA.

5.1 Package Parameters

Package parameters are provided in Table 22. The package type is a 37.5 × 37.5 mm, 480-lead TBGA.

Table 22. Package Parameters

Parameter	Value
Package Outline	37.5 × 37.5 mm
Interconnects	480 (29 × 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC826xA. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

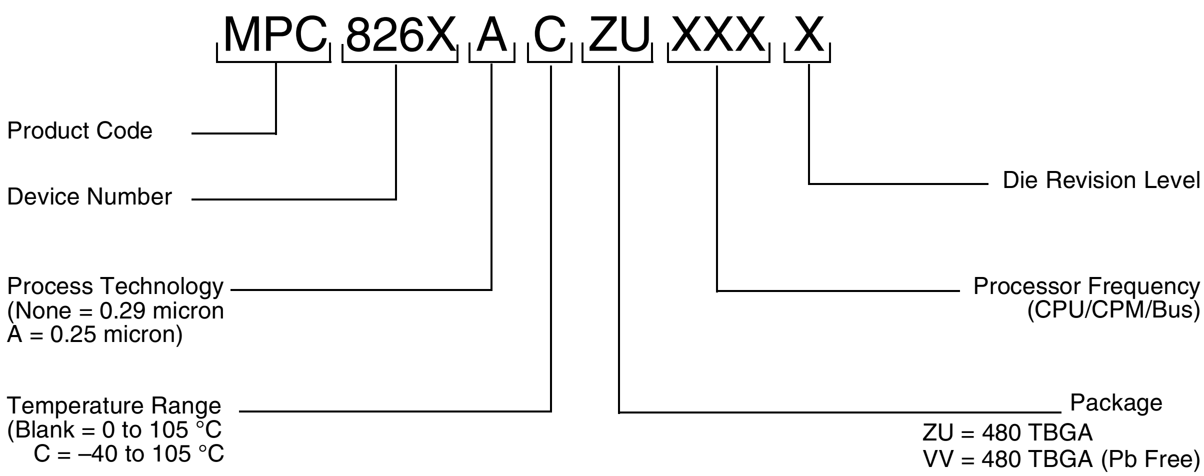


Figure 16. Freescale Part Number Key

7 Document Revision History

Table 23 lists significant changes in each revision of this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
2	06/2009	• Updated package values in Figure 16.
1.1	02/2006	• Addition of Table 12.
1.0	9/2005	• Document template update