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Understanding Embedded - Microprocessors

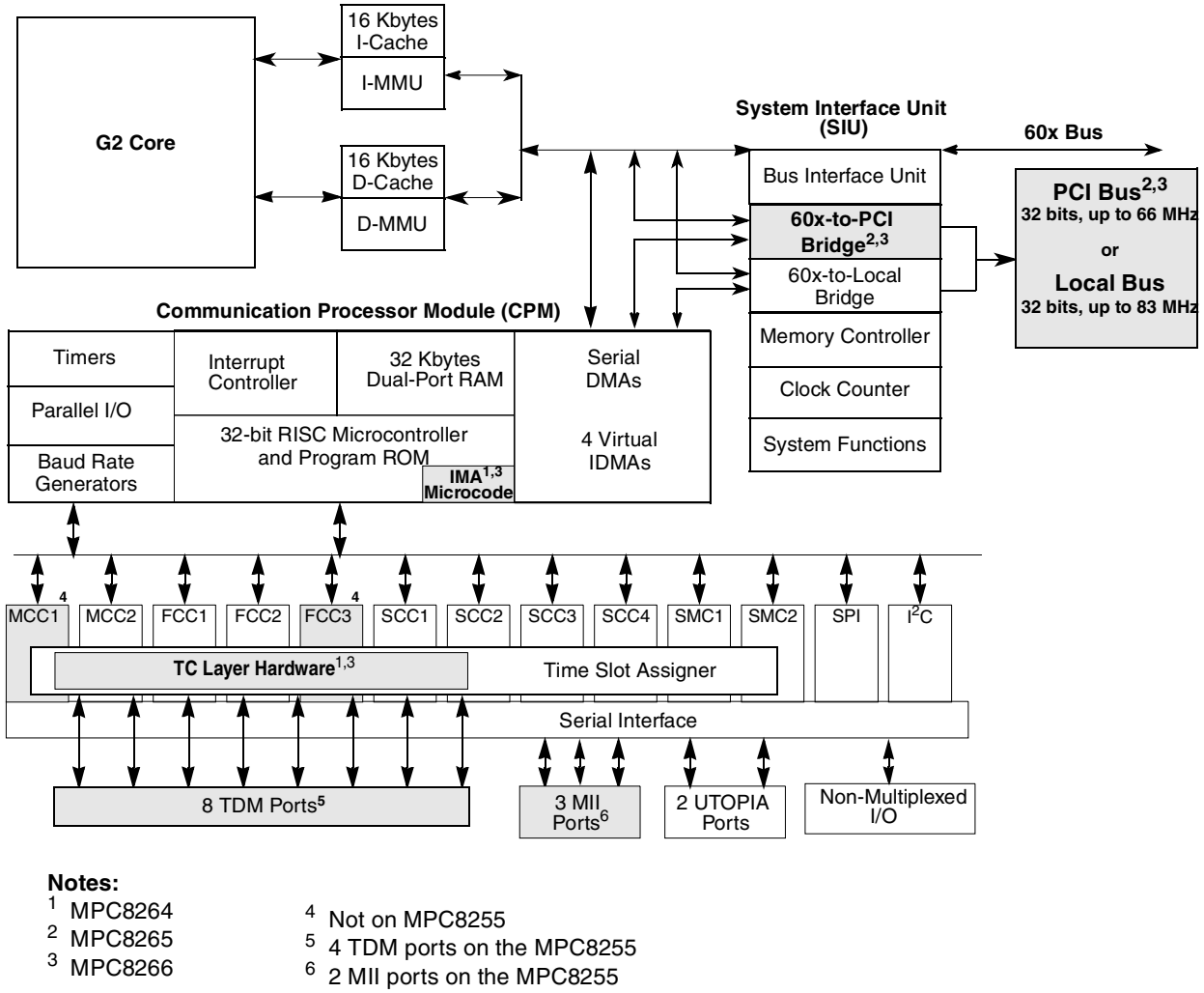
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8260avvpjdb

Figure 1 shows the block diagram for the MPC8266, the HiP4 superset device. Shaded portions indicate functionality that is not available on all devices; refer to the notes.



Notes:
1 MPC8264
2 MPC8265
3 MPC8266
4 Not on MPC8255
5 4 TDM ports on the MPC8255
6 2 MII ports on the MPC8255

Figure 1. MPC8266 Block Diagram

1 Features

The major features of the MPC826xA family are as follows:

- Dual-issue integer core
  - A core version of the EC603e microprocessor
  - System core microprocessor supporting frequencies of 150–300 MHz
  - Separate 16-Kbyte data and instruction caches:
    - Four-way set associative
    - Physically addressed
    - LRU replacement algorithm

  - PowerPC architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPs/MHz without inlining and 1.90 Dhrystones MIPS/MHz with
  - Supports bus snooping for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge (MPC8265 and MPC8266 only)
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE Std. 1149.1™ standard JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation

  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8255)
  - Supports two groups of four TDM channels for a total of eight TDMs
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

Additional features of the MPC826xA family are as follows:

- CPM
  - 32-Kbyte dual-port RAM
  - Additional MCC host commands
  - Eight transfer transmission convergence (TC) layers between the TDMs and FCC2 to support inverse multiplexing for ATM capabilities (IMA) (MPC8264 and MPC8266 only)
- CPM multiplexing
  - FCC2 can also be connected to the TC layer.
- TC layer (MPC8264 and MPC8266 only)
  - Each of the 8 TDM channels is routed in hardware to a TC layer block
    - Protocol-specific overhead bits may be discarded or routed to other controllers by the SI
    - Performing ATM TC layer functions (according to ITU-T I.432)
    - Transmit (Tx) updates
      - Cell HEC generation
      - Payload scrambling using self synchronizing scrambler (programmable by the user)
      - Coset generation (programmable by the user)
      - Cell rate by inserting idle/unassigned cells
    - Receive (Rx) updates
      - Cell delineation using bit by bit HEC checking and programmable ALPHA and DELTA parameters for the delineation state machine
      - Payload descrambling using self synchronizing scrambler (programmable by the user)

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC826xA have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3 W (when the ambient temperature is 70 °C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W)[2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

1 Test temperature = room temperature (25° C)

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

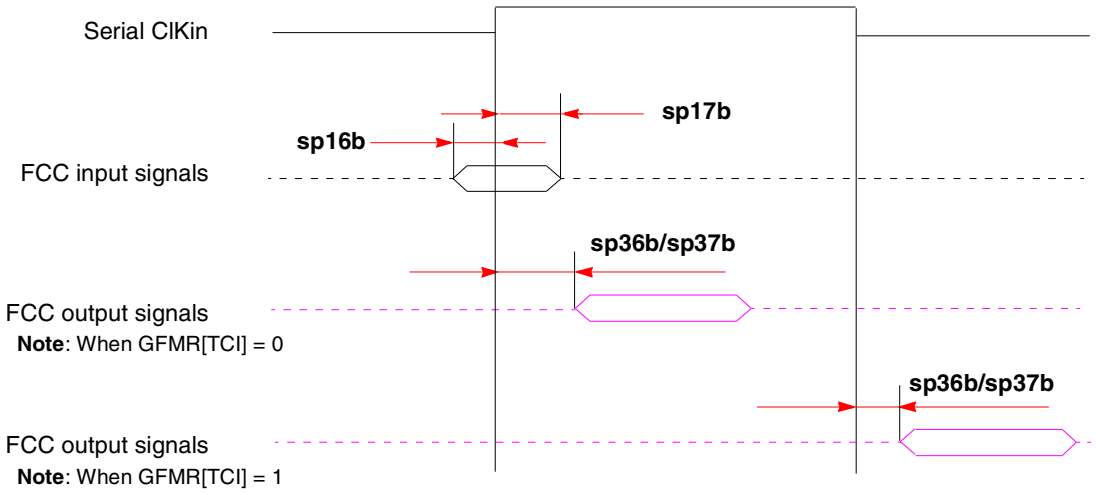
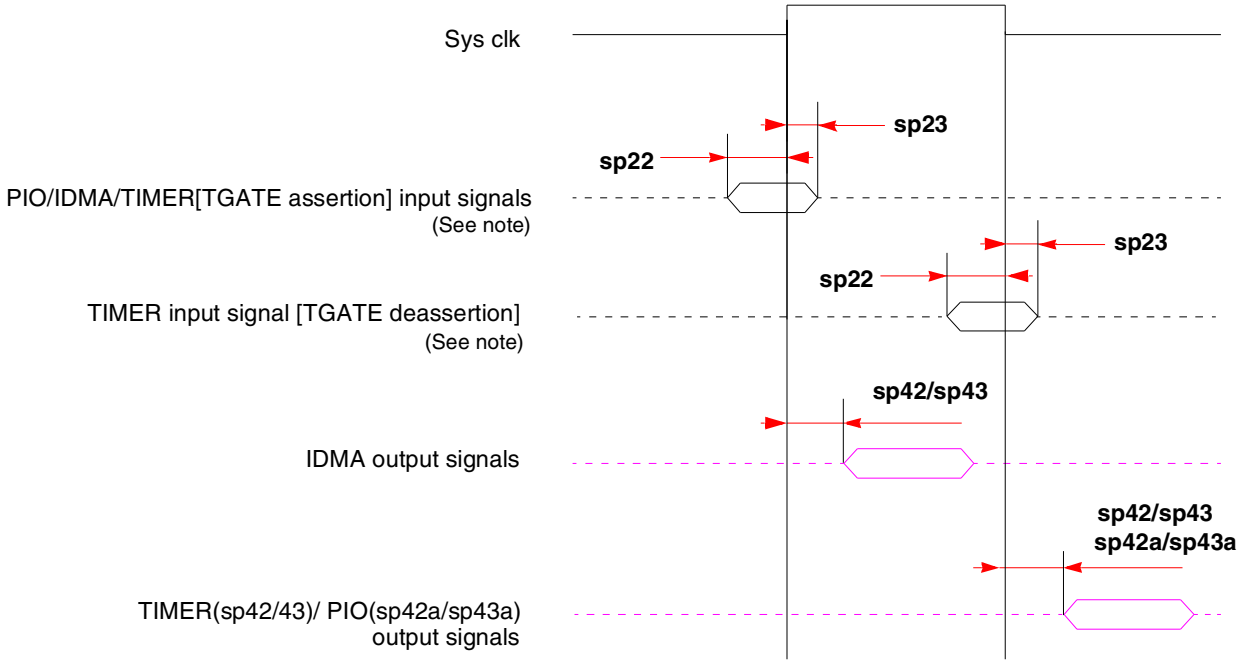


Figure 3. FCC External Clock Diagram

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 10 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	$\overline{\text{AACK}}/\overline{\text{ARTRY}}/\overline{\text{TA}}/\overline{\text{TS}}/\overline{\text{TEA}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}$	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2**/4	**66**/33 **MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	3/6	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000[5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

1 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.

2 Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user’s part.

3 Core frequency = (60x bus frequency)(core multiplication factor)

4 Bus frequency = CPM frequency/bus division factor

5 In this mode, PCI_MODCK must be “1”.

4 Pinout

This section provides the pin assignments and pinout list for the MPC826xA.

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC826xA's 480 TBGA package as viewed from the top surface.

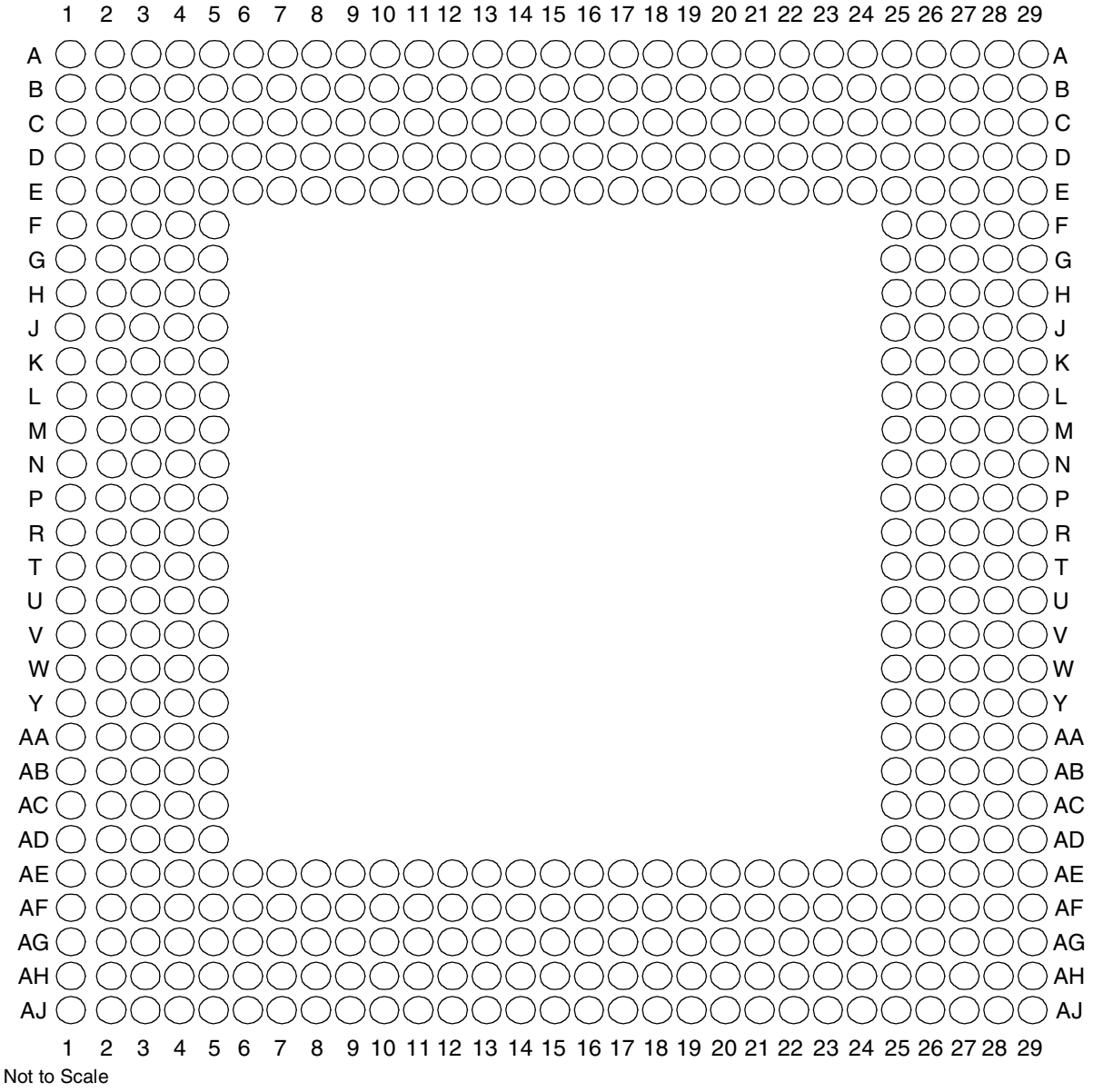


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

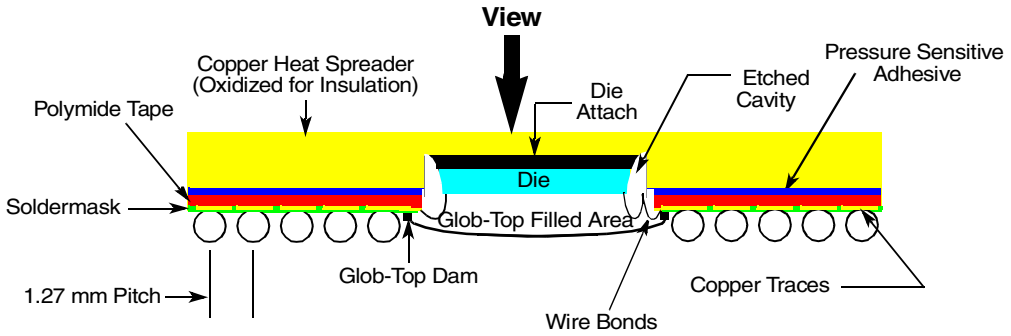


Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

Table 21. Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2

Table 21. Pinout List (continued)

Pin Name	Ball
A8	J1
A9	K4
A10	K3
A11	K2
A12	K1
A13	L5
A14	L4
A15	L3
A16	L2
A17	L1
A18	M5
A19	N5
A20	N4
A21	N3
A22	N2
A23	N1
A24	P4
A25	P3
A26	P2
A27	P1
A28	R1
A29	R3
A30	R5
A31	R4
TT0	F1
TT1	G4
TT2	G3
TT3	G2
TT4	F2
TBST	D3
TSIZ0	C1
TSIZ1	E4
TSIZ2	D2
TSIZ3	F5
AACK	F3

Table 21. Pinout List (continued)

Pin Name	Ball
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6

Table 21. Pinout List (continued)

Pin Name	Ball
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	B22
$\overline{\text{IRQ1}}$/DP1/$\overline{\text{EXT\_BG2}}$	A22
$\overline{\text{IRQ2}}$/DP2/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	E21

Table 21. Pinout List (continued)

Pin Name	Ball
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21[2]
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20[2]
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19[2]
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18[2]
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17[2]
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16[2]
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16[2]
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15[2]
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13[2]
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13[2]
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12[2]
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11[2]
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9[2]
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8[2]
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7[2]
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7[2]
PA28/$\overline{\text{FCC1\_UTM\_RXENB}}$/$\overline{\text{FCC1\_UTS\_RXENB}}$/FCC1_MII_TX_EN	AD5[2]
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1[2]
PA30/$\overline{\text{FCC1\_UTM\_TXCLAV}}$/FCC1_UTS_TXCLAV/FCC1_MII_CRS/ $\overline{\text{FCC1\_RTS}}$	AD3[2]
PA31/$\overline{\text{FCC1\_UTM\_TXENB}}$/$\overline{\text{FCC1\_UTS\_TXENB}}$/FCC1_MII_COL	AB5[2]
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/$\overline{\text{FCC3\_RTS}}$	AD28[2]
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26[2]
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25[2]
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26[2]
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27[2]
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24[2]
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24[2]
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24[2]
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22[2]
PB13/FCC3_MII_COL/$\overline{\text{L1RQB1}}$/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21[2]
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20[2]
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19[2]
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18[2]
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17[2]

Table 21. Pinout List (continued)

Pin Name	Ball
PC16/CLK16/TIN4	AF15[2]
PC17/CLK15/TIN3/BRGO8	AJ15[2]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[2]
PC19/CLK13/BRGO7/SPICLK	AG13[2]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[2]
PC21/CLK11/BRGO6	AJ11[2]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[2]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[2]
PC24/FCC2_UT8_TXD3/CLK8/$\overline{\text{TOUT4}}$	AF9[2]
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8[2]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[2]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[2]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[2]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[2]
PC30/FCC2_UT8_TXD3/CLK2/$\overline{\text{TOUT1}}$	AE1[2]
PC31/CLK1/BRGO1	AD1[2]
PD4/BRGO8/L1TSYNCD1/L1GNTD1/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[2]
PD5/FCC1_UT16_TXD3/$\overline{\text{DONE1}}$	AD27[2]
PD6/FCC1_UT16_TXD4/$\overline{\text{DACK1}}$	AF29[2]
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4/FCC1_TXCLAV2	AF28[2]
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25[2]
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26[2]
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27[2]
PD11/$\overline{\text{L1RQB2}}$/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23[2]
PD12/SI1_L1ST2/L1RXDB1	AG23[2]
PD13/SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20[2]
PD15/FCC1_UT16_RXD1/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[2]
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18[2]
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17[2]
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/FCC2_UTM_RXADDR3/SPICLK	AF16[2]
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/FCC2_UTM_TXADDR3/SPISEL/BRGO1	AH15[2]
PD20/$\overline{\text{RTS4}}$/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14[2]

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC826xA. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

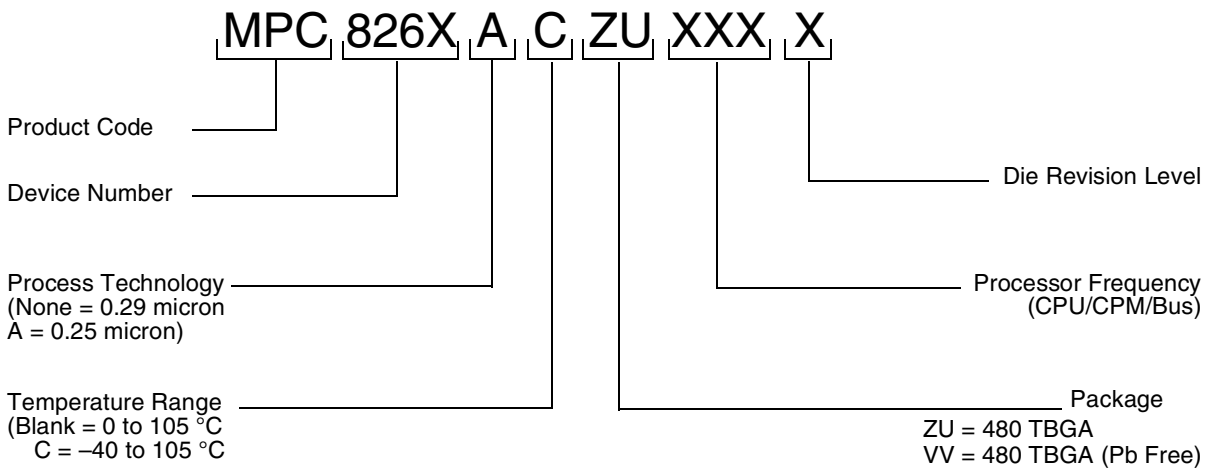


Figure 16. Freescale Part Number Key

7 Document Revision History

Table 23 lists significant changes in each revision of this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
2	06/2009	• Updated package values in Figure 16.
1.1	02/2006	• Addition of Table 12.
1.0	9/2005	• Document template update

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
0.9	8/2003	• Note: In revision 0.3, sp30 (Table 10) was changed. This change was not previously recorded in this "Document Revision History" Table. • Removal of "HiP4 PowerQUICC II Documentation" table. These supplemental specifications have been replaced by revision 1 of the *MPC8260 PowerQUICC II™ Family Reference Manual*. • Figure 1 and Section 1, "Features": Addition of MPC8255 notes • Addition of Figure 2 • Addition of VCCSYN to "Note: Core, PLL, and I/O Supply Voltages" following Table 2 • Addition of note 1 to Table 3 • Table 4: Changes to θ_{JA} and θ_{JB} and θ_{JC}. • Addition of notes or modifications to Figure 6, Figure 7, and Figure 8 • Table 9: Change of sp10. • Addition of Table 15. • Addition of note 2 to Table 21 • Table 21: Addition of FCC2 Rx and Tx [3,4] to CPM pins PD7, PD18, PD19, and PD29. Also, the addition of SPICLK to PC19. They are documented correctly in the parallel I/O ports chapter in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 21.
0.8	1/2003	• Table 2: Modification to supply voltage ranges reflected in notes 2, 3, and 4. • Table 4: Addition of θ_{JB} and θ_{JC}. • Table 7, Figure 8: Addition of sp42a/sp43a. • Figure 3, Figure 4: Addition of note for FCC output. • Figure 5, Figure 6, Figure 7: Addition of notes. • Table 14, Table 17, and Table 19: Removal of PLL bypass mode from clock tables.
0.7	5/2002	• Section 1, "Features": minimum supported core frequency of 150 MHz • Section 1, "Features": updated performance values (under "Dual-issue integer core") • Table 2: Note 2 (changes in italics): "...*less* than or equal to *233* MHz, *166* MHz CPM..." • Table 2: Addition of note 3.
0.6	3/2002	• Table 21: Modified notes to pins AE11 and AF25.
0.5	3/2002	• Table 21: Modified notes to pins AE11 and AF25. • Table 21: Addition of note to pins AA1 and AG4 (Therm0 and Therm1).
0.4	2/2002	• Note 2 for Table 2 (changes in italics): "...greater than *or equal to 266* MHz, *200* MHz CPM..." • Table 19: Core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 21: Notes added to pins at AE11, AF25, U5, and V4.
0.3	11/2001	• Table 1: note 3 • Section 2.1: Removal of "Warning" recommending use of bootstrap diodes. They are not needed. • Table 9: Change to sp12. • Table 10: Change to sp32. • Note 2 for Table 16 and Table 17 • Addition of note at beginning of Section 3.2 • Note 1 for Table 18 and Table 19 • Table 21: Additions to B27, C28, D25, D27, E26, G29, H26–28, N25, P29, AF25, AA25, AB27
0.2	11/2001	• Revision of Table 5, "Power Dissipation" • Modifications to Figure 9, Table 2,Table 10, Table 11, and Table 18 • Modification to pinout diagram, Figure 13 • Additional revisions to text and figures throughout
0.1	8/2001	• Table 8: Change to sp20/sp21.
0	—	Initial version

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