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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8260azumhbb

  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
    - 10/100-Mbit Ethernet/IEEE Std. 802.3® CDMA/CS interface through media independent interface (MII)
    - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
    - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels.Each MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8255)
  - Supports two groups of four TDM channels for a total of eight TDMs
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

Additional features of the MPC826xA family are as follows:

- CPM
  - 32-Kbyte dual-port RAM
  - Additional MCC host commands
  - Eight transfer transmission convergence (TC) layers between the TDMs and FCC2 to support inverse multiplexing for ATM capabilities (IMA) (MPC8264 and MPC8266 only)
- CPM multiplexing
  - FCC2 can also be connected to the TC layer.
- TC layer (MPC8264 and MPC8266 only)
  - Each of the 8 TDM channels is routed in hardware to a TC layer block
    - Protocol-specific overhead bits may be discarded or routed to other controllers by the SI
    - Performing ATM TC layer functions (according to ITU-T I.432)
    - Transmit (Tx) updates
      - Cell HEC generation
      - Payload scrambling using self synchronizing scrambler (programmable by the user)
      - Coset generation (programmable by the user)
      - Cell rate by inserting idle/unassigned cells
    - Receive (Rx) updates
      - Cell delineation using bit by bit HEC checking and programmable ALPHA and DELTA parameters for the delineation state machine
      - Payload descrambling using self synchronizing scrambler (programmable by the user)

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0 mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 5.3mA CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27–28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0–3]LSDDQM[0–3]/LBS[0–3]/PCI_CFG[0–3][3] LSDA10/LGPL0/PCI_MODCKH0[3] LSDWE/LGPL1/PCI_MODCKH1[3] LOE/LSDRAS/LGPL2/PCI_MODCKH2[3] LSDCAS/LGPL3/PCI_MODCKH3[3] LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK[3] LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2)	V_{OL}	—	0.4	V
I_{OL} = 3.2mA L_A14/PAR[3] L_A15/FRAME[3]/SMI L_A16/TRDY[3] L_A17/IRDY[3]/CKSTP_OUT L_A18/STOP[3] L_A19/DEVSEL[3] L_A20/IDSEL[3] L_A21/PERR[3] L_A22/SERR[3] L_A23/REQ0[3] L_A24/REQ1[3]/HSEJSW[3] L_A25/GNT0[3] L_A26/GNT1[3]/HSLED[3] L_A27/GNT2[3]/HSENUM[3] L_A28/RST[3]/CORE_SRESET L_A29/INTA[3] L_A30/REQ2[3] L_A31 LCL_D(0-31)/AD(0-31)[3] LCL_DP(0-3)/C/BE(0-3)[3] PA[0–31] PB[4–31] PC[0–31] PD[4–31] TDO				

1 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC826xA have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3 W (when the ambient temperature is 70 °C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W)[2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

1 Test temperature = room temperature (25° C)

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC826xA device. Note that AC timings are based on a 50-p*f* load. Typical output buffer impedances are shown in Table 6.

Table 6. Output Buffer Impedances[1]

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

1 These are typical values at 65° C. The impedance may vary by ±25% with process and temperature.

Table 7 lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs[1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

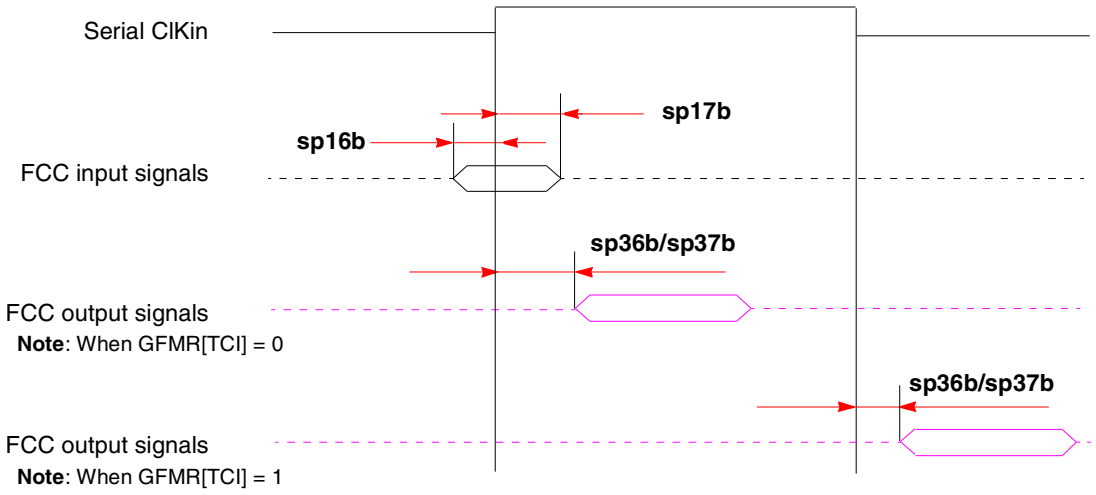


Figure 3. FCC External Clock Diagram

Figure 4 shows the FCC internal clock.

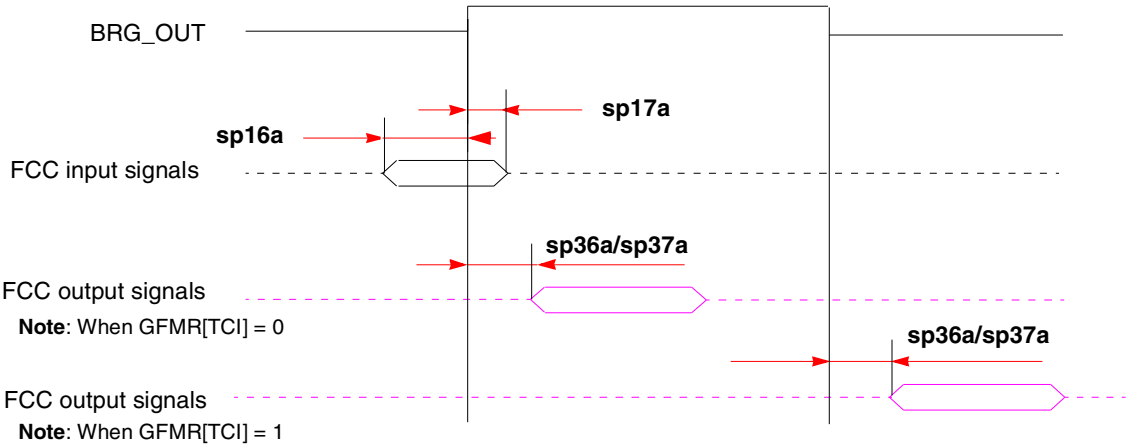
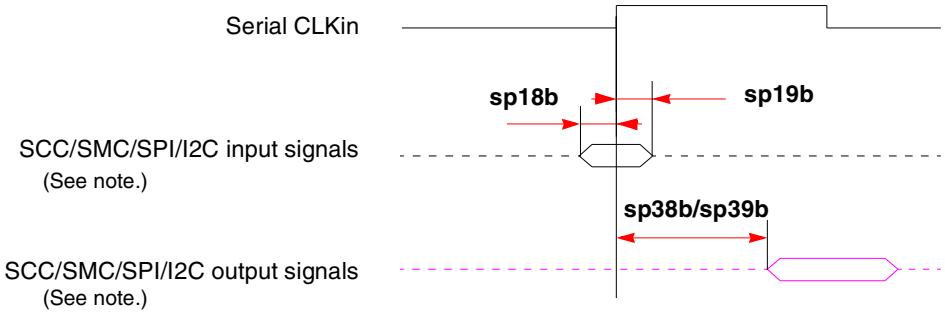


Figure 4. FCC Internal Clock Diagram

Figure 5 shows the SCC/SMC/SPI/I^2C external clock.



Note: There are four possible timing conditions for SCC and SPI:
1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I^2C External Clock Diagram

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

Figure 9 shows the interaction of several bus signals.

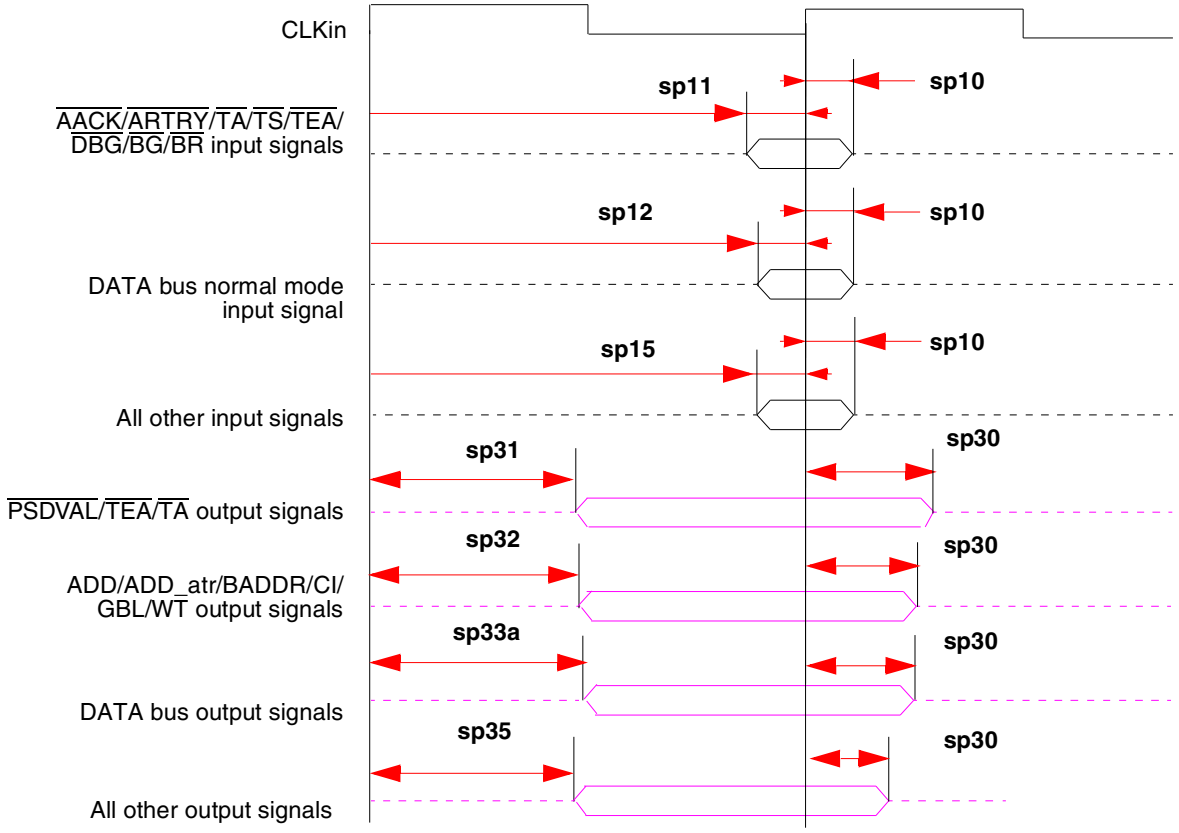


Figure 9. Bus Signals

Figure 10 shows signal behavior for all parity modes (including ECC, RMW parity, and standard parity).

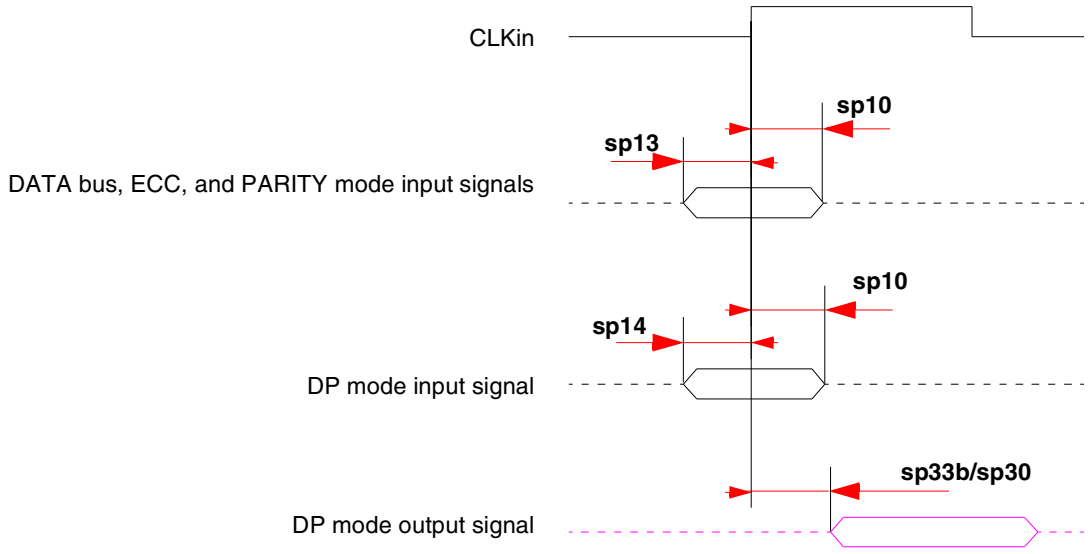


Figure 10. Parity Mode Diagram

Table 14. Clock Configuration Modes[1] (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**
0101_111	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**
0110_101	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2**/4	**66**/33 **MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	3/6	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000) (continued)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

1 Assumes MODCK_HI = 0000.
2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.
3 Core frequency = (60x bus frequency)(core multiplication factor)
4 Bus frequency = CPM frequency/bus division factor

Table 19 describes all possible clock configurations when using the MPC8265 or the MPC8266’s internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	**150 MHz**	3	180 MHz	2.5	**60 MHz**
0010_010	50/25 MHz	3/6	**150 MHz**	3.5	210 MHz	2.5	**60 MHz**
0010_011	50/25 MHz	3/6	**150 MHz**	4	240 MHz	2.5	**60 MHz**
0010_100	50/25 MHz	3/6	**150 MHz**	4.5	270 MHz	2.5	**60 MHz**
0011_000	66/33 MHz	2/4	**133 MHz**	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	**133 MHz**	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	**133 MHz**	3.5	154 MHz	3	**44 MHz**
0011_011	66/33 MHz	2/4	**133 MHz**	4	176MHz	3	**44 MHz**
0011_100	66/33 MHz	2/4	**133 MHz**	4.5	198 MHz	3	**44 MHz**
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	**3**	66 MHz
0100_001	66/33 MHz	3/6	**200 MHz**	3	200 MHz	**3**	**66 MHz**
0100_010	66/33 MHz	3/6	**200 MHz**	3.5	233 MHz	**3**	**66 MHz**
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0100_100	66/33 MHz	3/6	**200 MHz**	4.5	300 MHz	**3**	**66 MHz**
0101_000[5]	33 MHz	5	166 MHz	2.5	166 MHz	2.5	**66 MHz**
0101_001[5]	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010[5]	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011[5]	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100[5]	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Table 21. Pinout List (continued)

Pin Name	Ball
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6

Table 21. Pinout List (continued)

Pin Name	Ball
IRQ3/DP3/CKSTP_OUT/EXT_BR3	D21
IRQ4/DP4/CORE_SRESET/EXT_BG3	C21
IRQ5/DP5/TBEN/EXT_DBG3	B21
IRQ6/DP6/CSE0	A21
IRQ7/DP7/CSE1	E20
PSDVAL	V3
TA	C22
TEA	V5
GBL/IRQ1	W1
CI/BADDR29/IRQ2	U2
WT/BADDR30/IRQ3	U3
L2_HIT/IRQ4	Y4
CPU_BG/BADDR31/IRQ5	U4
CPU_DBG	R2
CPU_BR	Y3
CS0	F25
CS1	C29
CS2	E27
CS3	E28
CS4	F26
CS5	F27
CS6	F28
CS7	G25
CS8	D29
CS9	E29
CS10/BCTL1	F29
CS11/AP0	G28
BADDR27	T5
BADDR28	U1
ALE	T2
BCTL0	A27
PWE0/PSDDQM0/PBS0	C25
PWE1/PSDDQM1/PBS1	E24
PWE2/PSDDQM2/PBS2	D24
PWE3/PSDDQM3/PBS3	C24

Table 21. Pinout List (continued)

Pin Name	Ball
L_A28/$\overline{\text{RST}}$[1]/$\overline{\text{CORE\_SRESET}}$	AB29
L_A29/$\overline{\text{INTA}}$[1]	AB28
L_A30/$\overline{\text{REQ2}}$[1]	P25
L_A31/DLLOUT[1]	AB27
LCL_D0/AD0[1]	H29
LCL_D1/AD1[1]	J29
LCL_D2/AD2[1]	J28
LCL_D3/AD3[1]	J27
LCL_D4/AD4[1]	J26
LCL_D5/AD5[1]	J25
LCL_D6/AD6[1]	K25
LCL_D7/AD7[1]	L29
LCL_D8/AD8[1]	L27
LCL_D9/AD9[1]	L26
LCL_D10/AD10[1]	L25
LCL_D11/AD11[1]	M29
LCL_D12/AD12[1]	M28
LCL_D13/AD13[1]	M27
LCL_D14/AD14[1]	M26
LCL_D15/AD15[1]	N29
LCL_D16/AD16[1]	T25
LCL_D17/AD17[1]	U27
LCL_D18/AD18[1]	U26
LCL_D19/AD19[1]	U25
LCL_D20/AD20[1]	V29
LCL_D21/AD21[1]	V28
LCL_D22/AD22[1]	V27
LCL_D23/AD23[1]	V26
LCL_D24/AD24[1]	W27
LCL_D25/AD25[1]	W26
LCL_D26/AD26[1]	W25
LCL_D27/AD27[1]	Y29
LCL_D28/AD28[1]	Y28
LCL_D29/AD29[1]	Y25
LCL_D30/AD30[1]	AA29

Table 21. Pinout List (continued)

Pin Name	Ball
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13[2]
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12[2]
PD23/$\overline{\text{RTS3}}$/TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12[2]
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10[2]
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9[2]
PD26/$\overline{\text{RTS2}}$/TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8[2]
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7[2]
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4[2]
PD29/$\overline{\text{RTS1}}$/TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4	AG1[2]
PD30/$\overline{\text{FCC2\_UTM\_TXENB}}$/$\overline{\text{FCC2\_UTS\_TXENB}}$/TXD1	AD4[2]
PD31/RXD1	AD2[2]
VCCSYN	AB3
VCCSYN1	B9
GNDSYN	AB1
CLKIN2[1,3]	AE11
SPARE4[4]	U5
$\overline{\text{PCI\_MODE}}$[1,5]	AF25
SPARE6[4]	V4
THERMAL0[6]	AA1
THERMAL1[6]	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

1 MPC8265 and MPC8266 only.

2 The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC826xA. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

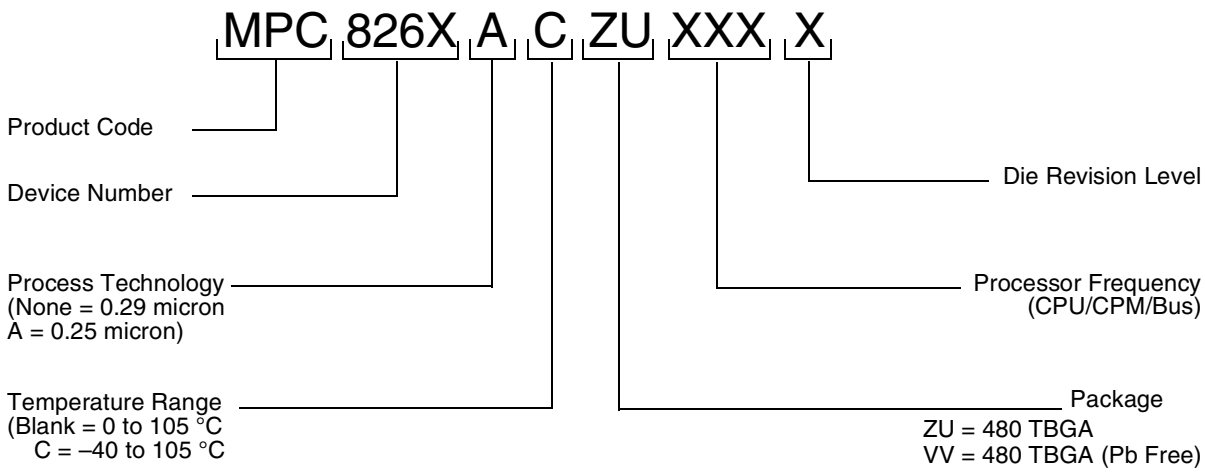


Figure 16. Freescale Part Number Key

7 Document Revision History

Table 23 lists significant changes in each revision of this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
2	06/2009	• Updated package values in Figure 16.
1.1	02/2006	• Addition of Table 12.
1.0	9/2005	• Document template update

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
0.9	8/2003	• Note: In revision 0.3, sp30 (Table 10) was changed. This change was not previously recorded in this "Document Revision History" Table. • Removal of "HiP4 PowerQUICC II Documentation" table. These supplemental specifications have been replaced by revision 1 of the *MPC8260 PowerQUICC II™ Family Reference Manual*. • Figure 1 and Section 1, "Features": Addition of MPC8255 notes • Addition of Figure 2 • Addition of VCCSYN to "Note: Core, PLL, and I/O Supply Voltages" following Table 2 • Addition of note 1 to Table 3 • Table 4: Changes to θ_{JA} and θ_{JB} and θ_{JC}. • Addition of notes or modifications to Figure 6, Figure 7, and Figure 8 • Table 9: Change of sp10. • Addition of Table 15. • Addition of note 2 to Table 21 • Table 21: Addition of FCC2 Rx and Tx [3,4] to CPM pins PD7, PD18, PD19, and PD29. Also, the addition of SPICLK to PC19. They are documented correctly in the parallel I/O ports chapter in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 21.
0.8	1/2003	• Table 2: Modification to supply voltage ranges reflected in notes 2, 3, and 4. • Table 4: Addition of θ_{JB} and θ_{JC}. • Table 7, Figure 8: Addition of sp42a/sp43a. • Figure 3, Figure 4: Addition of note for FCC output. • Figure 5, Figure 6, Figure 7: Addition of notes. • Table 14, Table 17, and Table 19: Removal of PLL bypass mode from clock tables.
0.7	5/2002	• Section 1, "Features": minimum supported core frequency of 150 MHz • Section 1, "Features": updated performance values (under "Dual-issue integer core") • Table 2: Note 2 (changes in italics): "...*less* than or equal to *233* MHz, *166* MHz CPM..." • Table 2: Addition of note 3.
0.6	3/2002	• Table 21: Modified notes to pins AE11 and AF25.
0.5	3/2002	• Table 21: Modified notes to pins AE11 and AF25. • Table 21: Addition of note to pins AA1 and AG4 (Therm0 and Therm1).
0.4	2/2002	• Note 2 for Table 2 (changes in italics): "...greater than *or equal to 266* MHz, *200* MHz CPM..." • Table 19: Core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 21: Notes added to pins at AE11, AF25, U5, and V4.
0.3	11/2001	• Table 1: note 3 • Section 2.1: Removal of "Warning" recommending use of bootstrap diodes. They are not needed. • Table 9: Change to sp12. • Table 10: Change to sp32. • Note 2 for Table 16 and Table 17 • Addition of note at beginning of Section 3.2 • Note 1 for Table 18 and Table 19 • Table 21: Additions to B27, C28, D25, D27, E26, G29, H26–28, N25, P29, AF25, AA25, AB27
0.2	11/2001	• Revision of Table 5, "Power Dissipation" • Modifications to Figure 9, Table 2,Table 10, Table 11, and Table 18 • Modification to pinout diagram, Figure 13 • Additional revisions to text and figures throughout
0.1	8/2001	• Table 8: Change to sp20/sp21.
0	—	Initial version