Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8264acvvmibb

  - PowerPC architecture-compliant memory management unit (MMU)
  - Common on-chip processor (COP) test interface
  - High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPs/MHz without inlining and 1.90 Dhrystones MIPS/MHz with
  - Supports bus snooping for data cache coherency
  - Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
  - G2 core and CPM can run at different frequencies for power/performance optimization
  - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
  - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
  - Bus supports multiple master designs
  - Supports single- and four-beat burst transfers
  - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
  - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
  - Single-master bus, supports external slaves
  - Eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge (MPC8265 and MPC8266 only)
  - Programmable host bridge and agent
  - 32-bit data bus, 66 MHz, 3.3 V
  - Synchronous and asynchronous 60x and PCI clock modes
  - All internal address space available to external PCI host
  - DMA for memory block transfers
  - PCI-to-60x address remapping
- System interface unit (SIU)
  - Clock synthesizer
  - Reset controller
  - Real-time clock (RTC) register
  - Periodic interrupt timer
  - Hardware bus monitor and software watchdog timer
  - IEEE Std. 1149.1™ standard JTAG test access port
- Twelve-bank memory controller
  - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
  - Byte write enables and selectable parity generation

  - 32-bit address decodes with programmable bank size
  - Three user programmable machines, general-purpose chip-select machine, and page-mode pipeline SDRAM machine
  - Byte selects for 64 bus width (60x) and byte selects for 32 bus width (local)
  - Dedicated interface logic for SDRAM
- CPU core can be disabled and the device can be used in slave mode to an external core
- Communications processor module (CPM)
  - Embedded 32-bit communications processor (CP) uses a RISC architecture for flexible support for communications protocols
  - Interfaces to G2 core through on-chip 32-Kbyte dual-port RAM and DMA controller
  - Serial DMA channels for receive and transmit on all serial channels
  - Parallel I/O registers with open-drain and interrupt capability
  - Virtual DMA functionality executing memory-to-memory and memory-to-I/O transfers
  - Three fast communications controllers supporting the following protocols (only FCC1 and FCC2 on the MPC8255):
    - 10/100-Mbit Ethernet/IEEE Std. 802.3® CDMA/CS interface through media independent interface (MII)
    - ATM—Full-duplex SAR protocols at 155 Mbps, through UTOPIA interface, AAL5, AAL1, AAL0 protocols, TM 4.0 CBR, VBR, UBR, ABR traffic types, up to 16 K external connections
    - Transparent
    - HDLC—Up to T3 rates (clear channel)
  - Two multichannel controllers (MCCs) (only MCC2 on the MPC8255)
    - Each MCC handles 128 serial, full-duplex, 64-Kbps data channels.Each MCC can be split into four subgroups of 32 channels each.
    - Almost any combination of subgroups can be multiplexed to single or multiple TDM interfaces up to four TDM interfaces per MCC
  - Four serial communications controllers (SCCs) identical to those on the MPC860, supporting the digital portions of the following protocols:
    - Ethernet/IEEE 802.3 CDMA/CS
    - HDLC/SDLC and HDLC bus
    - Universal asynchronous receiver transmitter (UART)
    - Synchronous UART
    - Binary synchronous (BISYNC) communications
    - Transparent
  - Two serial management controllers (SMCs), identical to those of the MPC860
    - Provide management for BRI devices as general circuit interface (GCI) controllers in time-division-multiplexed (TDM) channels

  - Transparent
  - UART (low-speed operation)
- One serial peripheral interface identical to the MPC860 SPI
- One inter-integrated circuit (I^2C) controller (identical to the MPC860 I^2C controller)
  - Microwire compatible
  - Multiple-master, single-master, and slave modes
- Up to eight TDM interfaces (four on the MPC8255)
  - Supports two groups of four TDM channels for a total of eight TDMs
  - 2,048 bytes of SI RAM
  - Bit or byte resolution
  - Independent transmit and receive routing, frame synchronization
  - Supports T1, CEPT, T1/E1, T3/E3, pulse code modulation highway, ISDN basic rate, ISDN primary rate, Freescale interchip digital link (IDL), general circuit interface (GCI), and user-defined TDM serial interfaces
- Eight independent baud rate generators and 20 input clock pins for supplying clocks to FCCs, SCCs, SMCs, and serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

Additional features of the MPC826xA family are as follows:

- CPM
  - 32-Kbyte dual-port RAM
  - Additional MCC host commands
  - Eight transfer transmission convergence (TC) layers between the TDMs and FCC2 to support inverse multiplexing for ATM capabilities (IMA) (MPC8264 and MPC8266 only)
- CPM multiplexing
  - FCC2 can also be connected to the TC layer.
- TC layer (MPC8264 and MPC8266 only)
  - Each of the 8 TDM channels is routed in hardware to a TC layer block
    - Protocol-specific overhead bits may be discarded or routed to other controllers by the SI
    - Performing ATM TC layer functions (according to ITU-T I.432)
    - Transmit (Tx) updates
      - Cell HEC generation
      - Payload scrambling using self synchronizing scrambler (programmable by the user)
      - Coset generation (programmable by the user)
      - Cell rate by inserting idle/unassigned cells
    - Receive (Rx) updates
      - Cell delineation using bit by bit HEC checking and programmable ALPHA and DELTA parameters for the delineation state machine
      - Payload descrambling using self synchronizing scrambler (programmable by the user)

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions[1]

Rating	Symbol	Value			Unit
Core supply voltage	VDD	1.7 – 1.9[2]	1.7–2.1[3]	1.9 –2.2[4]	V
PLL supply voltage	VCCSYN	1.7 – 1.9[2]	1.7–2.1[3]	1.9–2.2[4]	V
I/O supply voltage	VDDH	3.135 – 3.465			V
Input voltage	VIN	GND (–0.3) – 3.465			V
Junction temperature (maximum)	T_j	105[5]			°C
Ambient temperature	T_A	0–70[5]			°C

1 **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.
2 CPU frequency less than or equal to 200 MHz.
3 CPU frequency greater than 200 MHz but less than 233 MHz.
4 CPU frequency greater than or equal to 233 MHz.
5 Note that for extended temperature parts the range is $(-40)_{T_A} – 105_{T_j}$.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (–5% and –0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

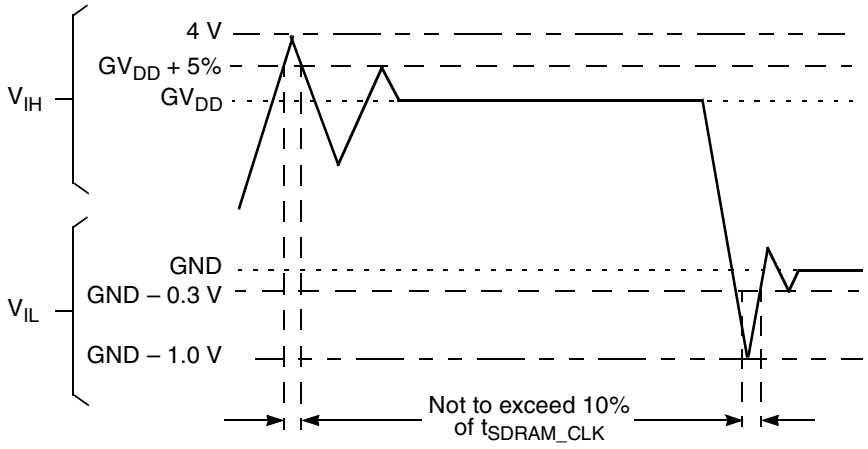


Figure 2. Overshoot/Undershoot Voltage

Table 3. DC Electrical Characteristics[1] (continued)

Characteristic	Symbol	Min	Max	Unit
I_{OL} = 7.0 mA BR BG ABB/IRQ2 TS A[0-31] TT[0-4] TBST TSIZE[0–3] AACK ARTRY DBG DBB/IRQ3 D[0-63] DP(0)/RSRV/EXT_BR2 DP(1)/IRQ1/EXT_BG2 DP(2)/TLBISYNC/IRQ2/EXT_DBG2 DP(3)/IRQ3/EXT_BR3/CKSTP_OUT DP(4)/IRQ4/EXT_BG3/CORE_SREST DP(5)/TBEN/IRQ5/EXT_DBG3 DP(6)/CSE(0)/IRQ6 DP(7)/CSE(1)/IRQ7 PSDVAL TA TEA GBL/IRQ1 CI/BADDR29/IRQ2 WT/BADDR30/IRQ3 L2_HIT/IRQ4 CPU_BG/BADDR31/IRQ5 CPU_DBG CPU_BR IRQ0/NMI_OUT IRQ7/INT_OUT/APE PORESET HRESET SRESET RSTCONF QREQ	V_{OL}	—	0.4	V

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC826xA have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above P_D = 3 W (when the ambient temperature is 70 °C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations[1]

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	P_{INT}(W)[2]			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

1 Test temperature = room temperature (25° C)

2 $P_{INT} = I_{DD} \times V_{DD}$ Watts

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

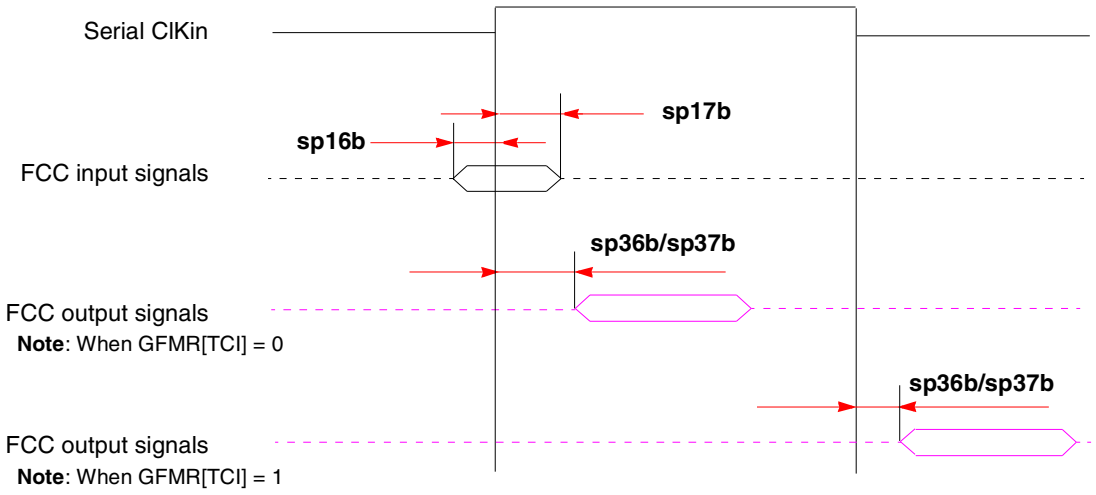
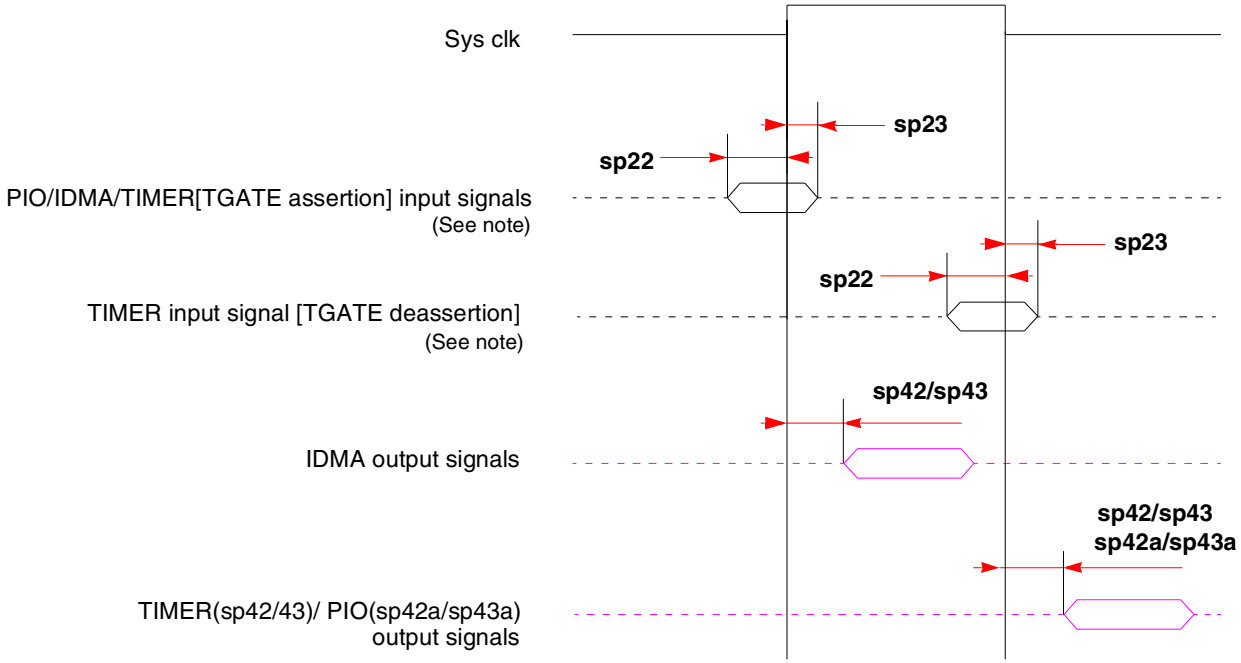


Figure 3. FCC External Clock Diagram

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 10 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs[1]

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	$\overline{\text{AACK}}/\overline{\text{ARTRY}}/\overline{\text{TA}}/\overline{\text{TS}}/\overline{\text{TEA}}/\overline{\text{DBG}}/\overline{\text{BG}}/\overline{\text{BR}}$	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

1 Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs[1]

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

1 Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BR*x*[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 13 lists the eight basic configuration modes. Table 14 lists the other modes that are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four bits from hardware configuration word on the data bus.

Note that the MPC8265 and the MPC8266 have two additional clocking modes—PCI agent and PCI host. Refer to Section 3.2, “PCI Mode” on page 26 for information.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 13 describes default clock modes for the MPC826xA.

Table 13. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note that basic modes are shown in boldface type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

Table 14. Clock Configuration Modes[1]

MODCK_H–MODCK[1–3]	Input Clock Frequency[2,3]	CPM Multiplication Factor[2]	CPM Frequency[2]	Core Multiplication Factor[2]	Core Frequency[2]
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency[1] (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor[2]	PCI Frequency[2]
0011_011[3]	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000[3]	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001[3]	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010[3]	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011[3]	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	**66 MHz**	**2**	**133 MHz**	**2.5**	**166 MHz**	**2/4**	**66/33 MHz**
0101_001	**66 MHz**	**2**	**133 MHz**	**3**	**200 MHz**	**2**/4	**66**/33 **MHz**
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	**66 MHz**	**2.5**	**166 MHz**	**2.5**	**166 MHz**	3/6	**55/28 MHz**
0110_001	**66 MHz**	**2.5**	**166 MHz**	**3**	**200 MHz**	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000) (continued)

MODCK[1–3][1]	Input Clock Frequency (PCI)[2]	CPM Multiplication Factor[2]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

1 Assumes MODCK_HI = 0000.
2 The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic ‘1’), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to Table 15.
3 Core frequency = (60x bus frequency)(core multiplication factor)
4 Bus frequency = CPM frequency/bus division factor

Table 19 describes all possible clock configurations when using the MPC8265 or the MPC8266’s internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI)[1,2]	CPM Multiplication Factor[1]	CPM Frequency	Core Multiplication Factor	Core Frequency[3]	Bus Division Factor	60x Bus Frequency[4]
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	**150 MHz**	3	180 MHz	2.5	**60 MHz**
0010_010	50/25 MHz	3/6	**150 MHz**	3.5	210 MHz	2.5	**60 MHz**
0010_011	50/25 MHz	3/6	**150 MHz**	4	240 MHz	2.5	**60 MHz**
0010_100	50/25 MHz	3/6	**150 MHz**	4.5	270 MHz	2.5	**60 MHz**
0011_000	66/33 MHz	2/4	**133 MHz**	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	**133 MHz**	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	**133 MHz**	3.5	154 MHz	3	**44 MHz**
0011_011	66/33 MHz	2/4	**133 MHz**	4	176MHz	3	**44 MHz**
0011_100	66/33 MHz	2/4	**133 MHz**	4.5	198 MHz	3	**44 MHz**
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	**3**	66 MHz
0100_001	66/33 MHz	3/6	**200 MHz**	3	200 MHz	**3**	**66 MHz**
0100_010	66/33 MHz	3/6	**200 MHz**	3.5	233 MHz	**3**	**66 MHz**
0100_011	66/33 MHz	3/6	**200 MHz**	4	266 MHz	**3**	**66 MHz**

4 Pinout

This section provides the pin assignments and pinout list for the MPC826xA.

4.1 Pin Assignments

Figure 13 shows the pinout of the MPC826xA's 480 TBGA package as viewed from the top surface.

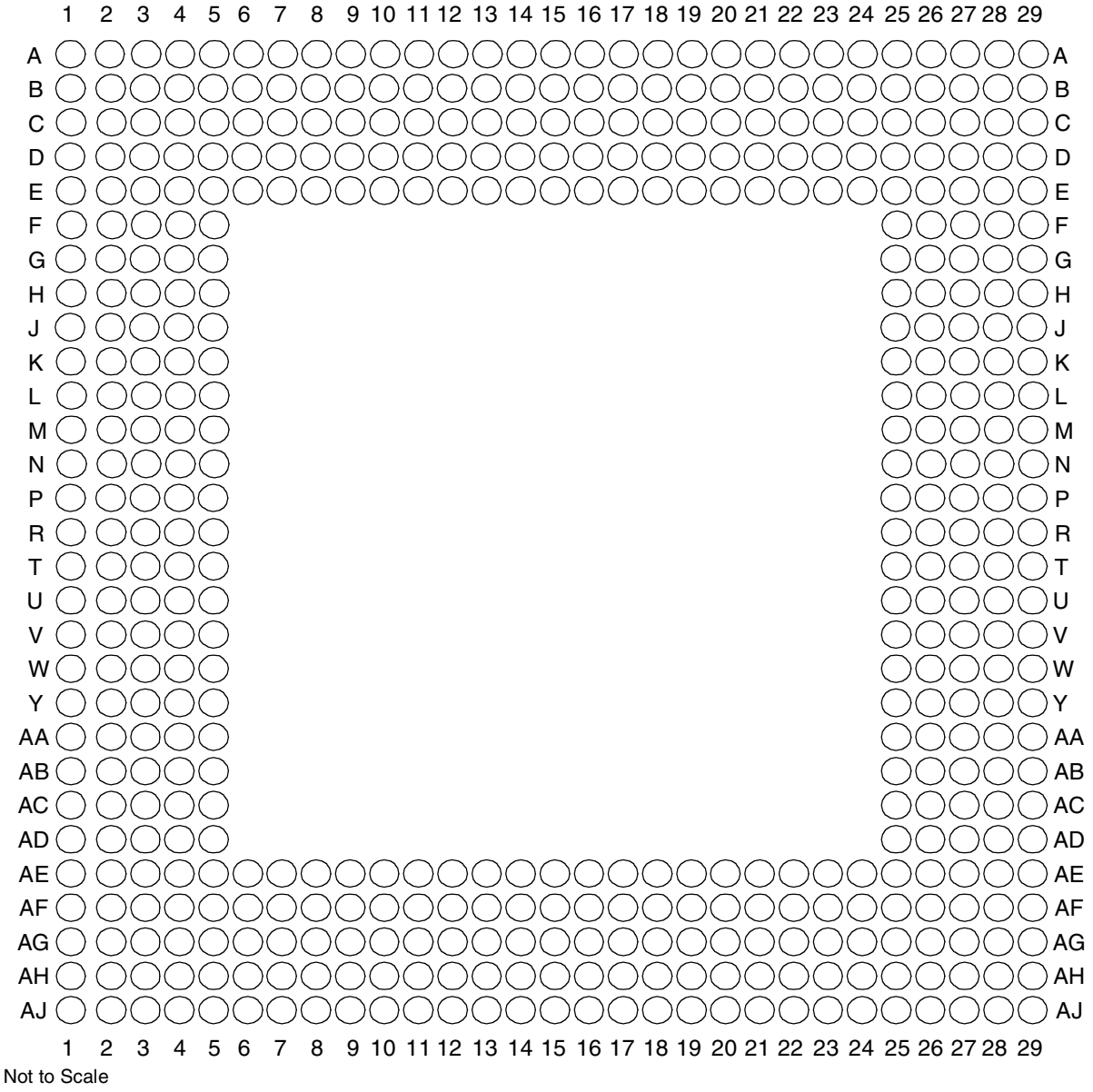


Figure 13. Pinout of the 480 TBGA Package as Viewed from the Top Surface

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

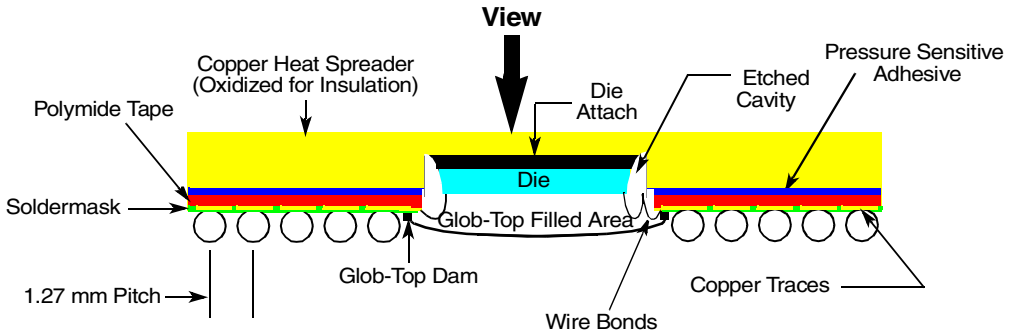


Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

Table 21. Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2

Table 21. Pinout List (continued)

Pin Name	Ball
L_A28/$\overline{\text{RST}}$[1]/$\overline{\text{CORE\_SRESET}}$	AB29
L_A29/$\overline{\text{INTA}}$[1]	AB28
L_A30/$\overline{\text{REQ2}}$[1]	P25
L_A31/DLLOUT[1]	AB27
LCL_D0/AD0[1]	H29
LCL_D1/AD1[1]	J29
LCL_D2/AD2[1]	J28
LCL_D3/AD3[1]	J27
LCL_D4/AD4[1]	J26
LCL_D5/AD5[1]	J25
LCL_D6/AD6[1]	K25
LCL_D7/AD7[1]	L29
LCL_D8/AD8[1]	L27
LCL_D9/AD9[1]	L26
LCL_D10/AD10[1]	L25
LCL_D11/AD11[1]	M29
LCL_D12/AD12[1]	M28
LCL_D13/AD13[1]	M27
LCL_D14/AD14[1]	M26
LCL_D15/AD15[1]	N29
LCL_D16/AD16[1]	T25
LCL_D17/AD17[1]	U27
LCL_D18/AD18[1]	U26
LCL_D19/AD19[1]	U25
LCL_D20/AD20[1]	V29
LCL_D21/AD21[1]	V28
LCL_D22/AD22[1]	V27
LCL_D23/AD23[1]	V26
LCL_D24/AD24[1]	W27
LCL_D25/AD25[1]	W26
LCL_D26/AD26[1]	W25
LCL_D27/AD27[1]	Y29
LCL_D28/AD28[1]	Y28
LCL_D29/AD29[1]	Y25
LCL_D30/AD30[1]	AA29

Table 21. Pinout List (continued)

Pin Name	Ball
LCL_D31/AD31[1]	AA28
LCL_DP0/C0[1]/$\overline{\text{BE0}}$[1]	L28
LCL_DP1/C1[1]/$\overline{\text{BE1}}$[1]	N28
LCL_DP2/C2[1]/$\overline{\text{BE2}}$[1]	T28
LCL_DP3/C3[1]/$\overline{\text{BE3}}$[1]	W28
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/$\overline{\text{RESTART1}}$/DREQ3/FCC2_UTM_TXADDR2	AC29[2]
PA1/$\overline{\text{REJECT1}}$/FCC2_UTM_TXADDR1/$\overline{\text{DONE3}}$	AC25[2]
PA2/CLK20/FCC2_UTM_TXADDR0/$\overline{\text{DACK3}}$	AE28[2]
PA3/CLK19/FCC2_UTM_RXADDR0/$\overline{\text{DACK4}}$/L1RXD1A2	AG29[2]
PA4/$\overline{\text{REJECT2}}$/FCC2_UTM_RXADDR1/$\overline{\text{DONE4}}$	AG28[2]
PA5/$\overline{\text{RESTART2}}$/DREQ4/FCC2_UTM_RXADDR2	AG26[2]
PA6/L1RSYNCA1	AE24[2]
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25[2]
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23[2]
PA9/SMTXD2/L1TXD0A1	AH23[2]
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22[2]
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22[2]

Table 21. Pinout List (continued)

Pin Name	Ball
PC16/CLK16/TIN4	AF15[2]
PC17/CLK15/TIN3/BRGO8	AJ15[2]
PC18/CLK14/$\overline{\text{TGATE2}}$	AH14[2]
PC19/CLK13/BRGO7/SPICLK	AG13[2]
PC20/CLK12/$\overline{\text{TGATE1}}$	AH12[2]
PC21/CLK11/BRGO6	AJ11[2]
PC22/CLK10/$\overline{\text{DONE1}}$	AG10[2]
PC23/CLK9/BRGO5/$\overline{\text{DACK1}}$	AE10[2]
PC24/FCC2_UT8_TXD3/CLK8/$\overline{\text{TOUT4}}$	AF9[2]
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8[2]
PC26/CLK6/$\overline{\text{TOUT3}}$/TMCLK	AJ6[2]
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2[2]
PC28/CLK4/TIN1/$\overline{\text{TOUT2}}$/$\overline{\text{CTS2}}$/CLSN2	AF3[2]
PC29/CLK3/TIN2/BRGO2/$\overline{\text{CTS1}}$/CLSN1	AF2[2]
PC30/FCC2_UT8_TXD3/CLK2/$\overline{\text{TOUT1}}$	AE1[2]
PC31/CLK1/BRGO1	AD1[2]
PD4/BRGO8/L1TSYNCD1/L1GNTD1/$\overline{\text{FCC3\_RTS}}$/SMRXD2	AC28[2]
PD5/FCC1_UT16_TXD3/$\overline{\text{DONE1}}$	AD27[2]
PD6/FCC1_UT16_TXD4/$\overline{\text{DACK1}}$	AF29[2]
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4/FCC1_TXCLAV2	AF28[2]
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25[2]
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26[2]
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27[2]
PD11/$\overline{\text{L1RQB2}}$/FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23[2]
PD12/SI1_L1ST2/L1RXDB1	AG23[2]
PD13/SI1_L1ST1/L1TXDB1	AJ22[2]
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20[2]
PD15/FCC1_UT16_RXD1/$\overline{\text{L1RQC2}}$/I2CSDA	AJ20[2]
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18[2]
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17[2]
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/FCC2_UTM_RXADDR3/SPICLK	AF16[2]
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/FCC2_UTM_TXADDR3/SPISEL/BRGO1	AH15[2]
PD20/$\overline{\text{RTS4}}$/TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14[2]

3 On PCI devices (MPC8265 and MPC8266) this pin should be used as CLKIN2. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled down or left floating.
4 Must be pulled down or left floating.
5 On PCI devices (MPC8265 and MPC8266) this pin should be asserted if the PCI function is desired or pulled up or left floating if PCI is not desired. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled up or left floating.
6 For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com.

5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC826xA.

5.1 Package Parameters

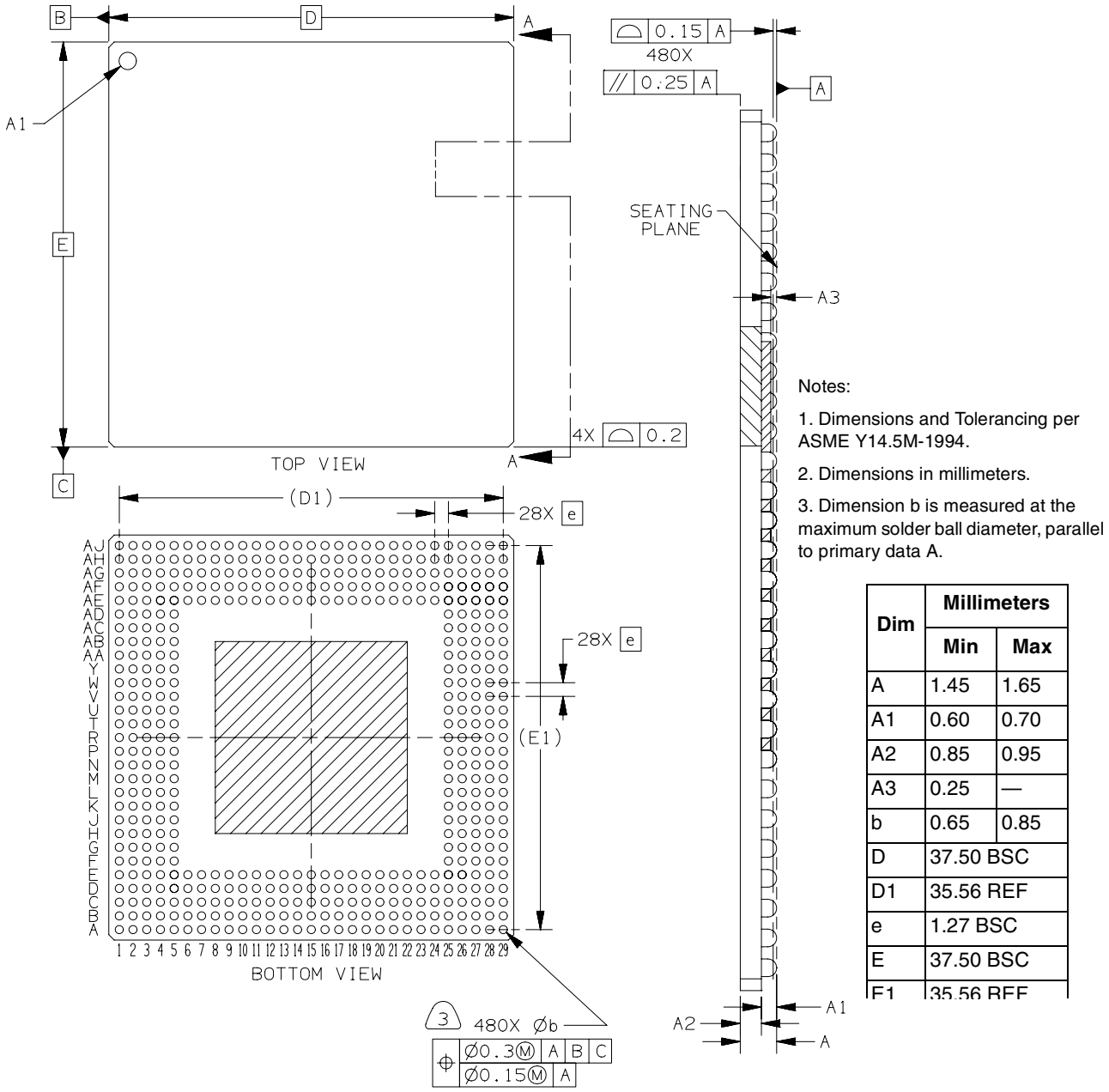
Package parameters are provided in Table 22. The package type is a 37.5 × 37.5 mm, 480-lead TBGA.

Table 22. Package Parameters

Parameter	Value
Package Outline	37.5 × 37.5 mm
Interconnects	480 (29 × 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

5.2 Mechanical Dimensions

Figure 15 provides the mechanical dimensions and bottom surface nomenclature of the 480 TBGA package.



Notes:

1. Dimensions and Tolerancing per ASME Y14.5M-1994.
2. Dimensions in millimeters.
3. Dimension b is measured at the maximum solder ball diameter, parallel to primary data A.

Dim	Millimeters	
	Min	Max
A	1.45	1.65
A1	0.60	0.70
A2	0.85	0.95
A3	0.25	—
b	0.65	0.85
D	37.50 BSC	
D1	35.56 REF	
e	1.27 BSC	
E	37.50 BSC	
E1	35.56 REF	

Figure 15. Mechanical Dimensions and Bottom Surface Nomenclature

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
0.9	8/2003	• Note: In revision 0.3, sp30 (Table 10) was changed. This change was not previously recorded in this "Document Revision History" Table. • Removal of "HiP4 PowerQUICC II Documentation" table. These supplemental specifications have been replaced by revision 1 of the *MPC8260 PowerQUICC II™ Family Reference Manual*. • Figure 1 and Section 1, "Features": Addition of MPC8255 notes • Addition of Figure 2 • Addition of VCCSYN to "Note: Core, PLL, and I/O Supply Voltages" following Table 2 • Addition of note 1 to Table 3 • Table 4: Changes to θ_{JA} and θ_{JB} and θ_{JC}. • Addition of notes or modifications to Figure 6, Figure 7, and Figure 8 • Table 9: Change of sp10. • Addition of Table 15. • Addition of note 2 to Table 21 • Table 21: Addition of FCC2 Rx and Tx [3,4] to CPM pins PD7, PD18, PD19, and PD29. Also, the addition of SPICLK to PC19. They are documented correctly in the parallel I/O ports chapter in the *MPC8260 PowerQUICC II™ Family Reference Manual* but had previously been omitted from Table 21.
0.8	1/2003	• Table 2: Modification to supply voltage ranges reflected in notes 2, 3, and 4. • Table 4: Addition of θ_{JB} and θ_{JC}. • Table 7, Figure 8: Addition of sp42a/sp43a. • Figure 3, Figure 4: Addition of note for FCC output. • Figure 5, Figure 6, Figure 7: Addition of notes. • Table 14, Table 17, and Table 19: Removal of PLL bypass mode from clock tables.
0.7	5/2002	• Section 1, "Features": minimum supported core frequency of 150 MHz • Section 1, "Features": updated performance values (under "Dual-issue integer core") • Table 2: Note 2 (changes in italics): "...*less* than or equal to *233* MHz, *166* MHz CPM..." • Table 2: Addition of note 3.
0.6	3/2002	• Table 21: Modified notes to pins AE11 and AF25.
0.5	3/2002	• Table 21: Modified notes to pins AE11 and AF25. • Table 21: Addition of note to pins AA1 and AG4 (Therm0 and Therm1).
0.4	2/2002	• Note 2 for Table 2 (changes in italics): "...greater than *or equal to 266* MHz, *200* MHz CPM..." • Table 19: Core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 • Table 21: Notes added to pins at AE11, AF25, U5, and V4.
0.3	11/2001	• Table 1: note 3 • Section 2.1: Removal of "Warning" recommending use of bootstrap diodes. They are not needed. • Table 9: Change to sp12. • Table 10: Change to sp32. • Note 2 for Table 16 and Table 17 • Addition of note at beginning of Section 3.2 • Note 1 for Table 18 and Table 19 • Table 21: Additions to B27, C28, D25, D27, E26, G29, H26–28, N25, P29, AF25, AA25, AB27
0.2	11/2001	• Revision of Table 5, "Power Dissipation" • Modifications to Figure 9, Table 2,Table 10, Table 11, and Table 18 • Modification to pinout diagram, Figure 13 • Additional revisions to text and figures throughout
0.1	8/2001	• Table 8: Change to sp20/sp21.
0	—	Initial version