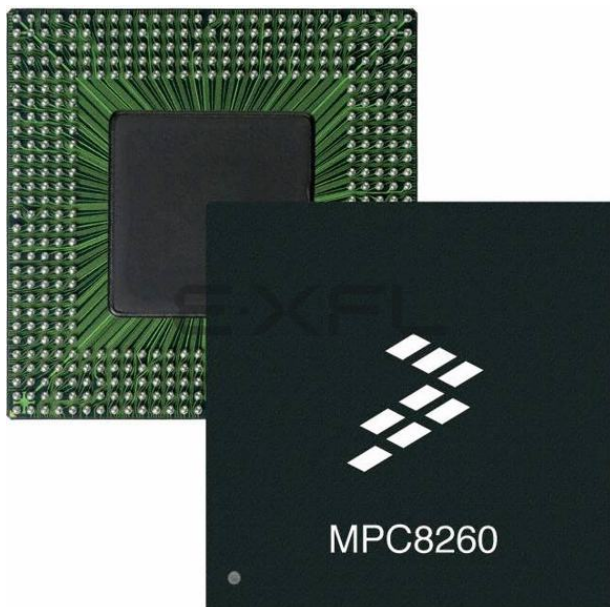




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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8264azupjdb

- PowerPC architecture-compliant memory management unit (MMU)
- Common on-chip processor (COP) test interface
- High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPS/MHz without inlining and 1.90 Dhrystones MIPS/MHz with
- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
 - G2 core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
 - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge (MPC8265 and MPC8266 only)
 - Programmable host bridge and agent
 - 32-bit data bus, 66 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE Std. 1149.1™ standard JTAG test access port
- Twelve-bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
 - Byte write enables and selectable parity generation

Table 2 lists recommended operational voltage conditions.

Table 2. Recommended Operating Conditions¹

Rating	Symbol	Value			Unit
Core supply voltage	VDD	1.7 – 1.9 ²	1.7–2.1 ³	1.9 – 2.2 ⁴	V
PLL supply voltage	VCCSYN	1.7 – 1.9 ²	1.7–2.1 ³	1.9 – 2.2 ⁴	V
I/O supply voltage	VDDH	3.135 – 3.465			V
Input voltage	VIN	GND (–0.3) – 3.465			V
Junction temperature (maximum)	T _j	105 ⁵			°C
Ambient temperature	T _A	0–70 ⁵			°C

¹ **Caution:** These are the recommended and tested operating conditions. Proper device operating outside of these conditions is not guaranteed.

² CPU frequency less than or equal to 200 MHz.

³ CPU frequency greater than 200 MHz but less than 233 MHz.

⁴ CPU frequency greater than or equal to 233 MHz.

⁵ Note that for extended temperature parts the range is (–40)_{T_A} – 105_{T_j}.

NOTE: Core, PLL, and I/O Supply Voltages

VDDH, VCCSYN, and VDD must track each other and both must vary in the same direction—in the positive direction (+5% and +0.1 Vdc) or in the negative direction (–5% and –0.1 Vdc).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (either GND or V_{CC}).

Figure 2 shows the undershoot and overshoot voltage of the 60x and local bus memory interface of the MPC8280. Note that in PCI mode the I/O interface is different.

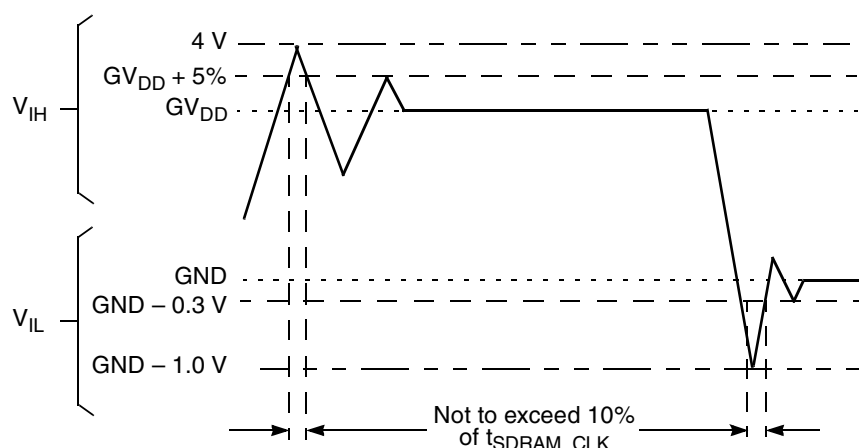


Figure 2. Overshoot/Undershoot Voltage

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 7.0 \text{ mA}$ $\overline{BR}$ $\overline{BG}$ $\overline{ABB/IRQ2}$ $\overline{TS}$ $A[0-31]$ $TT[0-4]$ $\overline{TBST}$ $TSIZE[0-3]$ $\overline{AACK}$ $\overline{ARTRY}$ $\overline{DBG}$ $\overline{DBB/IRQ3}$ $D[0-63]$ $DP(0)/\overline{RSRV/EXT_BR2}$ $DP(1)/\overline{IRQ1/EXT_BG2}$ $DP(2)/\overline{TLBISYNC/IRQ2/EXT_DBG2}$ $DP(3)/\overline{IRQ3/EXT_BR3/CKSTP_OUT}$ $DP(4)/\overline{IRQ4/EXT_BG3/CORE_SREST}$ $DP(5)/\overline{TBEN/IRQ5/EXT_DBG3}$ $DP(6)/\overline{CSE(0)/IRQ6}$ $DP(7)/\overline{CSE(1)/IRQ7}$ $\overline{PSDVAL}$ $\overline{TA}$ $\overline{TEA}$ $\overline{GBL/IRQ1}$ $\overline{CI/BADDR29/IRQ2}$ $\overline{WT/BADDR30/IRQ3}$ $\overline{L2_HIT/IRQ4}$ $\overline{CPU_BG/BADDR31/IRQ5}$ $\overline{CPU_DBG}$ $\overline{CPU_BR}$ $\overline{IRQ0/NMI_OUT}$ $\overline{IRQ7/INT_OUT/APE}$ $\overline{PORESET}$ $\overline{HRESET}$ $\overline{SRESET}$ $\overline{RSTCONF}$ $\overline{QREQ}$	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ $\overline{ALE}$ $\overline{BCTL0}$ $\overline{PWE}(0:7)/\overline{PSDDQM}(0:7)/\overline{PBS}(0:7)$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0-3]/\overline{LBS}[0-3]/\overline{PCI_CFG}[0-3]^3$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI_MODCKH0}^3$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI_MODCKH1}^3$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI_MODCKH2}^3$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI_MODCKH3}^3$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI_MODCK}^3$ $\overline{LWR}$ $\overline{MODCK1}/\overline{AP}(1)/\overline{TC}(0)/\overline{BNKSEL}(0)$ $\overline{MODCK2}/\overline{AP}(2)/\overline{TC}(1)/\overline{BNKSEL}(1)$ $\overline{MODCK3}/\overline{AP}(3)/\overline{TC}(2)/\overline{BNKSEL}(2)$ $I_{OL} = 3.2\text{mA}$ $\overline{L_A14}/\overline{PAR}^3$ $\overline{L_A15}/\overline{FRAME}^3/\overline{SMI}$ $\overline{L_A16}/\overline{TRDY}^3$ $\overline{L_A17}/\overline{IRDY}^3/\overline{CKSTP_OUT}$ $\overline{L_A18}/\overline{STOP}^3$ $\overline{L_A19}/\overline{DEVSEL}^3$ $\overline{L_A20}/\overline{IDSEL}^3$ $\overline{L_A21}/\overline{PERR}^3$ $\overline{L_A22}/\overline{SERR}^3$ $\overline{L_A23}/\overline{REQ0}^3$ $\overline{L_A24}/\overline{REQ1}^3/\overline{HSEJSW}^3$ $\overline{L_A25}/\overline{GNT0}^3$ $\overline{L_A26}/\overline{GNT1}^3/\overline{HSLED}^3$ $\overline{L_A27}/\overline{GNT2}^3/\overline{HSENUM}^3$ $\overline{L_A28}/\overline{RST}^3/\overline{CORE_SRESET}$ $\overline{L_A29}/\overline{INTA}^3$ $\overline{L_A30}/\overline{REQ2}^3$ $\overline{L_A31}$ $\overline{LCL_D}(0-31)/\overline{AD}(0-31)^3$ $\overline{LCL_DP}(0-3)/\overline{C}/\overline{BE}(0-3)^3$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ $\overline{TDO}$	V_{OL}	—	0.4	V

¹ The default configuration of the CPM pins ($\overline{PA}[0-31]$, $\overline{PB}[4-31]$, $\overline{PC}[0-31]$, $\overline{PD}[4-31]$) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

² The leakage current is measured for nominal VDD, VCCSYN, and VDD.

³ MPC8265 and MPC8266 only.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics for 480 TBGA Package

Characteristics	Symbol	Value	Unit	Air Flow
Junction to ambient	θ_{JA}	13 ¹	°C/W	NC ²
		10 ¹		1 m/s
		11 ³		NC
		8 ³		1 m/s
Junction to board ⁴	θ_{JB}	4	°C/W	—
Junction to case ⁵	θ_{JC}	1.1	°C/W	—

¹ Assumes a single layer board with no thermal vias

² Natural convection

³ Assumes a four layer board

⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 Power Considerations

The average chip-junction temperature, T_J , in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where

T_A = ambient temperature °C

θ_{JA} = package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)

$P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K / (T_J + 273^\circ \text{C}) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273^\circ \text{C}) + \theta_{JA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K , the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

2.3.1 Layout Practices

Each V_{CC} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 μ F by-pass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and ground should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the MPC826xA have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize overdamped conditions and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Table 5 provides preliminary, estimated power dissipation for various configurations. Note that suitable thermal management is required for conditions above $P_D = 3$ W (when the ambient temperature is 70 °C or greater) to ensure the junction temperature does not exceed the maximum specified value. Also note that the I/O power should be included when determining whether to use a heat sink.

Table 5. Estimated Power Dissipation for Various Configurations¹

Bus (MHz)	CPM Multiplier	Core CPU Multiplier	CPM (MHz)	CPU (MHz)	$P_{INT}(W)^2$			
					Vddl 1.8 Volts		Vddl 2.0 Volts	
					Nominal	Maximum	Nominal	Maximum
66.66	2	3	133	200	1.2	2	1.8	2.3
66.66	2.5	3	166	200	1.3	2.1	1.9	2.3
66.66	3	4	200	266	—	—	2.3	2.9
66.66	3	4.5	200	300	—	—	2.4	3.1
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2	3	166	250	—	—	2.2	2.8
83.33	2.5	3.5	208	291	—	—	2.4	3.1

¹ Test temperature = room temperature (25° C)

² $P_{INT} = I_{DD} \times V_{DD}$ Watts

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC826xA device. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in [Table 6](#).

Table 6. Output Buffer Impedances¹

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

¹ These are typical values at 65° C. The impedance may vary by $\pm 25\%$ with process and temperature.

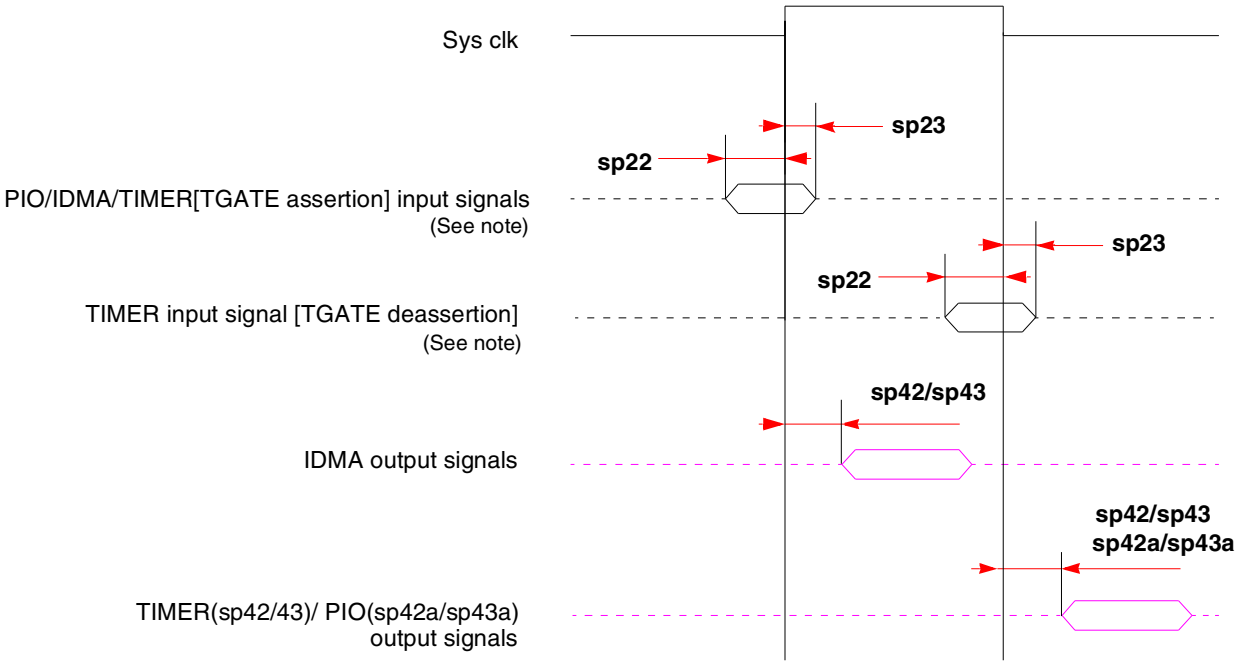
[Table 7](#) lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs¹

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Figure 8 shows PIO, timer, and DMA signals.



Note: TGATE is asserted on the rising edge of the clock; it is deasserted on the falling edge.

Figure 8. PIO, Timer, and DMA Signal Diagram

Table 10 lists SIU input characteristics.

Table 9. AC Characteristics for SIU Inputs¹

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp11	sp10	AACK/ARTRY/T $\bar{A}$ /TS/TEA/DBG/BG/BR	6	5	0.5	0.5
sp12	sp10	Data bus in normal mode	5	4	0.5	0.5
sp13	sp10	Data bus in ECC and PARITY modes	8	6	0.5	0.5
sp14	sp10	DP pins	7	6	0.5	0.5
sp15	sp10	All other pins	5	4	0.5	0.5

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Figure 11 shows signal behavior in MEMC mode.

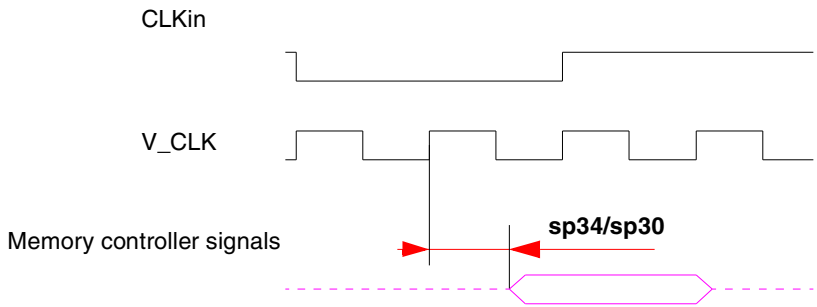


Figure 11. MEMC Mode Diagram

NOTE

Generally, all MPC826xA bus and system output signals are driven from the rising edge of the input clock (CLKIn). Memory controller signals, however, trigger on four points within a CLKIn cycle. Each cycle is divided by four internal ticks: T1, T2, T3, and T4. T1 always occurs at the rising edge, and T3 at the falling edge, of CLKIn. However, the spacing of T2 and T4 depends on the PLL clock ratio selected, as shown in Table 11.

Table 11. Tick Spacing for Memory Controller Signals

PLL Clock Ratio	Tick Spacing (T1 Occurs at the Rising Edge of CLKIn)		
	T2	T3	T4
1:2, 1:3, 1:4, 1:5, 1:6	1/4 CLKIn	1/2 CLKIn	3/4 CLKIn
1:2.5	3/10 CLKIn	1/2 CLKIn	8/10 CLKIn
1:3.5	4/14 CLKIn	1/2 CLKIn	11/14 CLKIn

Figure 12 is a graphical representation of Table 11.

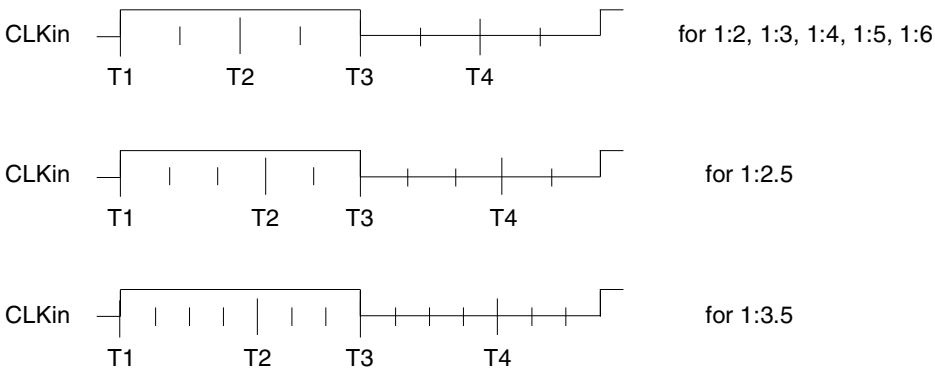


Figure 12. Internal Tick Spacing for Memory Controller Signals

Table 14. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3}	CPM Multiplication Factor ²	CPM Frequency ²	Core Multiplication Factor ²	Core Frequency ²
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	33 MHz	4	133 MHz	4	133 MHz
0010_011	33 MHz	4	133 MHz	5	166 MHz
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					

Table 14. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3}	CPM Multiplication Factor ²	CPM Frequency ²	Core Multiplication Factor ²	Core Frequency ²
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	66 MHz	2	133 MHz	2.5	166 MHz
0101_111	66 MHz	2	133 MHz	3	200 MHz
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	66 MHz	2.5	166 MHz	2.5	166 MHz
0110_101	66 MHz	2.5	166 MHz	3	200 MHz
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz

3.2.1 PCI Host Mode

The frequencies listed in [Table 16](#) and [Table 17](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 16. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3] ¹	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

¹ Assumes MODCK_HI = 0000.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to [Table 15](#).

[Table 17](#) describes all possible clock configurations when using the MPC8265's or the MPC8266's internal PCI bridge in host mode.

Table 17. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency ¹ (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	33 MHz	4	133 MHz	5	166 MHz	4/8	33/16 MHz
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000 ³	33 MHz	5	166 MHz	5	166 MHz	5	33 MHz
0011_001 ³	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz
0011_010 ³	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) ^{1,2}	CPM Multiplication Factor ¹	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
0100_100	66/33 MHz	3/6	200 MHz	4.5	300 MHz	3	66 MHz
0101_000 ⁵	33 MHz	5	166 MHz	2.5	166 MHz	2.5	66 MHz
0101_001 ⁵	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010 ⁵	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011 ⁵	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100 ⁵	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Table 21. Pinout List (continued)

Pin Name	Ball
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/ $\overline{\text{RSRV/EXT_BR2}}$	B22
IRQ1/DP1/ $\overline{\text{EXT_BG2}}$	A22
IRQ2/DP2/ $\overline{\text{TLBISYNC/EXT_DBG2}}$	E21

Table 21. Pinout List (continued)

Pin Name	Ball
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
PSDWE/PGPL1	B24
POE/PSDRAS/PGPL2	A24
PSDCAS/PGPL3	B23
PGTA/PUPMWAIT/PGPL4/PPBS	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/LBS0/PCI_CFG0 ¹	H28
LWE1/LSDDQM1/LBS1/PCI_CFG1 ¹	H27
LWE2/LSDDQM2/LBS2/PCI_CFG2 ¹	H26
LWE3/LSDDQM3/LBS3/PCI_CFG3 ¹	G29
LSDA10/LGPL0/PCI_MODCKH0 ¹	D27
LSDWE/LGPL1/PCI_MODCKH1 ¹	C28
LOE/LSDRAS/LGPL2/PCI_MODCKH2 ¹	E26
LSDCAS/LGPL3/PCI_MODCKH3 ¹	D25
LGTA/LUPMWAIT/LGPL4/LPBS	C26
LGPL5/LSDAMUX/PCI_MODCK ¹	B27
LWR	D28
L_A14/PAR ¹	N27
L_A15/FRAME ¹ /SMI	T29
L_A16/TRDY ¹	R27
L_A17/IRDY ¹ /CKSTP_OUT	R26
L_A18/STOP ¹	R29
L_A19/DEVSEL ¹	R28
L_A20/IDSEL ¹	W29
L_A21/PERR ¹	P28
L_A22/SERR ¹	N26
L_A23/REQ0 ¹	AA27
L_A24/REQ1 ¹ /HSEJSW ¹	P29
L_A25/GNT0 ¹	AA26
L_A26/GNT1 ¹ /HSLED ¹	N25
L_A27/GNT2 ¹ /HSENUM ¹	AA25

Table 21. Pinout List (continued)

Pin Name	Ball
L_A28/RST ¹ /CORE_SRESET	AB29
L_A29/INTA ¹	AB28
L_A30/REQ2 ¹	P25
L_A31/DLLOUT ¹	AB27
LCL_D0/AD0 ¹	H29
LCL_D1/AD1 ¹	J29
LCL_D2/AD2 ¹	J28
LCL_D3/AD3 ¹	J27
LCL_D4/AD4 ¹	J26
LCL_D5/AD5 ¹	J25
LCL_D6/AD6 ¹	K25
LCL_D7/AD7 ¹	L29
LCL_D8/AD8 ¹	L27
LCL_D9/AD9 ¹	L26
LCL_D10/AD10 ¹	L25
LCL_D11/AD11 ¹	M29
LCL_D12/AD12 ¹	M28
LCL_D13/AD13 ¹	M27
LCL_D14/AD14 ¹	M26
LCL_D15/AD15 ¹	N29
LCL_D16/AD16 ¹	T25
LCL_D17/AD17 ¹	U27
LCL_D18/AD18 ¹	U26
LCL_D19/AD19 ¹	U25
LCL_D20/AD20 ¹	V29
LCL_D21/AD21 ¹	V28
LCL_D22/AD22 ¹	V27
LCL_D23/AD23 ¹	V26
LCL_D24/AD24 ¹	W27
LCL_D25/AD25 ¹	W26
LCL_D26/AD26 ¹	W25
LCL_D27/AD27 ¹	Y29
LCL_D28/AD28 ¹	Y28
LCL_D29/AD29 ¹	Y25
LCL_D30/AD30 ¹	AA29

Table 21. Pinout List (continued)

Pin Name	Ball
PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14 ²
PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13 ²
PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12 ²
PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2/L1TXD2A1	AH11 ²
PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_TXD/L1RXD1A1/L1RXDD2	AH16 ²
PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1TXDD2	AE15 ²
PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2	AJ9 ²
PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9 ²
PB26/FCC2_MII_CRD/FCC2_UT8_TXD1/L1RXDC2	AJ7 ²
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6 ²
PB28/FCC2_MII_RX_ER/FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1	AE3 ²
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/FCC2_MII_TX_EN	AE2 ²
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2	AC5 ²
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4 ²
PC0/DREQ1/BRGO7/SMSYN2/L1CLKOA2	AB26 ²
PC1/DREQ2/BRGO6/L1RQA2	AD29 ²
PC2/FCC3_CD/FCC2_UT8_TXD3/DONE2	AE29 ²
PC3/FCC3_CTS/FCC2_UT8_TXD2/DACK2/CTS4	AE27 ²
PC4/FCC2_UTM_RXENB/FCC2_UTS_RXENB/SI2_L1ST4/FCC2_CD	AF27 ²
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/FCC2_CTS	AF24 ²
PC6/FCC1_CD/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR/FCC1_UTM_RXCLAV1	AJ26 ²
PC7/FCC1_CTS/L1RQC1/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/FCC1_UTM_TXCLAV1	AJ25 ²
PC8/CD4/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/CTS3	AF22 ²
PC9/CTS4/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21 ²
PC10/CD3/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AF20 ²
PC11/CTS3/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19 ²
PC12/CD2/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18 ²
PC13/CTS2/CLSN2/L1RQD1/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18 ²
PC14/CD1/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17 ²
PC15/CTS1/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16 ²

Table 21. Pinout List (continued)

Pin Name	Ball
PC16/CLK16/TIN4	AF15 ²
PC17/CLK15/TIN3/BRGO8	AJ15 ²
PC18/CLK14/ $\overline{\text{TGATE2}}$	AH14 ²
PC19/CLK13/BRGO7/SPICLK	AG13 ²
PC20/CLK12/ $\overline{\text{TGATE1}}$	AH12 ²
PC21/CLK11/BRGO6	AJ11 ²
PC22/CLK10/ $\overline{\text{DONE1}}$	AG10 ²
PC23/CLK9/BRGO5/ $\overline{\text{DACK1}}$	AE10 ²
PC24/FCC2_UT8_TXD3/CLK8/ $\overline{\text{TOUT4}}$	AF9 ²
PC25/FCC2_UT8_TXD2/CLK7/BRGO4	AE8 ²
PC26/CLK6/ $\overline{\text{TOUT3}}$ /TMCLK	AJ6 ²
PC27/FCC3_TXD/FCC3_TXD0/CLK5/BRGO3	AG2 ²
PC28/CLK4/TIN1/ $\overline{\text{TOUT2}}$ / $\overline{\text{CTS2}}$ /CLSN2	AF3 ²
PC29/CLK3/TIN2/BRGO2/ $\overline{\text{CTS1}}$ /CLSN1	AF2 ²
PC30/FCC2_UT8_TXD3/CLK2/ $\overline{\text{TOUT1}}$	AE1 ²
PC31/CLK1/BRGO1	AD1 ²
PD4/BRGO8/L1TSYNCD1/L1GNTD1/ $\overline{\text{FCC3_RTS}}$ /SMRXD2	AC28 ²
PD5/FCC1_UT16_TXD3/ $\overline{\text{DONE1}}$	AD27 ²
PD6/FCC1_UT16_TXD4/ $\overline{\text{DACK1}}$	AF29 ²
PD7/SMSYN1/FCC1_UTM_TXADDR3/FCC1_UTS_TXADDR3/ FCC2_UTM_TXADDR4/FCC1_TXCLAV2	AF28 ²
PD8/SMRXD1/FCC2_UT_TXPRTY/BRGO5	AG25 ²
PD9/SMTXD1/FCC2_UT_RXPRTY/BRGO3	AH26 ²
PD10/L1CLKOB2/FCC2_UT8_RXD1/L1RSYNCB1/BRGO4	AJ27 ²
PD11/ $\overline{\text{L1RQB2}}$ /FCC2_UT8_RXD0/L1TSYNCB1/L1GNTB1	AJ23 ²
PD12/SI1_L1ST2/L1RXDB1	AG23 ²
PD13/SI1_L1ST1/L1TXDB1	AJ22 ²
PD14/FCC1_UT16_RXD0/L1CLKOC2/I2CSCL	AE20 ²
PD15/FCC1_UT16_RXD1/ $\overline{\text{L1RQC2}}$ /I2CSDA	AJ20 ²
PD16/FCC1_UT_TXPRTY/L1TSYNCC1/L1GNTC1/SPIMISO	AG18 ²
PD17/FCC1_UT_RXPRTY/BRGO2/SPIMOSI	AG17 ²
PD18/FCC1_UTM_RXADDR4/FCC1_UTS_RXADDR4/ FCC1_UTM_RXCLAV3/FCC2_UTM_RXADDR3/SPICLK	AF16 ²
PD19/FCC1_UTM_TXADDR4/FCC1_UTS_TXADDR4/ FCC1_UTM_TXCLAV3/FCC2_UTM_TXADDR3/SPISEL/BRGO1	AH15 ²
PD20/ $\overline{\text{RTS4}}$ /TENA4/FCC1_UT16_RXD2/L1RSYNCA2	AJ14 ²

Table 21. Pinout List (continued)

Pin Name	Ball
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13 ²
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12 ²
PD23/ $\overline{\text{RTS3}}$ /TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12 ²
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10 ²
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9 ²
PD26/ $\overline{\text{RTS2}}$ /TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8 ²
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7 ²
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4 ²
PD29/ $\overline{\text{RTS1}}$ /TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4	AG1 ²
PD30/ $\overline{\text{FCC2_UTM_TXENB}}$ /FCC2_UTS_TXENB/TXD1	AD4 ²
PD31/RXD1	AD2 ²
VCCSYN	AB3
VCCSYN1	B9
GNDSYN	AB1
CLKIN2 ^{1,3}	AE11
SPARE4 ⁴	U5
$\overline{\text{PCI_MODE}}$ ^{1,5}	AF25
SPARE6 ⁴	V4
THERMAL0 ⁶	AA1
THERMAL1 ⁶	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

¹ MPC8265 and MPC8266 only.

² The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

6 Ordering Information

Figure 16 provides an example of the Freescale part numbering nomenclature for the MPC826xA. In addition to the processor frequency, the part numbering scheme also consists of a part modifier that indicates any enhancement(s) in the part from the original production design. Each part number also contains a revision code that refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only. For more information, contact your local Freescale sales office.

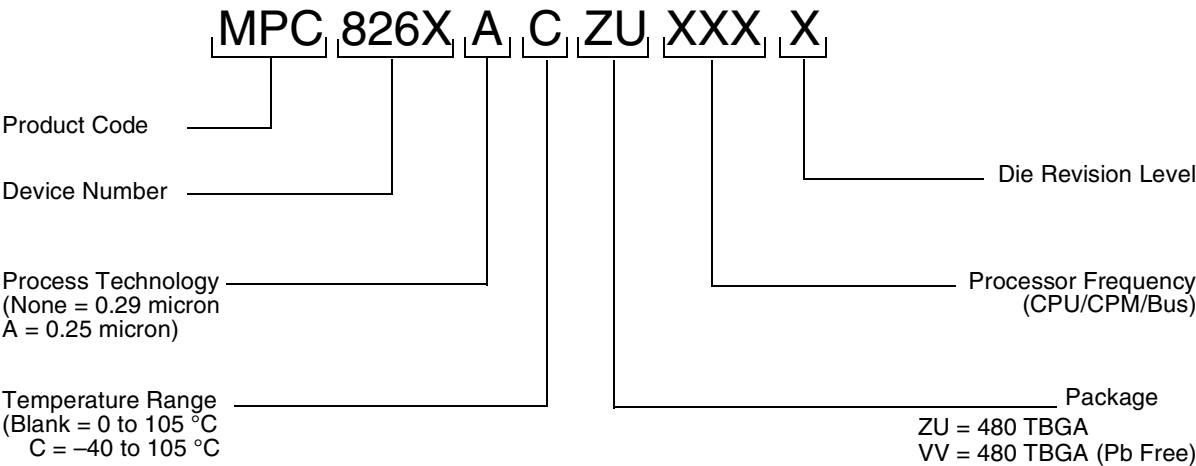


Figure 16. Freescale Part Number Key

7 Document Revision History

Table 23 lists significant changes in each revision of this document.

Table 23. Document Revision History

Revision	Date	Substantive Changes
2	06/2009	Updated package values in Figure 16.
1.1	02/2006	Addition of Table 12.
1.0	9/2005	Document template update