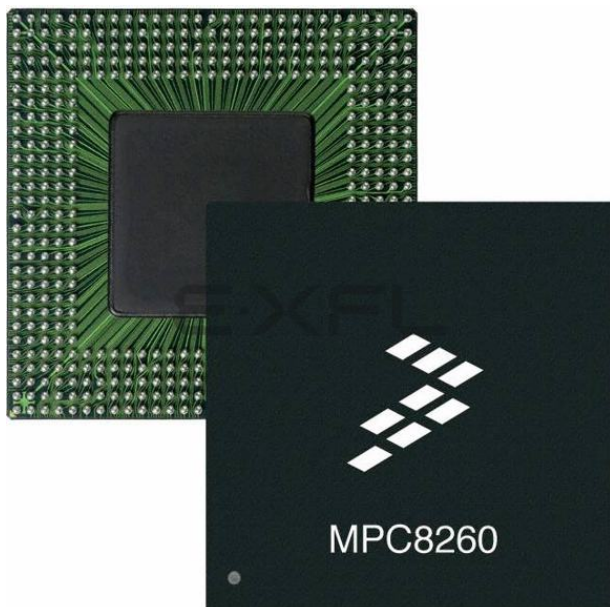




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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8265acvvmibc

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ $\overline{CS}[0-9]$ $\overline{CS}(10)/\overline{BCTL1}$ $\overline{CS}(11)/\overline{AP}(0)$ $\overline{BADDR}[27-28]$ $\overline{ALE}$ $\overline{BCTL0}$ $\overline{PWE}(0:7)/\overline{PSDDQM}(0:7)/\overline{PBS}(0:7)$ $\overline{PSDA10}/\overline{PGPL0}$ $\overline{PSDWE}/\overline{PGPL1}$ $\overline{POE}/\overline{PSDRAS}/\overline{PGPL2}$ $\overline{PSDCAS}/\overline{PGPL3}$ $\overline{PGTA}/\overline{PUPMWAIT}/\overline{PGPL4}/\overline{PPBS}$ $\overline{PSDAMUX}/\overline{PGPL5}$ $\overline{LWE}[0-3]/\overline{LSDDQM}[0-3]/\overline{LBS}[0-3]/\overline{PCI_CFG}[0-3]^3$ $\overline{LSDA10}/\overline{LGPL0}/\overline{PCI_MODCKH0}^3$ $\overline{LSDWE}/\overline{LGPL1}/\overline{PCI_MODCKH1}^3$ $\overline{LOE}/\overline{LSDRAS}/\overline{LGPL2}/\overline{PCI_MODCKH2}^3$ $\overline{LSDCAS}/\overline{LGPL3}/\overline{PCI_MODCKH3}^3$ $\overline{LGTA}/\overline{LUPMWAIT}/\overline{LGPL4}/\overline{LPBS}$ $\overline{LSDAMUX}/\overline{LGPL5}/\overline{PCI_MODCK}^3$ $\overline{LWR}$ $\overline{MODCK1}/\overline{AP}(1)/\overline{TC}(0)/\overline{BNKSEL}(0)$ $\overline{MODCK2}/\overline{AP}(2)/\overline{TC}(1)/\overline{BNKSEL}(1)$ $\overline{MODCK3}/\overline{AP}(3)/\overline{TC}(2)/\overline{BNKSEL}(2)$ $I_{OL} = 3.2\text{mA}$ $\overline{L_A14}/\overline{PAR}^3$ $\overline{L_A15}/\overline{FRAME}^3/\overline{SMI}$ $\overline{L_A16}/\overline{TRDY}^3$ $\overline{L_A17}/\overline{IRDY}^3/\overline{CKSTP_OUT}$ $\overline{L_A18}/\overline{STOP}^3$ $\overline{L_A19}/\overline{DEVSEL}^3$ $\overline{L_A20}/\overline{IDSEL}^3$ $\overline{L_A21}/\overline{PERR}^3$ $\overline{L_A22}/\overline{SERR}^3$ $\overline{L_A23}/\overline{REQ0}^3$ $\overline{L_A24}/\overline{REQ1}^3/\overline{HSEJSW}^3$ $\overline{L_A25}/\overline{GNT0}^3$ $\overline{L_A26}/\overline{GNT1}^3/\overline{HSLED}^3$ $\overline{L_A27}/\overline{GNT2}^3/\overline{HSENUM}^3$ $\overline{L_A28}/\overline{RST}^3/\overline{CORE_SRESET}$ $\overline{L_A29}/\overline{INTA}^3$ $\overline{L_A30}/\overline{REQ2}^3$ $\overline{L_A31}$ $\overline{LCL_D}(0-31)/\overline{AD}(0-31)^3$ $\overline{LCL_DP}(0-3)/\overline{C}/\overline{BE}(0-3)^3$ $\overline{PA}[0-31]$ $\overline{PB}[4-31]$ $\overline{PC}[0-31]$ $\overline{PD}[4-31]$ $\overline{TDO}$	V_{OL}	—	0.4	V

¹ The default configuration of the CPM pins ($\overline{PA}[0-31]$, $\overline{PB}[4-31]$, $\overline{PC}[0-31]$, $\overline{PD}[4-31]$) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

- ² The leakage current is measured for nominal VDD, VCCSYN, and VDD.
³ MPC8265 and MPC8266 only.

2.2 Thermal Characteristics

Table 4 describes thermal characteristics.

Table 4. Thermal Characteristics for 480 TBGA Package

Characteristics	Symbol	Value	Unit	Air Flow
Junction to ambient	θ_{JA}	13 ¹	°C/W	NC ²
		10 ¹		1 m/s
		11 ³		NC
		8 ³		1 m/s
Junction to board ⁴	θ_{JB}	4	°C/W	—
Junction to case ⁵	θ_{JC}	1.1	°C/W	—

- ¹ Assumes a single layer board with no thermal vias
² Natural convection
³ Assumes a four layer board
⁴ Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 Power Considerations

The average chip-junction temperature, T_J , in °C can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA}) \tag{1}$$

where

- T_A = ambient temperature °C
 θ_{JA} = package thermal resistance, junction to ambient, °C/W
 $P_D = P_{INT} + P_{I/O}$
 $P_{INT} = I_{DD} \times V_{DD}$ Watts (chip internal power)
 $P_{I/O}$ = power dissipation on input and output pins (determined by user)

For most applications $P_{I/O} < 0.3 \times P_{INT}$. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is the following:

$$P_D = K / (T_J + 273^\circ \text{C}) \tag{2}$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273^\circ \text{C}) + \theta_{JA} \times P_D^2 \tag{3}$$

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs¹

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

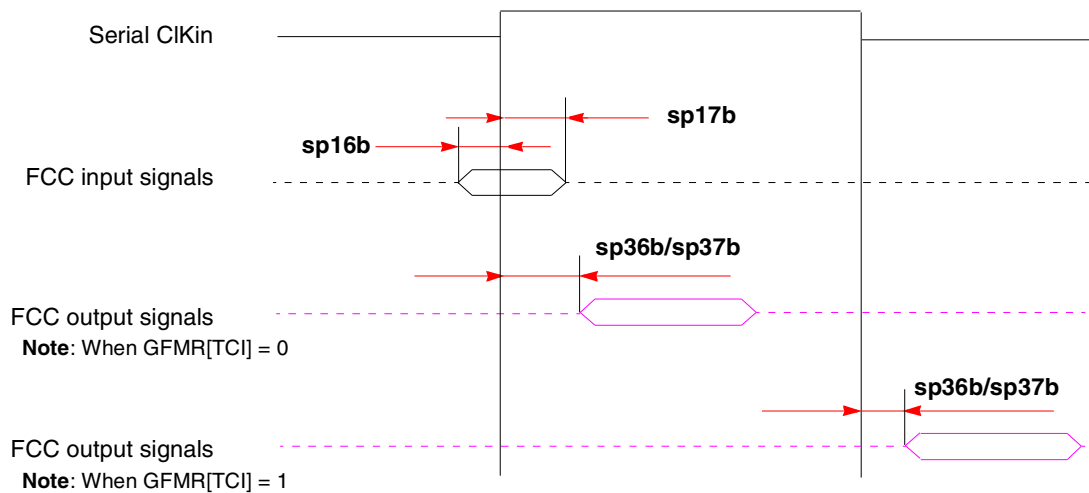


Figure 3. FCC External Clock Diagram

Figure 4 shows the FCC internal clock.

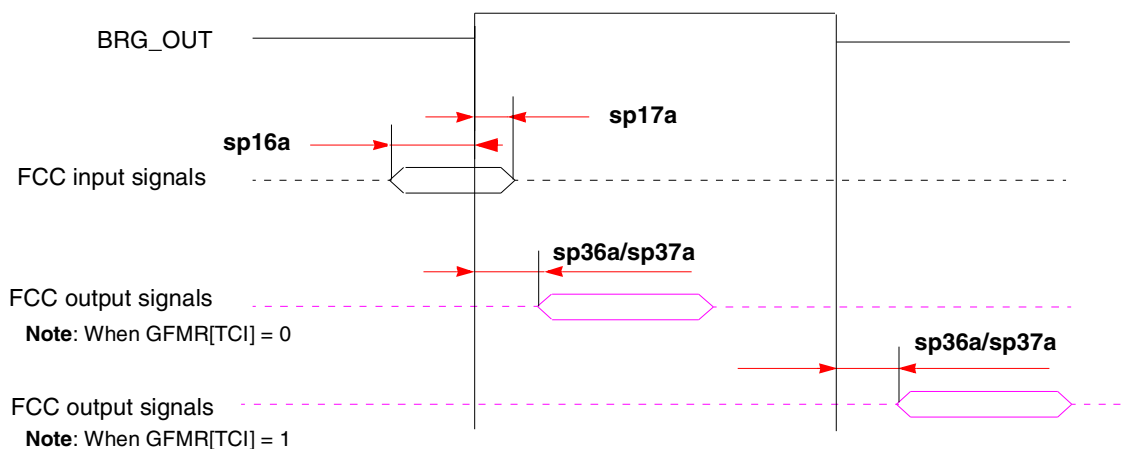
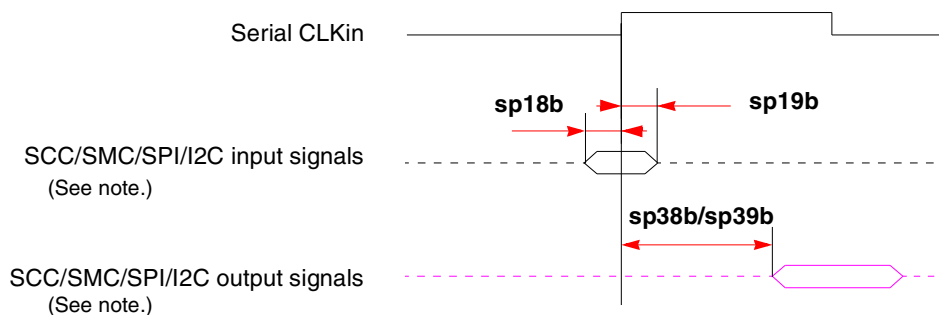


Figure 4. FCC Internal Clock Diagram

Figure 5 shows the SCC/SMC/SPI/I²C external clock.

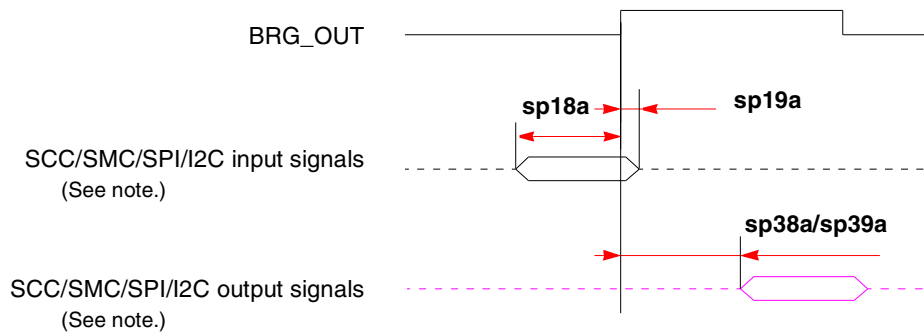


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 5. SCC/SMC/SPI/I²C External Clock Diagram

Figure 6 shows the SCC/SMC/SPI/I²C internal clock.

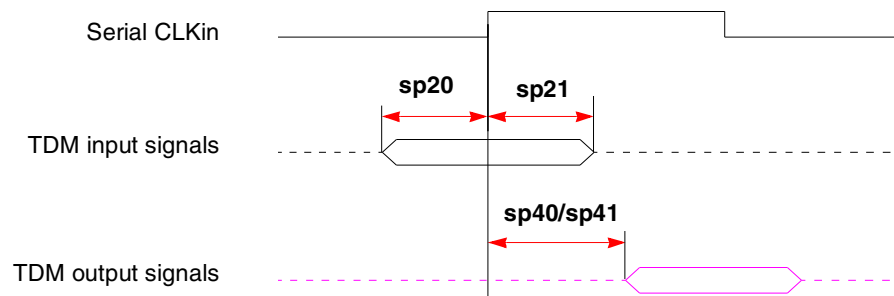


Note: There are four possible timing conditions for SCC and SPI:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 6. SCC/SMC/SPI/I²C Internal Clock Diagram

Figure 7 shows TDM input and output signals.



Note: There are four possible TDM timing conditions:

1. Input sampled on the rising edge and output driven on the rising edge (shown).
2. Input sampled on the rising edge and output driven on the falling edge.
3. Input sampled on the falling edge and output driven on the falling edge.
4. Input sampled on the falling edge and output driven on the rising edge.

Figure 7. TDM Signal Diagram

Table 10 lists SIU output characteristics.

Table 10. AC Characteristics for SIU Outputs¹

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp31	sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	7	6	0.5	0.5
sp32	sp30	ADD/ADD_atr./BADDR/CI/GBL/WT	8	6.5	0.5	0.5
sp33a	sp30	Data bus	6.5	6.5	0.5	0.5
sp33b	sp30	DP	8	7	0.5	0.5
sp34	sp30	Memory controller signals/ALE	6	5	0.5	0.5
sp35	sp30	All other signals	6	5.5	0.5	0.5

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

NOTE

Activating data pipelining (setting BRx[DR] in the memory controller) improves the AC timing. When data pipelining is activated, sp12 can be used for data bus setup even when ECC or PARITY are used. Also, sp33a can be used as the AC specification for DP signals.

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 13 lists the eight basic configuration modes. Table 14 lists the other modes that are available by using the configuration pin ($\overline{\text{RSTCONF}}$) and driving four bits from hardware configuration word on the data bus.

Note that the MPC8265 and the MPC8266 have two additional clocking modes—PCI agent and PCI host. Refer to Section 3.2, “PCI Mode” on page 26 for information.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 13 describes default clock modes for the MPC826xA.

Table 13. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note that basic modes are shown in boldface type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

Table 14. Clock Configuration Modes¹

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3}	CPM Multiplication Factor ²	CPM Frequency ²	Core Multiplication Factor ²	Core Frequency ²
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

Table 14. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3}	CPM Multiplication Factor ²	CPM Frequency ²	Core Multiplication Factor ²	Core Frequency ²
0001_101	33 MHz	3	100 MHz	4	133 MHz
0001_110	33 MHz	3	100 MHz	5	166 MHz
0001_111	33 MHz	3	100 MHz	6	200 MHz
0010_000	33 MHz	3	100 MHz	7	233 MHz
0010_001	33 MHz	3	100 MHz	8	266 MHz
0010_010	33 MHz	4	133 MHz	4	133 MHz
0010_011	33 MHz	4	133 MHz	5	166 MHz
0010_100	33 MHz	4	133 MHz	6	200 MHz
0010_101	33 MHz	4	133 MHz	7	233 MHz
0010_110	33 MHz	4	133 MHz	8	266 MHz
0010_111	33 MHz	5	166 MHz	4	133 MHz
0011_000	33 MHz	5	166 MHz	5	166 MHz
0011_001	33 MHz	5	166 MHz	6	200 MHz
0011_010	33 MHz	5	166 MHz	7	233 MHz
0011_011	33 MHz	5	166 MHz	8	266 MHz
0011_100	33 MHz	6	200 MHz	4	133 MHz
0011_101	33 MHz	6	200 MHz	5	166 MHz
0011_110	33 MHz	6	200 MHz	6	200 MHz
0011_111	33 MHz	6	200 MHz	7	233 MHz
0100_000	33 MHz	6	200 MHz	8	266 MHz
0100_001	Reserved				
0100_010					
0100_011					
0100_100					
0100_101					
0100_110					

3.2.1 PCI Host Mode

The frequencies listed in [Table 16](#) and [Table 17](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 16. Clock Default Configurations in PCI Host Mode (MODCK_HI = 0000)

MODCK[1–3] ¹	Input Clock Frequency (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
010	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
011	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
100	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
101	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
110	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
111	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz

¹ Assumes MODCK_HI = 0000.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) Refer to [Table 15](#).

[Table 17](#) describes all possible clock configurations when using the MPC8265's or the MPC8266's internal PCI bridge in host mode.

Table 17. Clock Configuration Modes in PCI Host Mode

MODCK_H – MODCK[1–3]	Input Clock Frequency ¹ (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
0001_000	33 MHz	3	100 MHz	5	166 MHz	3/6	33/16 MHz
0001_001	33 MHz	3	100 MHz	6	200 MHz	3/6	33/16 MHz
0001_010	33 MHz	3	100 MHz	7	233 MHz	3/6	33/16 MHz
0001_011	33 MHz	3	100 MHz	8	266 MHz	3/6	33/16 MHz
0010_000	33 MHz	4	133 MHz	5	166 MHz	4/8	33/16 MHz
0010_001	33 MHz	4	133 MHz	6	200 MHz	4/8	33/16 MHz
0010_010	33 MHz	4	133 MHz	7	233 MHz	4/8	33/16 MHz
0010_011	33 MHz	4	133 MHz	8	266 MHz	4/8	33/16 MHz
0011_000 ³	33 MHz	5	166 MHz	5	166 MHz	5	33 MHz
0011_001 ³	33 MHz	5	166 MHz	6	200 MHz	5	33 MHz
0011_010 ³	33 MHz	5	166 MHz	7	233 MHz	5	33 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency ¹ (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
0011_011 ³	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000 ³	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001 ³	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010 ³	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011 ³	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
0101_001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	66 MHz	2.5	166 MHz	2.5	166 MHz	3/6	55/28 MHz
0110_001	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency ¹ (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

¹ Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to [Table 15](#).

³ In this mode, PCI_MODCK must be "0".

3.2.2 PCI Agent Mode

The frequencies listed in [Table 18](#) and [Table 19](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

MODCK[1–3] ¹	Input Clock Frequency (PCI) ²	CPM Multiplication Factor ²	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) ^{1,2}	CPM Multiplication Factor ¹	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
1010_001	66/33 MHz	4/8	266 MHz	3	266 MHz	3	88 MHz
1010_010	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
1010_011	66/33 MHz	4/8	266 MHz	4	350 MHz	3	88 MHz
1010_100	66/33 MHz	4/8	266 MHz	4.5	400 MHz	3	88 MHz
1011_000	66/33 MHz	4/8	266 MHz	2	212MHz	2.5	106 MHz
1011_001	66/33 MHz	4/8	266 MHz	2.5	265 MHz	2.5	106 MHz
1011_010	66/33 MHz	4/8	266 MHz	3	318 MHz	2.5	106 MHz
1011_011	66/33 MHz	4/8	266 MHz	3.5	371 MHz	2.5	106 MHz
1011_100	66/33 MHz	4/8	266 MHz	4	424 MHz	2.5	106 MHz

- ¹ The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to [Table 15](#).
- ² Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.
- ³ Core frequency = (60x bus frequency)(core multiplication factor)
- ⁴ Bus frequency = CPM frequency/bus division factor
- ⁵ In this mode, PCI_MODCK must be "1".

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

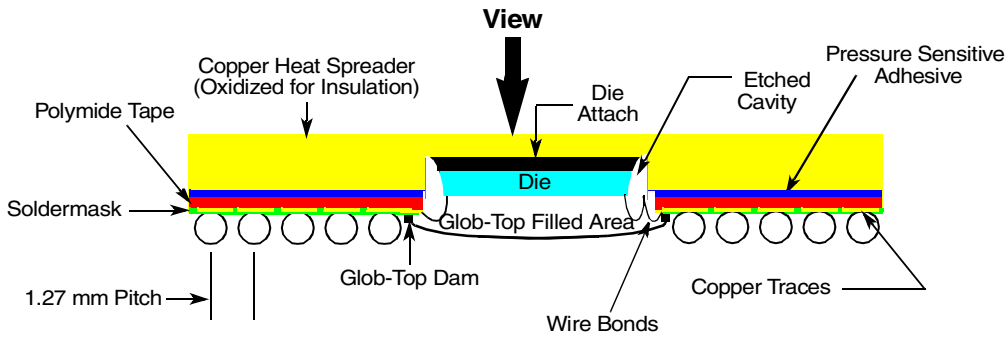


Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as $\overline{TA}$, are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

Table 21. Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2

Table 21. Pinout List (continued)

Pin Name	Ball
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6

Table 21. Pinout List (continued)

Pin Name	Ball
LCL_D31/AD31 ¹	AA28
LCL_DP0/C0 ¹ /BE0 ¹	L28
LCL_DP1/C1 ¹ /BE1 ¹	N28
LCL_DP2/C2 ¹ /BE2 ¹	T28
LCL_DP3/C3 ¹ /BE3 ¹	W28
IRQ0/NMI_OUT	T1
IRQ7/INT_OUT/APE	D1
TRST	AH3
TCK	AG5
TMS	AJ3
TDI	AE6
TDO	AF5
TRIS	AB4
PORESET	AG6
HRESET	AH5
SRESET	AF6
QREQ	AA3
RSTCONF	AJ4
MODCK1/AP1/TC0/BNKSEL0	W2
MODCK2/AP2/TC1/BNKSEL1	W3
MODCK3/AP3/TC2/BNKSEL2	W4
XFC	AB2
CLKIN1	AH4
PA0/RESTART1/DREQ3/FCC2_UTM_TXADDR2	AC29 ²
PA1/REJECT1/FCC2_UTM_TXADDR1/DONE3	AC25 ²
PA2/CLK20/FCC2_UTM_TXADDR0/DACK3	AE28 ²
PA3/CLK19/FCC2_UTM_RXADDR0/DACK4/L1RXD1A2	AG29 ²
PA4/REJECT2/FCC2_UTM_RXADDR1/DONE4	AG28 ²
PA5/RESTART2/DREQ4/FCC2_UTM_RXADDR2	AG26 ²
PA6/L1RSYNCA1	AE24 ²
PA7/SMSYN2/L1TSYNCA1/L1GNTA1	AH25 ²
PA8/SMRXD2/L1RXD0A1/L1RXDA1	AF23 ²
PA9/SMTXD2/L1TXD0A1	AH23 ²
PA10/FCC1_UT8_RXD0/FCC1_UT16_RXD8/MSNUM5	AE22 ²
PA11/FCC1_UT8_RXD1/FCC1_UT16_RXD9/MSNUM4	AH22 ²

Table 21. Pinout List (continued)

Pin Name	Ball
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21 ²
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20 ²
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19 ²
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18 ²
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17 ²
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16 ²
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16 ²
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15 ²
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13 ²
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13 ²
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12 ²
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11 ²
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9 ²
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8 ²
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7 ²
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7 ²
PA28/FCC1_UTM_RXENB/FCC1_UTS_RXENB/FCC1_MII_TX_EN	AD5 ²
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1 ²
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/ FCC1_RTS	AD3 ²
PA31/FCC1_UTM_TXENB/FCC1_UTS_TXENB/FCC1_MII_COL	AB5 ²
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/FCC3_RTS	AD28 ²
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26 ²
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25 ²
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26 ²
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27 ²
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24 ²
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24 ²
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24 ²
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22 ²
PB13/FCC3_MII_COL/L1RQB1/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21 ²
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20 ²
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19 ²
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18 ²
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17 ²

Table 21. Pinout List (continued)

Pin Name	Ball
PB18/FCC2_UT8_RXD4/FCC2_RXD3/L1CLKOD2/L1RXD2A2	AE14 ²
PB19/FCC2_UT8_RXD5/FCC2_RXD2/L1RQD2/L1RXD3A2	AF13 ²
PB20/FCC2_UT8_RXD6/FCC2_RXD1/L1RSYNCD2/L1TXD1A1	AG12 ²
PB21/FCC2_UT8_RXD7/FCC2_RXD0/FCC2_RXD/L1TSYNCD2/L1GNTD2/L1TXD2A1	AH11 ²
PB22/FCC2_UT8_TXD7/FCC2_TXD0/FCC2_TXD/L1RXD1A1/L1RXDD2	AH16 ²
PB23/FCC2_UT8_TXD6/FCC2_TXD1/L1RXD2A1/L1TXDD2	AE15 ²
PB24/FCC2_UT8_TXD5/FCC2_TXD2/L1RXD3A1/L1RSYNCC2	AJ9 ²
PB25/FCC2_UT8_TXD4/FCC2_TXD3/L1TSYNCC2/L1GNTC2/L1TXD3A1	AE9 ²
PB26/FCC2_MII_CRS/FCC2_UT8_TXD1/L1RXDC2	AJ7 ²
PB27/FCC2_MII_COL/FCC2_UT8_TXD0/L1TXDC2	AH6 ²
PB28/FCC2_MII_RX_ER/FCC2_RTS/L1TSYNCB2/L1GNTB2/TXD1	AE3 ²
PB29/FCC2_UTM_RXCLAV/FCC2_UTS_RXCLAV/L1RSYNCB2/FCC2_MII_TX_EN	AE2 ²
PB30/FCC2_MII_RX_DV/FCC2_UT_TXSOC/L1RXDB2	AC5 ²
PB31/FCC2_MII_TX_ER/FCC2_UT_RXSOC/L1TXDB2	AC4 ²
PC0/DREQ1/BRGO7/SMSYN2/L1CLKOA2	AB26 ²
PC1/DREQ2/BRGO6/L1RQA2	AD29 ²
PC2/FCC3_CD/FCC2_UT8_TXD3/DONE2	AE29 ²
PC3/FCC3_CTS/FCC2_UT8_TXD2/DACK2/CTS4	AE27 ²
PC4/FCC2_UTM_RXENB/FCC2_UTS_RXENB/SI2_L1ST4/FCC2_CD	AF27 ²
PC5/FCC2_UTM_TXCLAV/FCC2_UTS_TXCLAV/SI2_L1ST3/FCC2_CTS	AF24 ²
PC6/FCC1_CD/L1CLKOC1/FCC1_UTM_RXADDR2/FCC1_UTS_RXADDR/FCC1_UTM_RXCLAV1	AJ26 ²
PC7/FCC1_CTS/L1RQC1/FCC1_UTM_TXADDR2/FCC1_UTS_TXADDR2/FCC1_UTM_TXCLAV1	AJ25 ²
PC8/CD4/RENA4/FCC1_UT16_TXD0/SI2_L1ST2/CTS3	AF22 ²
PC9/CTS4/CLSN4/FCC1_UT16_TXD1/SI2_L1ST1/L1TSYNCA2/L1GNTA2	AE21 ²
PC10/CD3/RENA3/FCC1_UT16_TXD2/SI1_L1ST4/FCC2_UT8_RXD3	AF20 ²
PC11/CTS3/CLSN3/L1CLKOD1/L1TXD3A2/FCC2_UT8_RXD2	AE19 ²
PC12/CD2/RENA2/SI1_L1ST3/FCC1_UTM_RXADDR1/FCC1_UTS_RXADDR1	AE18 ²
PC13/CTS2/CLSN2/L1RQD1/FCC1_UTM_TXADDR1/FCC1_UTS_TXADDR1	AH18 ²
PC14/CD1/RENA1/FCC1_UTM_RXADDR0/FCC1_UTS_RXADDR0	AH17 ²
PC15/CTS1/CLSN1/SMTXD2/FCC1_UTM_TXADDR0/FCC1_UTS_TXADDR0	AG16 ²

Table 21. Pinout List (continued)

Pin Name	Ball
PD21/TXD4/FCC1_UT16_RXD3/L1RXD0A2/L1RXDA2	AH13 ²
PD22/RXD4/FCC1_UT16_TXD5/L1TXD0A2/L1TXDA2	AJ12 ²
PD23/ $\overline{\text{RTS3}}$ /TENA3/FCC1_UT16_RXD4/L1RSYNCD1	AE12 ²
PD24/TXD3/FCC1_UT16_RXD5/L1RXDD1	AF10 ²
PD25/RXD3/FCC1_UT16_TXD6/L1TXDD1	AG9 ²
PD26/ $\overline{\text{RTS2}}$ /TENA2/FCC1_UT16_RXD6/L1RSYNCC1	AH8 ²
PD27/TXD2/FCC1_UT16_RXD7/L1RXDC1	AG7 ²
PD28/RXD2/FCC1_UT16_TXD7/L1TXDC1	AE4 ²
PD29/ $\overline{\text{RTS1}}$ /TENA1/FCC1_UTM_RXADDR3/FCC1_UTS_RXADDR3/ FCC1_UTM_RXCLAV2/FCC2_UTM_RXADDR4	AG1 ²
PD30/ $\overline{\text{FCC2_UTM_TXENB}}$ /FCC2_UTS_TXENB/TXD1	AD4 ²
PD31/RXD1	AD2 ²
VCCSYN	AB3
VCCSYN1	B9
GNDSYN	AB1
CLKIN2 ^{1,3}	AE11
SPARE4 ⁴	U5
$\overline{\text{PCI_MODE}}$ ^{1,5}	AF25
SPARE6 ⁴	V4
THERMAL0 ⁶	AA1
THERMAL1 ⁶	AG4
I/O power	AG21, AG14, AG8, AJ1, AJ2, AH1, AH2, AG3, AF4, AE5, AC27, Y27, T27, P27, K26, G27, AE25, AF26, AG27, AH28, AH29, AJ28, AJ29, C7, C14, C16, C20, C23, E10, A28, A29, B28, B29, C27, D26, E25, H3, M4, T3, AA4, A1, A2, B1, B2, C3, D4, E5
Core Power	U28, U29, K28, K29, A9, A19, B19, M1, M2, Y1, Y2, AC1, AC2, AH19, AJ19, AH10, AJ10, AJ5
Ground	AA5, AF21, AF14, AF8, AE7, AF11, AE17, AE23, AC26, AB25, Y26, V25, T26, R25, P26, M25, K27, H25, G26, D7, D10, D14, D16, D20, D23, C9, E11, E13, E15, E19, E22, B3, G5, H4, K5, M3, P5, T4, Y5, AA2, AC3

¹ MPC8265 and MPC8266 only.

² The default configuration of the CPM pins (PA[0–31], PB[4–31], PC[0–31], PD[4–31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

Package Description

- ³ On PCI devices (MPC8265 and MPC8266) this pin should be used as CLKIN2. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled down or left floating.
- ⁴ Must be pulled down or left floating.
- ⁵ On PCI devices (MPC8265 and MPC8266) this pin should be asserted if the PCI function is desired or pulled up or left floating if PCI is not desired. On non-PCI devices (MPC8260A and MPC8264) this is a spare pin that must be pulled up or left floating.
- ⁶ For information on how to use this pin, refer to *MPC8260 PowerQUICC II Thermal Resistor Guide* available at www.freescale.com.

5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC826xA.

5.1 Package Parameters

Package parameters are provided in [Table 22](#). The package type is a 37.5 × 37.5 mm, 480-lead TBGA.

Table 22. Package Parameters

Parameter	Value
Package Outline	37.5 × 37.5 mm
Interconnects	480 (29 × 29 ball array)
Pitch	1.27 mm
Nominal unmounted package height	1.55 mm

Table 23. Document Revision History (continued)

Revision	Date	Substantive Changes
0.9	8/2003	- Note: In revision 0.3, sp30 (Table 10) was changed. This change was not previously recorded in this “Document Revision History” Table. - Removal of “HiP4 PowerQUICC II Documentation” table. These supplemental specifications have been replaced by revision 1 of the <i>MPC8260 PowerQUICC II™ Family Reference Manual</i>. Figure 1 and Section 1, “Features”: Addition of MPC8255 notes - Addition of Figure 2 - Addition of VCCSYN to “Note: Core, PLL, and I/O Supply Voltages” following Table 2 - Addition of note 1 to Table 3 Table 4: Changes to θ_{JA} and θ_{JB} and θ_{JC}. - Addition of notes or modifications to Figure 6, Figure 7, and Figure 8 Table 9: Change of sp10. - Addition of Table 15. - Addition of note 2 to Table 21 Table 21: Addition of FCC2 Rx and Tx [3,4] to CPM pins PD7, PD18, PD19, and PD29. Also, the addition of SPICLK to PC19. They are documented correctly in the parallel I/O ports chapter in the <i>MPC8260 PowerQUICC II™ Family Reference Manual</i> but had previously been omitted from Table 21.
0.8	1/2003	Table 2: Modification to supply voltage ranges reflected in notes 2, 3, and 4. Table 4: Addition of θ_{JB} and θ_{JC}. Table 7, Figure 8: Addition of sp42a/sp43a. Figure 3, Figure 4: Addition of note for FCC output. Figure 5, Figure 6, Figure 7: Addition of notes. Table 14, Table 17, and Table 19: Removal of PLL bypass mode from clock tables.
0.7	5/2002	Section 1, “Features”: minimum supported core frequency of 150 MHz Section 1, “Features”: updated performance values (under “Dual-issue integer core”) Table 2: Note 2 (changes in italics): “...less than or equal to 233 MHz, 166 MHz CPM...” Table 2: Addition of note 3.
0.6	3/2002	Table 21: Modified notes to pins AE11 and AF25.
0.5	3/2002	Table 21: Modified notes to pins AE11 and AF25. Table 21: Addition of note to pins AA1 and AG4 (Therm0 and Therm1).
0.4	2/2002	- Note 2 for Table 2 (changes in italics): “...greater than or equal to 266 MHz, 200 MHz CPM...” Table 19: Core and bus frequency values for the following ranges of MODCK_HMODCK: 0011_000 to 0011_100 and 1011_000 to 1011_1000 Table 21: Notes added to pins at AE11, AF25, U5, and V4.
0.3	11/2001	Table 1: note 3 Section 2.1: Removal of “Warning” recommending use of bootstrap diodes. They are not needed. Table 9: Change to sp12. Table 10: Change to sp32. - Note 2 for Table 16 and Table 17 - Addition of note at beginning of Section 3.2 - Note 1 for Table 18 and Table 19 Table 21: Additions to B27, C28, D25, D27, E26, G29, H26–28, N25, P29, AF25, AA25, AB27
0.2	11/2001	- Revision of Table 5, “Power Dissipation” - Modifications to Figure 9, Table 2, Table 10, Table 11, and Table 18 - Modification to pinout diagram, Figure 13 - Additional revisions to text and figures throughout
0.1	8/2001	Table 8: Change to sp20/sp21.
0	—	Initial version