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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC G2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	Communications; RISC CPM
RAM Controllers	DRAM, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (3)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	480-LBGA Exposed Pad
Supplier Device Package	480-TBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8265azumhbc

- PowerPC architecture-compliant memory management unit (MMU)
- Common on-chip processor (COP) test interface
- High-performance (6.6–7.65 SPEC95 benchmark at 300 MHz; 1.68 MIPS/MHz without inlining and 1.90 Dhrystones MIPS/MHz with
- Supports bus snooping for data cache coherency
- Floating-point unit (FPU)
- Separate power supply for internal logic and for I/O
- Separate PLLs for G2 core and for the CPM
 - G2 core and CPM can run at different frequencies for power/performance optimization
 - Internal core/bus clock multiplier that provides 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
 - Internal CPM/bus clock multiplier that provides 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 5:1, 6:1 ratios
- 64-bit data and 32-bit address 60x bus
 - Bus supports multiple master designs
 - Supports single- and four-beat burst transfers
 - 64-, 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
 - Supports data parity or ECC and address parity
- 32-bit data and 18-bit address local bus
 - Single-master bus, supports external slaves
 - Eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by on-chip memory controller
- 60x-to-PCI bridge (MPC8265 and MPC8266 only)
 - Programmable host bridge and agent
 - 32-bit data bus, 66 MHz, 3.3 V
 - Synchronous and asynchronous 60x and PCI clock modes
 - All internal address space available to external PCI host
 - DMA for memory block transfers
 - PCI-to-60x address remapping
- System interface unit (SIU)
 - Clock synthesizer
 - Reset controller
 - Real-time clock (RTC) register
 - Periodic interrupt timer
 - Hardware bus monitor and software watchdog timer
 - IEEE Std. 1149.1™ standard JTAG test access port
- Twelve-bank memory controller
 - Glueless interface to SRAM, page mode SDRAM, DRAM, EPROM, Flash and other user-definable peripherals
 - Byte write enables and selectable parity generation

- Coset removing (programmable by the user)
- Filtering idle/unassigned cells (programmable by the user)
- Performing HEC error detection and single bit error correction (programmable by user)
- Generating loss of cell delineation status/interrupt (LOC/LCD)
- Operates with FCC2 (UTOPIA 8)
- Provides serial loop back mode
- Cell echo mode is provided
- Supports both FCC transmit modes
 - External rate mode—Idle cells are generated by the FCC (microcode) to control data rate.
 - Internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate.
- Supports TC-layer and PMD-WIRE interface (according to the ATM-Forum af-phy-0063.000)
- Cell counters for performance monitoring
 - 16-bit counters count
 - HEC error cells
 - HEC single bit error and corrected cells
 - Idle/unassigned cells filtered
 - Idle/unassigned cells transmitted
 - Transmitted ATM cells
 - Received ATM cells
 - Maskable interrupt is sent to the host when a counter expires
- Overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
- May be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported
- PCI bridge (MPC8265 and MPC8266 only)
 - PCI Specification Revision 2.2 compliant and supports frequencies up to 66 MHz
 - On-chip arbitration
 - Support for PCI to 60x memory and 60x memory to PCI streaming
 - PCI Host Bridge or Peripheral capabilities
 - Includes 4 DMA channels for the following transfers:
 - PCI-to-60x to 60x-to-PCI
 - 60x-to-PCI to PCI-to-60x
 - PCI-to-60x to PCI-to-60x
 - 60x-to-PCI to 60x-to-PCI
 - Includes all of the configuration registers (which are automatically loaded from the EPROM and used to configure the MPC8265) required by the PCI standard as well as message and doorbell registers
 - Supports the I₂O standard

- Hot-Swap friendly (supports the Hot Swap Specification as defined by PICMG 2.1 R1.0 August 3, 1998)
- Support for 66 MHz, 3.3 V specification
- 60x-PCI bus core logic which uses a buffer pool to allocate buffers for each port
- Makes use of the local bus signals, so there is no need for additional pins

2 Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the MPC826xA.

2.1 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MPC826xA. [Table 1](#) shows the maximum electrical ratings.

Table 1. Absolute Maximum Ratings¹

Rating	Symbol	Value	Unit
Core supply voltage ²	VDD	-0.3 – 2.5	V
PLL supply voltage ²	VCCSYN	-0.3 – 2.5	V
I/O supply voltage ³	VDDH	-0.3 – 4.0	V
Input voltage ⁴	VIN	GND(-0.3) – 3.6	V
Junction temperature	T _j	120	°C
Storage temperature range	T _{STG}	(-55) – (+150)	°C

¹ Absolute maximum ratings are stress ratings only; functional operation (see [Table 2](#)) at the maximums is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage.

² **Caution:** VDD/VCCSYN must not exceed VDDH by more than 0.4 V at any time, including during power-on reset.

³ **Caution:** VDDH can exceed VDD/VCCSYN by 3.3 V during power on reset by no more than 100 mSec. VDDH should not exceed VDD/VCCSYN by more than 2.5 V during normal operation.

⁴ **Caution:** VIN must not exceed VDDH by more than 2.5 V at any time, including during power-on reset.

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 7.0 \text{ mA}$ \overline{BR} \overline{BG} $\overline{ABB/IRQ2}$ \overline{TS} $A[0-31]$ $\overline{TT[0-4]}$ \overline{TBST} $\overline{TSIZE[0-3]}$ \overline{AACK} \overline{ARTRY} \overline{DBG} $\overline{DBB/IRQ3}$ $\overline{D[0-63]}$ $\overline{DP(0)/RSRV/EXT_BR2}$ $\overline{DP(1)/IRQ1/EXT_BG2}$ $\overline{DP(2)/TLBISYNC/IRQ2/EXT_DBG2}$ $\overline{DP(3)/IRQ3/EXT_BR3/CKSTP_OUT}$ $\overline{DP(4)/IRQ4/EXT_BG3/CORE_SREST}$ $\overline{DP(5)/TBEN/IRQ5/EXT_DBG3}$ $\overline{DP(6)/CSE(0)/IRQ6}$ $\overline{DP(7)/CSE(1)/IRQ7}$ \overline{PSDVAL} \overline{TA} \overline{TEA} $\overline{GBL/IRQ1}$ $\overline{CI/BADDR29/IRQ2}$ $\overline{WT/BADDR30/IRQ3}$ $\overline{L2_HIT/IRQ4}$ $\overline{CPU_BG/BADDR31/IRQ5}$ $\overline{CPU_DBG}$ $\overline{CPU_BR}$ $\overline{IRQ0/NMI_OUT}$ $\overline{IRQ7/INT_OUT/APE}$ $\overline{PORESET}$ \overline{HRESET} \overline{SRESET} $\overline{RSTCONF}$ \overline{QREQ}	V_{OL}	—	0.4	V

Table 3. DC Electrical Characteristics¹ (continued)

Characteristic	Symbol	Min	Max	Unit
$I_{OL} = 5.3\text{mA}$ CS[0-9] CS(10)/BCTL1 CS(11)/AP(0) BADDR[27-28] ALE BCTL0 PWE(0:7)/PSDDQM(0:7)/PBS(0:7) PSDA10/PGPL0 PSDWE/PGPL1 POE/PSDRAS/PGPL2 PSDCAS/PGPL3 PGTA/PUPMWAIT/PGPL4/PPBS PSDAMUX/PGPL5 LWE[0-3]/LSDDQM[0-3]/LBS[0-3]/PCI_CFG[0-3] ³ LSDA10/LGPL0/PCI_MODCKH0 ³ LSDWE/LGPL1/PCI_MODCKH1 ³ LOE/LSDRAS/LGPL2/PCI_MODCKH2 ³ LSDCAS/LGPL3/PCI_MODCKH3 ³ LGTA/LUPMWAIT/LGPL4/LPBS LSDAMUX/LGPL5/PCI_MODCK ³ LWR MODCK1/AP(1)/TC(0)/BNKSEL(0) MODCK2/AP(2)/TC(1)/BNKSEL(1) MODCK3/AP(3)/TC(2)/BNKSEL(2) $I_{OL} = 3.2\text{mA}$ L_A14/PAR ³ L_A15/FRAME ³ /SMI L_A16/TRDY ³ L_A17/IRDY ³ /CKSTP_OUT L_A18/STOP ³ L_A19/DEVSEL ³ L_A20/IDSEL ³ L_A21/PERR ³ L_A22/SERR ³ L_A23/REQ0 ³ L_A24/REQ1 ³ /HSEJSW ³ L_A25/GNT0 ³ L_A26/GNT1 ³ /HSELED ³ L_A27/GNT2 ³ /HSENUM ³ L_A28/RST ³ /CORE_SRESET L_A29/INTA ³ L_A30/REQ2 ³ L_A31 LCL_D(0-31)/AD(0-31) ³ LCL_DP(0-3)/C/BE(0-3) ³ PA[0-31] PB[4-31] PC[0-31] PD[4-31] TDO	V_{OL}	—	0.4	V

¹ The default configuration of the CPM pins (PA[0-31], PB[4-31], PC[0-31], PD[4-31]) is input. To prevent excessive DC current, it is recommended to either pull unused pins to GND or VDDH, or to configure them as outputs.

2.4 AC Electrical Characteristics

The following sections include illustrations and tables of clock diagrams, signals, and CPM outputs and inputs for the 66 MHz MPC826xA device. Note that AC timings are based on a 50-pf load. Typical output buffer impedances are shown in [Table 6](#).

Table 6. Output Buffer Impedances¹

Output Buffers	Typical Impedance (Ω)
60x bus	40
Local bus	40
Memory controller	40
Parallel I/O	46
PCI	25

¹ These are typical values at 65° C. The impedance may vary by $\pm 25\%$ with process and temperature.

[Table 7](#) lists CPM output characteristics.

Table 7. AC Characteristics for CPM Outputs¹

Spec Number		Characteristic	Max Delay (ns)		Min Delay (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp36a	sp37a	FCC outputs—internal clock (NMSI)	6	5.5	1	1
sp36b	sp37b	FCC outputs—external clock (NMSI)	14	12	2	1
sp40	sp41	TDM outputs/SI	25	16	5	4
sp38a	sp39a	SCC/SMC/SPI/I2C outputs—internal clock (NMSI)	19	16	1	0.5
sp38b	sp39b	Ex_SCC/SMC/SPI/I2C outputs—external clock (NMSI)	19	16	2	1
sp42	sp43	TIMER/IDMA outputs	14	11	1	0.5
sp42a	sp43a	PIO outputs	14	11	0.5	0.5

¹ Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.

Table 8 lists CPM input characteristics.

Table 8. AC Characteristics for CPM Inputs¹

Spec Number		Characteristic	Setup (ns)		Hold (ns)	
Max	Min		66 MHz	83 MHz	66 MHz	83 MHz
sp16a	sp17a	FCC inputs—internal clock (NMSI)	10	8	0	0
sp16b	sp17b	FCC inputs—external clock (NMSI)	3	2.5	3	2
sp20	sp21	TDM inputs/SI	15	12	12	10
sp18a	sp19a	SCC/SMC/SPI/I2C inputs—internal clock (NMSI)	20	16	0	0
sp18b	sp19b	SCC/SMC/SPI/I2C inputs—external clock (NMSI)	5	4	5	4
sp22	sp23	PIO/TIMER/IDMA inputs	10	8	3	3

¹ Input specifications are measured from the 50% level of the signal to the 50% level of the rising edge of CLKIN. Timings are measured at the pin.

Note that although the specifications generally reference the rising edge of the clock, the following AC timing diagrams also apply when the falling edge is the active edge.

Figure 3 shows the FCC external clock.

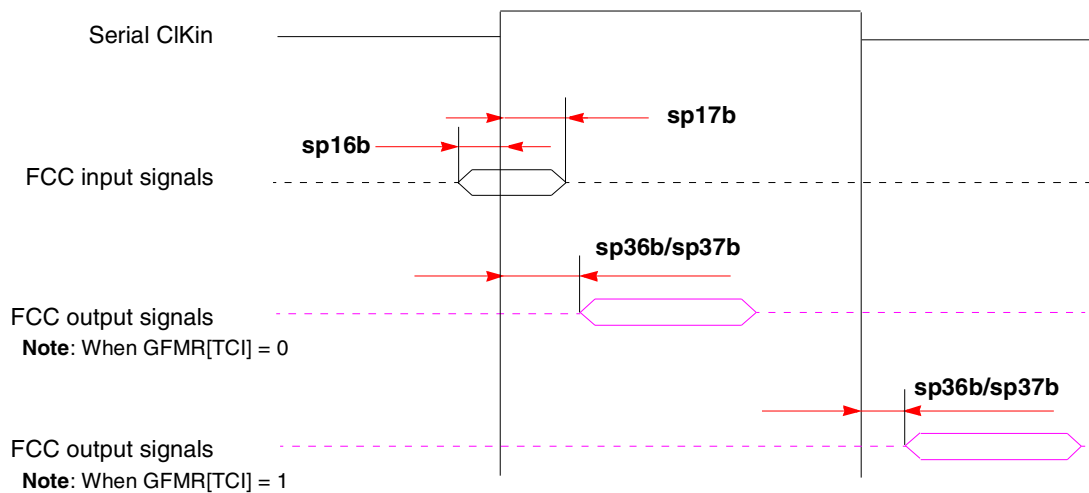


Figure 3. FCC External Clock Diagram

3 Clock Configuration Modes

To configure the main PLL multiplication factor and the core, CPM, and 60x bus frequencies, the MODCK[1–3] pins are sampled while $\overline{\text{HRESET}}$ is asserted. Table 13 lists the eight basic configuration modes. Table 14 lists the other modes that are available by using the configuration pin (RSTCONF) and driving four bits from hardware configuration word on the data bus.

Note that the MPC8265 and the MPC8266 have two additional clocking modes—PCI agent and PCI host. Refer to Section 3.2, “PCI Mode” on page 26 for information.

NOTE

Clock configurations change only after $\overline{\text{POR}}$ is asserted.

3.1 Local Bus Mode

Table 13 describes default clock modes for the MPC826xA.

Table 13. Clock Default Modes

MODCK[1–3]	Input Clock Frequency	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency
000	33 MHz	3	100 MHz	4	133 MHz
001	33 MHz	3	100 MHz	5	166 MHz
010	33 MHz	4	133 MHz	4	133 MHz
011	33 MHz	4	133 MHz	5	166 MHz
100	66 MHz	2	133 MHz	2.5	166 MHz
101	66 MHz	2	133 MHz	3	200 MHz
110	66 MHz	2.5	166 MHz	2.5	166 MHz
111	66 MHz	2.5	166 MHz	3	200 MHz

Table 14 describes all possible clock configurations when using the hard reset configuration sequence. Note that basic modes are shown in boldface type. The frequencies listed are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user’s device.

Table 14. Clock Configuration Modes¹

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3}	CPM Multiplication Factor ²	CPM Frequency ²	Core Multiplication Factor ²	Core Frequency ²
0001_000	33 MHz	2	66 MHz	4	133 MHz
0001_001	33 MHz	2	66 MHz	5	166 MHz
0001_010	33 MHz	2	66 MHz	6	200 MHz
0001_011	33 MHz	2	66 MHz	7	233 MHz
0001_100	33 MHz	2	66 MHz	8	266 MHz

Table 14. Clock Configuration Modes¹ (continued)

MODCK_H–MODCK[1–3]	Input Clock Frequency ^{2,3}	CPM Multiplication Factor ²	CPM Frequency ²	Core Multiplication Factor ²	Core Frequency ²
0100_111	Reserved				
0101_000					
0101_001					
0101_010					
0101_011					
0101_100					
0101_101	66 MHz	2	133 MHz	2	133 MHz
0101_110	66 MHz	2	133 MHz	2.5	166 MHz
0101_111	66 MHz	2	133 MHz	3	200 MHz
0110_000	66 MHz	2	133 MHz	3.5	233 MHz
0110_001	66 MHz	2	133 MHz	4	266 MHz
0110_010	66 MHz	2	133 MHz	4.5	300 MHz
0110_011	66 MHz	2.5	166 MHz	2	133 MHz
0110_100	66 MHz	2.5	166 MHz	2.5	166 MHz
0110_101	66 MHz	2.5	166 MHz	3	200 MHz
0110_110	66 MHz	2.5	166 MHz	3.5	233 MHz
0110_111	66 MHz	2.5	166 MHz	4	266 MHz
0111_000	66 MHz	2.5	166 MHz	4.5	300 MHz
0111_001	66 MHz	3	200 MHz	2	133 MHz
0111_010	66 MHz	3	200 MHz	2.5	166 MHz
0111_011	66 MHz	3	200 MHz	3	200 MHz
0111_100	66 MHz	3	200 MHz	3.5	233 MHz
0111_101	66 MHz	3	200 MHz	4	266 MHz
0111_110	66 MHz	3	200 MHz	4.5	300 MHz
0111_111	66 MHz	3.5	233 MHz	2	133 MHz
1000_000	66 MHz	3.5	233 MHz	2.5	166 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency¹ (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor²	PCI Frequency²
0011_011 ³	33 MHz	5	166 MHz	8	266 MHz	5	33 MHz
0100_000 ³	33 MHz	6	200 MHz	5	166 MHz	6	33 MHz
0100_001 ³	33 MHz	6	200 MHz	6	200 MHz	6	33 MHz
0100_010 ³	33 MHz	6	200 MHz	7	233 MHz	6	33 MHz
0100_011 ³	33 MHz	6	200 MHz	8	266 MHz	6	33 MHz
0101_000	66 MHz	2	133 MHz	2.5	166 MHz	2/4	66/33 MHz
0101_001	66 MHz	2	133 MHz	3	200 MHz	2/4	66/33 MHz
0101_010	66 MHz	2	133 MHz	3.5	233 MHz	2/4	66/33 MHz
0101_011	66 MHz	2	133 MHz	4	266 MHz	2/4	66/33 MHz
0101_100	66 MHz	2	133 MHz	4.5	300 MHz	2/4	66/33 MHz
0110_000	66 MHz	2.5	166 MHz	2.5	166 MHz	3/6	55/28 MHz
0110_001	66 MHz	2.5	166 MHz	3	200 MHz	3/6	55/28 MHz
0110_010	66 MHz	2.5	166 MHz	3.5	233 MHz	3/6	55/28 MHz
0110_011	66 MHz	2.5	166 MHz	4	266 MHz	3/6	55/28 MHz
0110_100	66 MHz	2.5	166 MHz	4.5	300 MHz	3/6	55/28 MHz
0111_000	66 MHz	3	200 MHz	2.5	166 MHz	3/6	66/33 MHz
0111_001	66 MHz	3	200 MHz	3	200 MHz	3/6	66/33 MHz
0111_010	66 MHz	3	200 MHz	3.5	233 MHz	3/6	66/33 MHz
0111_011	66 MHz	3	200 MHz	4	266 MHz	3/6	66/33 MHz
0111_100	66 MHz	3	200 MHz	4.5	300 MHz	3/6	66/33 MHz
1000_000	66 MHz	3	200 MHz	2.5	166 MHz	4/8	50/25 MHz
1000_001	66 MHz	3	200 MHz	3	200 MHz	4/8	50/25 MHz
1000_010	66 MHz	3	200 MHz	3.5	233 MHz	4/8	50/25 MHz
1000_011	66 MHz	3	200 MHz	4	266 MHz	4/8	50/25 MHz
1000_100	66 MHz	3	200 MHz	4.5	300 MHz	4/8	50/25 MHz
1001_000	66 MHz	3.5	233 MHz	2.5	166 MHz	4/8	58/29 MHz
1001_001	66 MHz	3.5	233 MHz	3	200 MHz	4/8	58/29 MHz

Table 17. Clock Configuration Modes in PCI Host Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency ¹ (Bus)	CPM Multiplication Factor	CPM Frequency	Core Multiplication Factor	Core Frequency	PCI Division Factor ²	PCI Frequency ²
1001_010	66 MHz	3.5	233 MHz	3.5	233 MHz	4/8	58/29 MHz
1001_011	66 MHz	3.5	233 MHz	4	266 MHz	4/8	58/29 MHz
1001_100	66 MHz	3.5	233 MHz	4.5	300 MHz	4/8	58/29 MHz
1010_000	100 MHz	2	200 MHz	2	200 MHz	3/6	66/33 MHz
1010_001	100 MHz	2	200 MHz	2.5	250 MHz	3/6	66/33 MHz
1010_010	100 MHz	2	200 MHz	3	300 MHz	3/6	66/33 MHz
1010_011	100 MHz	2	200 MHz	3.5	350 MHz	3/6	66/33 MHz
1010_100	100 MHz	2	200 MHz	4	400 MHz	3/6	66/33 MHz
1011_000	100 MHz	2.5	250 MHz	2	200 MHz	4/8	62/31 MHz
1011_001	100 MHz	2.5	250 MHz	2.5	250 MHz	4/8	62/31MHz
1011_010	100 MHz	2.5	250 MHz	3	300 MHz	4/8	62/31 MHz
1011_011	100 MHz	2.5	250 MHz	3.5	350 MHz	4/8	62/31 MHz
1011_100	100 MHz	2.5	250 MHz	4	400 MHz	4/8	62/31 MHz

¹ Input clock frequency is given only for the purpose of reference. User should set MODCK_H–MODCK_L so that the resulting configuration does not exceed the frequency rating of the user's part.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.). Refer to [Table 15](#).

³ In this mode, PCI_MODCK must be "0".

3.2.2 PCI Agent Mode

The frequencies listed in [Table 18](#) and [Table 19](#) are for the purpose of illustration only. Users must select a mode and input bus frequency so that the resulting configuration does not exceed the frequency rating of the user's device.

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000)

MODCK[1–3] ¹	Input Clock Frequency (PCI) ²	CPM Multiplication Factor ²	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
000	66/33 MHz	2/4	133 MHz	2.5	166 MHz	2	66 MHz
001	66/33 MHz	2/4	133 MHz	3	200 MHz	2	66 MHz
010	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 18. Clock Default Configurations in PCI Agent Mode (MODCK_HI = 0000) (continued)

MODCK[1-3] ¹	Input Clock Frequency (PCI) ²	CPM Multiplication Factor ²	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
100	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
101	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
110	66/33 MHz	4/8	266 MHz	3.5	300 MHz	3	88 MHz
111	66/33 MHz	4/8	266 MHz	3	300 MHz	2.5	100 MHz

¹ Assumes MODCK_HI = 0000.

² The frequency depends on the value of PCI_MODCK. If PCI_MODCK is high (logic '1'), the PCI frequency is divided by 2 (33 instead of 66 MHz, etc.) and the CPM multiplication factor is multiplied by 2. Refer to [Table 15](#).

³ Core frequency = (60x bus frequency)(core multiplication factor)

⁴ Bus frequency = CPM frequency/bus division factor

[Table 19](#) describes all possible clock configurations when using the MPC8265 or the MPC8266's internal PCI bridge in agent mode.

Table 19. Clock Configuration Modes in PCI Agent Mode

MODCK_H – MODCK[1-3]	Input Clock Frequency (PCI) ^{1,2}	CPM Multiplication Factor ¹	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
0001_001	66/33 MHz	2/4	133 MHz	5	166 MHz	4	33 MHz
0001_010	66/33 MHz	2/4	133 MHz	6	200 MHz	4	33 MHz
0001_011	66/33 MHz	2/4	133 MHz	7	233 MHz	4	33 MHz
0001_100	66/33 MHz	2/4	133 MHz	8	266 MHz	4	33 MHz
0010_001	50/25 MHz	3/6	150 MHz	3	180 MHz	2.5	60 MHz
0010_010	50/25 MHz	3/6	150 MHz	3.5	210 MHz	2.5	60 MHz
0010_011	50/25 MHz	3/6	150 MHz	4	240 MHz	2.5	60 MHz
0010_100	50/25 MHz	3/6	150 MHz	4.5	270 MHz	2.5	60 MHz
0011_000	66/33 MHz	2/4	133 MHz	2.5	110MHz	3	44 MHz
0011_001	66/33 MHz	2/4	133 MHz	3	132 MHz	3	44 MHz
0011_010	66/33 MHz	2/4	133 MHz	3.5	154 MHz	3	44 MHz
0011_011	66/33 MHz	2/4	133 MHz	4	176MHz	3	44 MHz
0011_100	66/33 MHz	2/4	133 MHz	4.5	198 MHz	3	44 MHz
0100_000	66/33 MHz	3/6	200 MHz	2.5	166 MHz	3	66 MHz
0100_001	66/33 MHz	3/6	200 MHz	3	200 MHz	3	66 MHz
0100_010	66/33 MHz	3/6	200 MHz	3.5	233 MHz	3	66 MHz
0100_011	66/33 MHz	3/6	200 MHz	4	266 MHz	3	66 MHz

Table 19. Clock Configuration Modes in PCI Agent Mode (continued)

MODCK_H – MODCK[1–3]	Input Clock Frequency (PCI) ^{1,2}	CPM Multiplication Factor ¹	CPM Frequency	Core Multiplication Factor	Core Frequency ³	Bus Division Factor	60x Bus Frequency ⁴
0100_100	66/33 MHz	3/6	200 MHz	4.5	300 MHz	3	66 MHz
0101_000 ⁵	33 MHz	5	166 MHz	2.5	166 MHz	2.5	66 MHz
0101_001 ⁵	33 MHz	5	166 MHz	3	200 MHz	2.5	66 MHz
0101_010 ⁵	33 MHz	5	166 MHz	3.5	233 MHz	2.5	66 MHz
0101_011 ⁵	33 MHz	5	166 MHz	4	266 MHz	2.5	66 MHz
0101_100 ⁵	33 MHz	5	166 MHz	4.5	300 MHz	2.5	66 MHz
0110_000	50/25 MHz	4/8	200 MHz	2.5	166 MHz	3	66 MHz
0110_001	50/25 MHz	4/8	200 MHz	3	200 MHz	3	66 MHz
0110_010	50/25 MHz	4/8	200 MHz	3.5	233 MHz	3	66 MHz
0110_011	50/25 MHz	4/8	200 MHz	4	266 MHz	3	66 MHz
0110_100	50/25 MHz	4/8	200 MHz	4.5	300 MHz	3	66 MHz
0111_000	66/33 MHz	3/6	200 MHz	2	200 MHz	2	100 MHz
0111_001	66/33 MHz	3/6	200 MHz	2.5	250 MHz	2	100 MHz
0111_010	66/33 MHz	3/6	200 MHz	3	300 MHz	2	100 MHz
0111_011	66/33 MHz	3/6	200 MHz	3.5	350 MHz	2	100 MHz
1000_000	66/33 MHz	3/6	200 MHz	2	160 MHz	2.5	80 MHz
1000_001	66/33 MHz	3/6	200 MHz	2.5	200 MHz	2.5	80 MHz
1000_010	66/33 MHz	3/6	200 MHz	3	240 MHz	2.5	80 MHz
1000_011	66/33 MHz	3/6	200 MHz	3.5	280 MHz	2.5	80 MHz
1000_100	66/33 MHz	3/6	200 MHz	4	320 MHz	2.5	80 MHz
1000_101	66/33 MHz	3/6	200 MHz	4.5	360 MHz	2.5	80 MHz
1001_000	66/33 MHz	4/8	266 MHz	2.5	166 MHz	4	66 MHz
1001_001	66/33 MHz	4/8	266 MHz	3	200 MHz	4	66 MHz
1001_010	66/33 MHz	4/8	266 MHz	3.5	233 MHz	4	66 MHz
1001_011	66/33 MHz	4/8	266 MHz	4	266 MHz	4	66 MHz
1001_100	66/33 MHz	4/8	266 MHz	4.5	300 MHz	4	66 MHz
1010_000	66/33 MHz	4/8	266 MHz	2.5	222 MHz	3	88 MHz

Figure 14 shows the side profile of the TBGA package to indicate the direction of the top surface view.

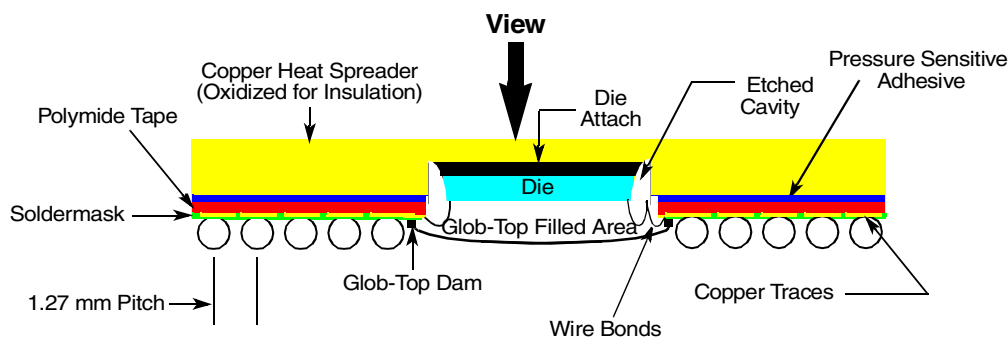


Figure 14. Side View of the TBGA Package

Table 21 shows the pinout list of the MPC826xA. Table 20 defines conventions and acronyms used in Table 21.

Symbols used in Table 21 are described in Table 20.

Table 20. Symbol Legend

Symbol	Meaning
OVERBAR	Signals with overbars, such as \overline{TA} , are active low.
UTM	Indicates that a signal is part of the UTOPIA master interface.
UTS	Indicates that a signal is part of the UTOPIA slave interface.
UT8	Indicates that a signal is part of the 8-bit UTOPIA interface.
UT16	Indicates that a signal is part of the 16-bit UTOPIA interface.
MII	Indicates that a signal is part of the media independent interface.

Table 21. Pinout List

Pin Name	Ball
BR	W5
BG	F4
ABB/IRQ2	E2
TS	E3
A0	G1
A1	H5
A2	H2
A3	H1
A4	J5
A5	J4
A6	J3
A7	J2

Table 21. Pinout List (continued)

Pin Name	Ball
ARTRY	E1
DBG	V1
DBB/IRQ3	V2
D0	B20
D1	A18
D2	A16
D3	A13
D4	E12
D5	D9
D6	A6
D7	B5
D8	A20
D9	E17
D10	B15
D11	B13
D12	A11
D13	E9
D14	B7
D15	B4
D16	D19
D17	D17
D18	D15
D19	C13
D20	B11
D21	A8
D22	A5
D23	C5
D24	C19
D25	C17
D26	C15
D27	D13
D28	C11
D29	B8
D30	A4
D31	E6

Table 21. Pinout List (continued)

Pin Name	Ball
D32	E18
D33	B17
D34	A15
D35	A12
D36	D11
D37	C8
D38	E7
D39	A3
D40	D18
D41	A17
D42	A14
D43	B12
D44	A10
D45	D8
D46	B6
D47	C4
D48	C18
D49	E16
D50	B14
D51	C12
D52	B10
D53	A7
D54	C6
D55	D5
D56	B18
D57	B16
D58	E14
D59	D12
D60	C10
D61	E8
D62	D6
D63	C2
DP0/RSRV/EXT_BR2	B22
IRQ1/DP1/EXT_BG2	A22
IRQ2/DP2/TLBISYNC/EXT_DBG2	E21

Table 21. Pinout List (continued)

Pin Name	Ball
PWE4/PSDDQM4/PBS4	B26
PWE5/PSDDQM5/PBS5	A26
PWE6/PSDDQM6/PBS6	B25
PWE7/PSDDQM7/PBS7	A25
PSDA10/PGPL0	E23
$\overline{\text{PSDWE}}$ /PGPL1	B24
$\overline{\text{POE}}$ / $\overline{\text{PSDRAS}}$ /PGPL2	A24
$\overline{\text{PSDCAS}}$ /PGPL3	B23
$\overline{\text{PGTA}}$ /PUPMWAIT/PGPL4/ $\overline{\text{PPBS}}$	A23
PSDAMUX/PGPL5	D22
LWE0/LSDDQM0/ $\overline{\text{LBS0}}$ /PCI_CFG0 ¹	H28
LWE1/LSDDQM1/ $\overline{\text{LBS1}}$ /PCI_CFG1 ¹	H27
LWE2/LSDDQM2/ $\overline{\text{LBS2}}$ /PCI_CFG2 ¹	H26
LWE3/LSDDQM3/ $\overline{\text{LBS3}}$ /PCI_CFG3 ¹	G29
LSDA10/LGPL0/PCI_MODCKH0 ¹	D27
$\overline{\text{LSDWE}}$ /LGPL1/PCI_MODCKH1 ¹	C28
$\overline{\text{LOE}}$ / $\overline{\text{LSDRAS}}$ /LGPL2/PCI_MODCKH2 ¹	E26
$\overline{\text{LSDCAS}}$ /LGPL3/PCI_MODCKH3 ¹	D25
$\overline{\text{LGT A}}$ /LUPMWAIT/LGPL4/ $\overline{\text{LPBS}}$	C26
LGPL5/LSDAMUX/PCI_MODCK ¹	B27
LWR	D28
L_A14/PAR ¹	N27
L_A15/ $\overline{\text{FRAME}}$ ¹ / $\overline{\text{SMI}}$	T29
L_A16/ $\overline{\text{TRDY}}$ ¹	R27
L_A17/ $\overline{\text{IRDY}}$ ¹ / $\overline{\text{CKSTP_OUT}}$	R26
L_A18/ $\overline{\text{STOP}}$ ¹	R29
L_A19/ $\overline{\text{DEVSEL}}$ ¹	R28
L_A20/ $\overline{\text{IDSEL}}$ ¹	W29
L_A21/ $\overline{\text{PERR}}$ ¹	P28
L_A22/ $\overline{\text{SERR}}$ ¹	N26
L_A23/ $\overline{\text{REQ0}}$ ¹	AA27
L_A24/ $\overline{\text{REQ1}}$ ¹ /HSEJSW ¹	P29
L_A25/ $\overline{\text{GNT0}}$ ¹	AA26
L_A26/ $\overline{\text{GNT1}}$ ¹ /HSLED ¹	N25
L_A27/ $\overline{\text{GNT2}}$ ¹ /HSENUM ¹	AA25

Table 21. Pinout List (continued)

Pin Name	Ball
L_A28/RST ¹ /CORE_SRESET	AB29
L_A29/INTA ¹	AB28
L_A30/REQ2 ¹	P25
L_A31/DLLOUT ¹	AB27
LCL_D0/AD0 ¹	H29
LCL_D1/AD1 ¹	J29
LCL_D2/AD2 ¹	J28
LCL_D3/AD3 ¹	J27
LCL_D4/AD4 ¹	J26
LCL_D5/AD5 ¹	J25
LCL_D6/AD6 ¹	K25
LCL_D7/AD7 ¹	L29
LCL_D8/AD8 ¹	L27
LCL_D9/AD9 ¹	L26
LCL_D10/AD10 ¹	L25
LCL_D11/AD11 ¹	M29
LCL_D12/AD12 ¹	M28
LCL_D13/AD13 ¹	M27
LCL_D14/AD14 ¹	M26
LCL_D15/AD15 ¹	N29
LCL_D16/AD16 ¹	T25
LCL_D17/AD17 ¹	U27
LCL_D18/AD18 ¹	U26
LCL_D19/AD19 ¹	U25
LCL_D20/AD20 ¹	V29
LCL_D21/AD21 ¹	V28
LCL_D22/AD22 ¹	V27
LCL_D23/AD23 ¹	V26
LCL_D24/AD24 ¹	W27
LCL_D25/AD25 ¹	W26
LCL_D26/AD26 ¹	W25
LCL_D27/AD27 ¹	Y29
LCL_D28/AD28 ¹	Y28
LCL_D29/AD29 ¹	Y25
LCL_D30/AD30 ¹	AA29

Table 21. Pinout List (continued)

Pin Name	Ball
PA12/FCC1_UT8_RXD2/FCC1_UT16_RXD10/MSNUM3	AJ21 ²
PA13/FCC1_UT8_RXD3/FCC1_UT16_RXD11/MSNUM2	AH20 ²
PA14/FCC1_UT8_RXD4/FCC1_UT16_RXD12/FCC1_RXD3	AG19 ²
PA15/FCC1_UT8_RXD5/FCC1_UT16_RXD13/FCC1_RXD2	AF18 ²
PA16/FCC1_UT8_RXD6/FCC1_UT16_RXD14/FCC1_RXD1	AF17 ²
PA17/FCC1_UT8_RXD7/FCC1_UT16_RXD15/FCC1_RXD0/FCC1_RXD	AE16 ²
PA18/FCC1_UT8_TXD7/FCC1_UT16_TXD15/FCC1_TXD0/FCC1_TXD	AJ16 ²
PA19/FCC1_UT8_TXD6/FCC1_UT16_TXD14/FCC1_TXD1	AG15 ²
PA20/FCC1_UT8_TXD5/FCC1_UT16_TXD13/FCC1_TXD2	AJ13 ²
PA21/FCC1_UT8_TXD4/FCC1_UT16_TXD12/FCC1_TXD3	AE13 ²
PA22/FCC1_UT8_TXD3/FCC1_UT16_TXD11	AF12 ²
PA23/FCC1_UT8_TXD2/FCC1_UT16_TXD10	AG11 ²
PA24/FCC1_UT8_TXD1/FCC1_UT16_TXD9/MSNUM1	AH9 ²
PA25/FCC1_UT8_TXD0/FCC1_UT16_TXD8/MSNUM0	AJ8 ²
PA26/FCC1_UTM_RXCLAV/FCC1_UTS_RXCLAV/FCC1_MII_RX_ER	AH7 ²
PA27/FCC1_UT_RXSOC/FCC1_MII_RX_DV	AF7 ²
PA28/FCC1_UTM_RXENB/FCC1_UTS_RXENB/FCC1_MII_TX_EN	AD5 ²
PA29/FCC1_UT_TXSOC/FCC1_MII_TX_ER	AF1 ²
PA30/FCC1_UTM_TXCLAV/FCC1_UTS_TXCLAV/FCC1_MII_CRS/ FCC1_RTS	AD3 ²
PA31/FCC1_UTM_TXENB/FCC1_UTS_TXENB/FCC1_MII_COL	AB5 ²
PB4/FCC3_TXD3/FCC2_UT8_RXD0/L1RSYNCA2/FCC3_RTS	AD28 ²
PB5/FCC3_TXD2/FCC2_UT8_RXD1/L1TSYNCA2/L1GNTA2	AD26 ²
PB6/FCC3_TXD1/FCC2_UT8_RXD2/L1RXDA2/L1RXD0A2	AD25 ²
PB7/FCC3_TXD0/FCC3_TXD/FCC2_UT8_RXD3/L1TXDA2/L1TXD0A2	AE26 ²
PB8/FCC2_UT8_TXD3/FCC3_RXD0/FCC3_RXD/TXD3/L1RSYNCD1	AH27 ²
PB9/FCC2_UT8_TXD2/FCC3_RXD1/L1TXD2A2/L1TSYNCD1/L1GNTD1	AG24 ²
PB10/FCC2_UT8_TXD1/FCC3_RXD2/L1RXDD1	AH24 ²
PB11/FCC3_RXD3/FCC2_UT8_TXD0/L1TXDD1	AJ24 ²
PB12/FCC3_MII_CRS/L1CLKOB1/L1RSYNCC1/TXD2	AG22 ²
PB13/FCC3_MII_COL/L1RQB1/L1TSYNCC1/L1GNTC1/L1TXD1A2	AH21 ²
PB14/FCC3_MII_TX_EN/RXD3/L1RXDC1	AG20 ²
PB15/FCC3_MII_TX_ER/RXD2/L1TXDC1	AF19 ²
PB16/FCC3_MII_RX_ER/L1CLKOA1/CLK18	AJ18 ²
PB17/FCC3_MII_RX_DV/L1RQA1/CLK17	AJ17 ²

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