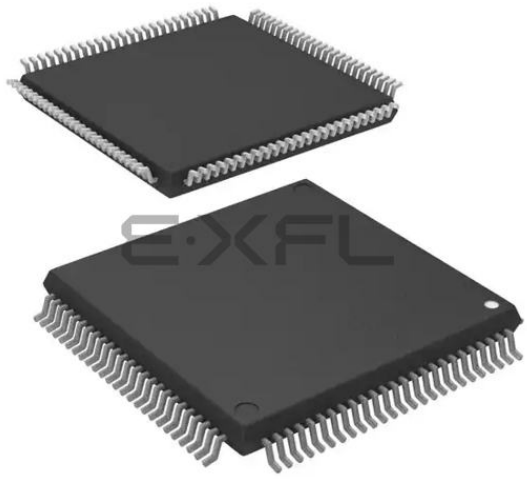
Renesas Electronics America Inc - UPD70F3738GC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	84
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3738gc-ueu-ax

(8/11)

Address	Function Register Name	Symbol	R/W	Manipulatable Bits			Default Value
				1	8	16	
FFFFF712H	Port 9 function control expansion register	PFCE9	R/W			√	0000H
FFFFF712H	Port 9 function control expansion register L	PFCE9L		√	√		00H
FFFFF713H	Port 9 function control expansion register H	PFCE9H		√	√		00H
FFFFF802H	System status register	SYS		√	√		00H
FFFFF80CH	Internal oscillation mode register	RCM		√	√		00H
FFFFF810H	DMA trigger factor register 0	DTFR0		√	√		00H
FFFFF812H	DMA trigger factor register 1	DTFR1		√	√		00H
FFFFF814H	DMA trigger factor register 2	DTFR2		√	√		00H
FFFFF816H	DMA trigger factor register 3	DTFR3		√	√		00H
FFFFF820H	Power save mode register	PSMR		√	√		00H
FFFFF822H	Clock control register	CKC		√	√		0AH
FFFFF824H	Lock register	LOCKR	R	√	√		00H
FFFFF828H	Processor clock control register	PCC[Note]	R/W	√	√		03H
FFFFF82CH	PLL control register	PLLCTL		√	√		01H
FFFFF82EH	CPU operation clock status register	CCLS	R	√	√		00H
FFFFF870H	Clock monitor mode register	CLM	R/W	√	√		00H
FFFFF888H	Reset source flag register	RESF		√	√		00H
FFFFF890H	Low-voltage detection register	LVIM		√	√		00H
FFFFF891H	Low-voltage detection level select register	LVIS			√		00H
FFFFF8B0H	Prescaler mode register 0	PRSM0		√	√		00H
FFFFF8B1H	Prescaler compare register 0	PRSCM0			√		00H
FFFFF9FCH	On-chip debug mode register	OCDM[Note]		√	√		01H
FFFFFA00H	UARTA0 control register 0	UA0CTL0		√	√		10H
FFFFFA01H	UARTA0 control register 1	UA0CTL1			√		00H
FFFFFA02H	UARTA0 control register 2	UA0CTL2			√		FFH
FFFFFA03H	UARTA0 option control register 0	UA0OPT0		√	√		14H
FFFFFA04H	UARTA0 status register	UA0STR		√	√		00H
FFFFFA06H	UARTA0 receive data register	UA0RX	R		√		FFH
FFFFFA07H	UARTA0 transmit data register	UA0TX	R/W		√		FFH
FFFFFA10H	UARTA1 control register 0	UA1CTL0		√	√		10H
FFFFFA11H	UARTA1 control register 1	UA1CTL1			√		00H
FFFFFA12H	UARTA1 control register 2	UA1CTL2			√		FFH
FFFFFA13H	UARTA1 option control register 0	UA1OPT0		√	√		14H
FFFFFA14H	UARTA1 status register	UA1STR		√	√		00H
FFFFFA16H	UARTA1 receive data register	UA1RX	R		√		FFH
FFFFFA17H	UARTA1 transmit data register	UA1TX	R/W		√		FFH
FFFFFA20H	UARTA2 control register 0	UA2CTL0		√	√		10H
FFFFFA21H	UARTA2 control register 1	UA2CTL1			√		00H
FFFFFA22H	UARTA2 control register 2	UA2CTL2			√		FFH
FFFFFA23H	UARTA2 option control register 0	UA2OPT0		√	√		14H
FFFFFA24H	UARTA2 status register	UA2STR		√	√		00H
FFFFFA26H	UARTA2 receive data register	UA2RX	R		√		FFH
FFFFFA27H	UARTA2 transmit data register	UA2TX	R/W		√		FFH

Note This is a special register.

(2) Port 0 mode register (PM0)

After reset: FFH R/W Address: FFFFF420H

	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	1	1

PM0n	I/O mode control (n = 2 to 6)
0	Output mode
1	Input mode

<R> **(3) Port 0 mode control register (PMC0)**

After reset: 00H R/W Address: FFFFF440H

	7	6	5	4	3	2	1	0
PMC0	0	PMC06	PMC05	PMC04	PMC03	PMC02	0	0

PMC06	Specification of pin operation
0	I/O port (p06)
1	INTP3 input

PMC05	Specification of pin operation
0	I/O port (p05)
1	INTP2 input

PMC04	Specification of pin operation
0	I/O port (p04)
1	INTP1 input (/RTCDIV output/RTCCL output)Note

PMC03	Specification of pin operation
0	I/O port (p03)
1	INTP0 input/ADTRG input (/RTC1HZ output)Note

PMC02	Specification of pin operation
0	I/O port (p02)
1	NMI input (/A21 output)Note

Note μPD70F3792, 70F3793 only.

Caution The P05/INTP2/$\overline{\text{DRST}}$ pin becomes the $\overline{\text{DRST}}$ pin regardless of the value of the PMC05 bit when the OCDM.OCDM0 bit is 1.

4.3.6 Port 7

Port 7 is a 12-bit port for which I/O settings can be controlled in 1-bit units.

Port 7 includes the following alternate-function pins.

Table 4-9. Port 7 Alternate-Function Pins

Pin No.			Function Name	Alternate Function		Remark	Block Type
GF	GC	F1		Name	I/O		
2	100	A3	P70	ANI0	Input	–	A-1
1	99	B3	P71	ANI1	Input		A-1
100	98	C3	P72	ANI2	Input		A-1
99	97	D3	P73	ANI3	Input		A-1
98	96	A4	P74	ANI4	Input		A-1
97	95	B4	P77	ANI5	Input		A-1
96	94	C4	P76	ANI6	Input		A-1
95	93	D4	P77	ANI7	Input		A-1
94	92	A5	P78	ANI8	Input		A-1
93	91	B5	P79	ANI9	Input		A-1
92	90	C5	P710	ANI10	Input		A-1
91	89	D5	P711	ANI11	Input		A-1

Remark GF: 100-pin plastic LQFP (14 × 20) (μPD70F3737, 70F3738 only)
GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
F1: 121-pin plastic FBGA (8 × 8)

(7) Port 9 function register (PF9)

After reset: 0000H R/W Address: PF9 FFFFFC72H,
PF9L FFFFFC72H, PF9H FFFFFC73H

	15	14	13	12	11	10	9	8
PF9 (PF9H)	PF915	PF914	PF913	PF912	PF911	PF910	PF99	PF98

	7	6	5	4	3	2	1	0
(PF9L)	PF97	PF96	PF95	PF94	PF93	PF92	PF91	PF90

PF9n	Specification of normal output (CMOS output) or N-ch open-drain output (n = 0 to 15)
0	Normal output (CMOS output)
1	N-ch open-drain output

Caution When output pins P90 to P96 are pulled up to EV_{DD} or higher, be sure to set the PF9n bit to 1.

Pull up output pins P97 to P915 to the same potential as EV_{DD}, even when they are used as N-ch open-drain output pins.

Remarks 1. The PF9 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PF9 register as the PF9H register and the lower 8 bits as the PF9L register, PF9 can be read or written in 8-bit or 1-bit units.

2. To read/write bits 8 to 15 of the PF9 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PF9H register.

5.6 Wait Function

5.6.1 Programmable wait function

(1) Data wait control register 0 (DWC0)

To realize interfacing with a low-speed memory or I/O device, up to seven data wait states can be inserted in the bus cycle that is executed for each memory block space.

The number of wait states can be programmed by using the DWC0 register. Immediately after system reset, 7 data wait states are inserted for all the memory block areas.

The DWC0 register can be read or written in 16-bit units.

Reset sets this register to 7777H.

Cautions 1. The internal ROM and internal RAM areas are not subject to programmable wait, and are always accessed without a wait state. The on-chip peripheral I/O area is also not subject to programmable wait, and only wait control from each peripheral function is performed.

2. Write to the DWC0 register after reset, and then do not change the set values. Also, when changing the initial values of the DWC0 register, do not access an external memory area until the settings are complete.

After reset: 7777H R/W Address: FFFFF484H

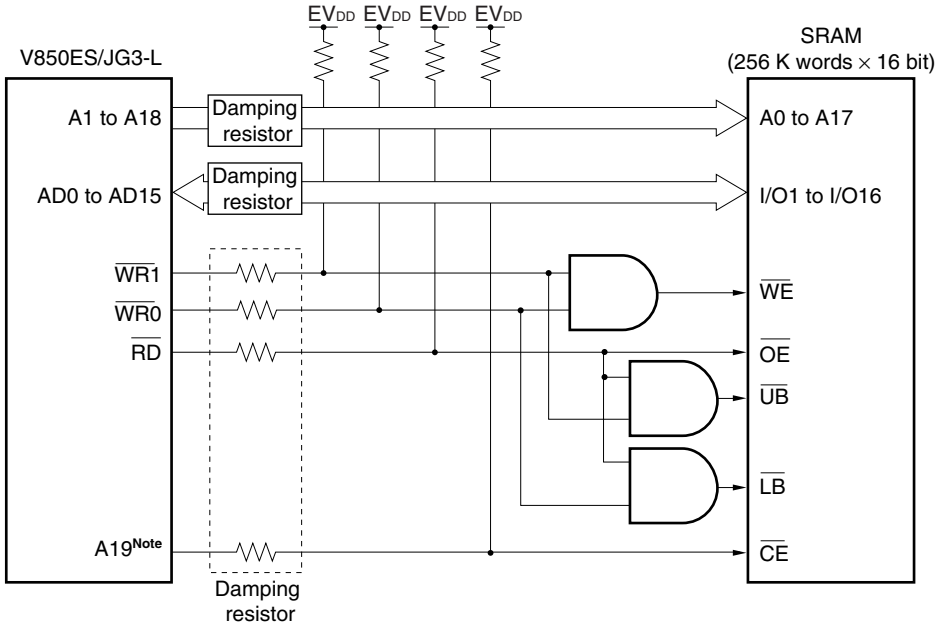
	15	14	13	12	11	10	9	8
DWC0	0	DW32	DW31	DW30	0	DW22	DW21	DW20
Memory block n signal		Memory block 3				Memory block 2		

	7	6	5	4	3	2	1	0
	0	DW12	DW11	DW10	0	DW02	DW01	DW00
Memory block n signal		Memory block 1				Memory block 0		

DWn2	DWn1	DWn0	Number of wait states inserted in memory block n space (n = 0 to 3)
0	0	0	None
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Caution Be sure to clear bits 15, 11, 7, and 3 to "0".

<R> **Figure 5-18. Connecting SRAM with 16-bit Data Bus to V850ES/JG3-L via 16-bit Bus**

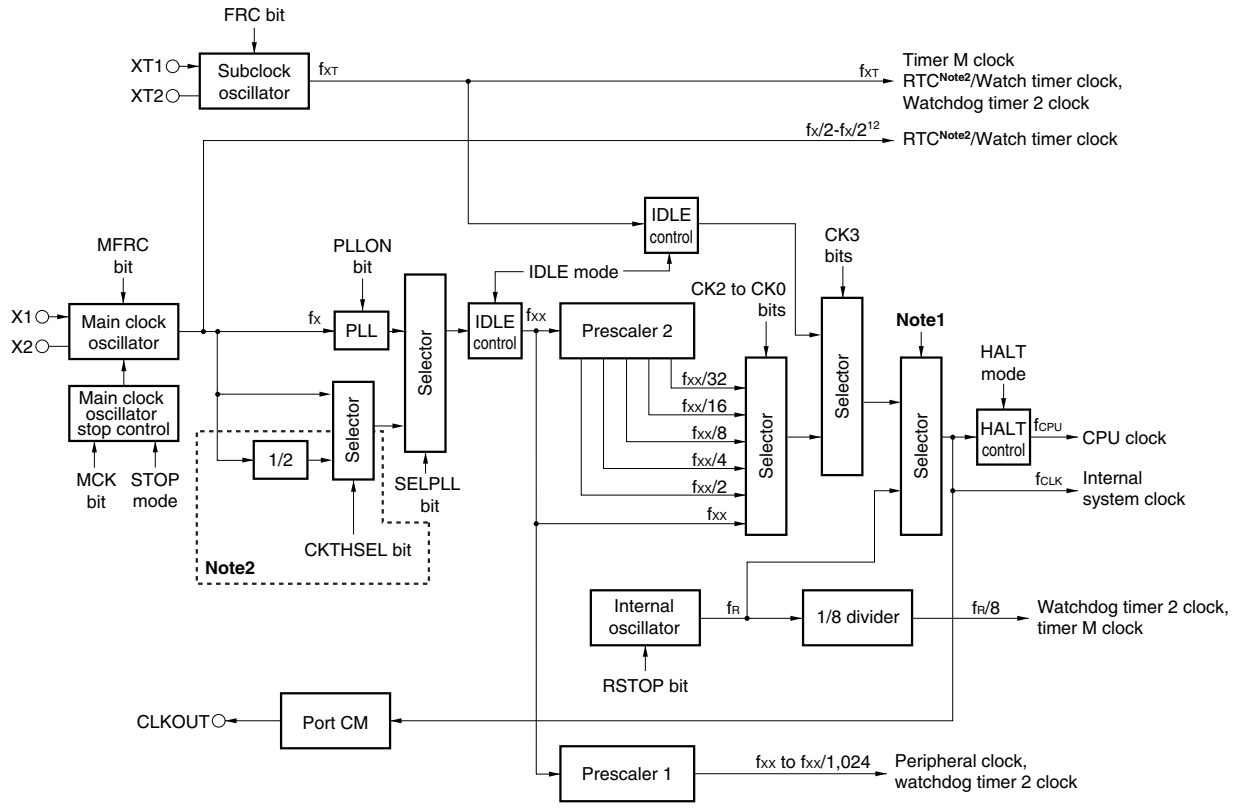


Note Generate the chip select signal using the higher address.

6.2 Configuration

<R>

Figure 6-1. Clock Generator



Notes1. The internal oscillator clock is selected when watchdog timer 2 overflows during the oscillation stabilization time.

2. The feature shown in the dotted line is only available in the μPD70F3792 and 70F3793.

Remark f_X: Main clock oscillation frequency
f_{XX}: Main clock frequency
f_{CLK}: Internal system clock frequency
f_{XT}: Subclock frequency
f_{CPU}: CPU clock frequency
f_R: Internal oscillator clock frequency

7.4 Operations

TMPn can execute the following operations:

Table 7-5. TMPn Operating Modes

Operating Mode	TPnCTL1.TPnEST Bit (Software Trigger Bit)	TIPn0 Pin (External Trigger Input)	Capture/Compare Register Setting	Compare Register Write	Count Clock
Interval timer mode	Invalid	Invalid	Compare only	Anytime write	Internal/external
External event count mode[Note 1]	Invalid	Invalid	Compare only	Anytime write	External
External trigger pulse output mode[Note 2]	Valid	Valid	Compare only	Batch write	Internal
One-shot pulse output mode[Note 2]	Valid	Valid	Compare only	Anytime write	Internal
PWM output mode	Invalid	Invalid	Compare only	Batch write	Internal/external
Free-running timer mode	Invalid	Invalid	Can be switched	Anytime write	Internal/external
Pulse width measurement mode[Note 2]	Invalid	Invalid	Capture only	Not applicable	Internal

Notes 1. When using the external event count mode, specify that the valid edge of the TIPn0 pin capture trigger input is not detected (by clearing the TPnIOC1.TPnIS1 and TPnIOC1.TPnIS0 bits to 0).

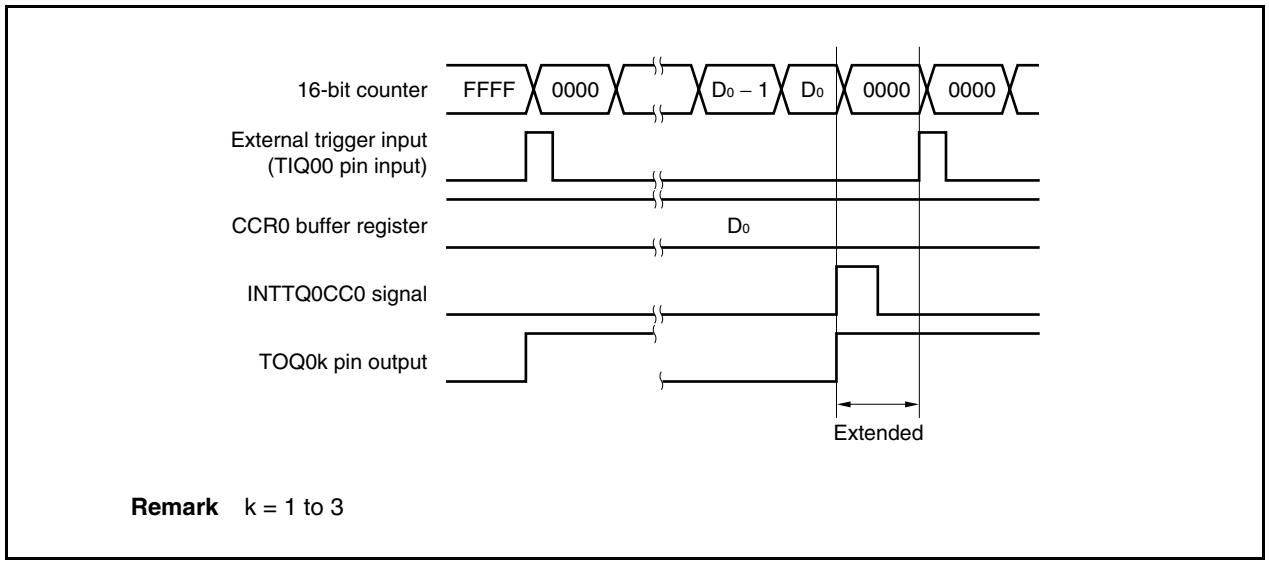
2. When using the external trigger pulse output mode, one-shot pulse output mode, and pulse width measurement mode, select the internal clock as the count clock (by clearing the TPnCTL1.TPnEEE bit to 0).

Remark n = 0 to 5

(d) Detection of trigger immediately before or after INTTQ0CC0 generation

If the trigger is detected immediately after the INTTQ0CC0 signal is generated, the 16-bit counter is cleared to 0000H and continues incrementing. Therefore, the active period of the TOQ0k pin is extended by the amount of time between the generation of the INTTQ0CC0 signal and the detection of the trigger.

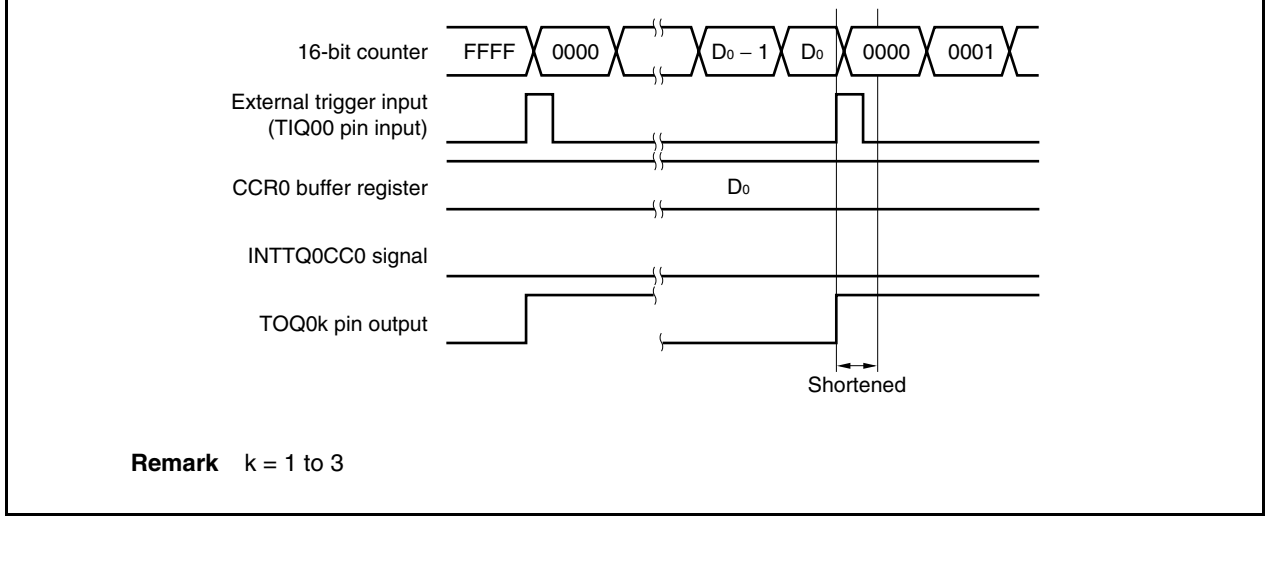
Figure 8-35. Detection of Trigger Immediately After INTTQ0CC0 Signal Was Generated



Remark k = 1 to 3

If the trigger is detected immediately before the INTTQ0CC0 signal is generated, the INTTQ0CC0 signal is not generated. The 16-bit counter is cleared to 0000H, the TOQ0k pin output is set to the active level, and the counter continues incrementing. Consequently, the inactive period of the PWM waveform is shortened.

Figure 8-36. Detection of Trigger Immediately Before INTTQ0CC0 Signal Is Generated



Remark k = 1 to 3

Figure 8-46. Register Settings in PWM Output Mode (3/3)

(f) TMQ0 capture/compare registers 0 to 3 (TQ0CCR0 to TQ0CCR3)

If the TQ0CCR0 register is set to D_0 and the TQ0CCRk register is set to D_k, the PWM waveform is as follows:

PWM waveform cycle = $(D_0 + 1) \times$ Count clock cycle

PWM waveform active level width = $D_k \times$ Count clock cycle

Remarks 1. TMQ0 I/O control register 1 (TQ0IOC1) and TMQ0 option register 0 (TQ0OPT0) are not used in the PWM output mode.

2. Updating TMQ0 capture/compare register 2 (TQ0CCR2) and TMQ0 capture/compare register 3 (TQ0CCR3) is enabled by writing to TMQ0 capture/compare register 1 (TQ0CCR1).

(2/2)

UC0SLS2	UC0SLS1	UC0SLS0	SBF transmit length selection
1	0	1	13-bit output (initial value)
1	1	0	14-bit output
1	1	1	15-bit output
0	0	0	16-bit output
0	0	1	17-bit output
0	1	0	18-bit output
0	1	1	19-bit output
1	0	0	20-bit output
This register can be set when the UC0PWR bit or the UC0TXE bit is 0.			

UC0TDL	Transmit data level bit
0	Normal output of transfer data
1	Inverted output of transfer data
• The output level of the TXDC0 pin can be inverted by using the UC0TDL bit. • This register can be set when the UC0PWR bit or the UC0TXE bit is 0.	

UC0RDL	Receive data level bit
0	Normal input of transfer data
1	Inverted input of transfer data
• The input level of the RXDC0 pin can be inverted by using the UC0RDL bit. • This register can be set when the UC0PWR bit or the UC0RXE bit is 0.	

Table 19-2. Clock Settings (1/2)

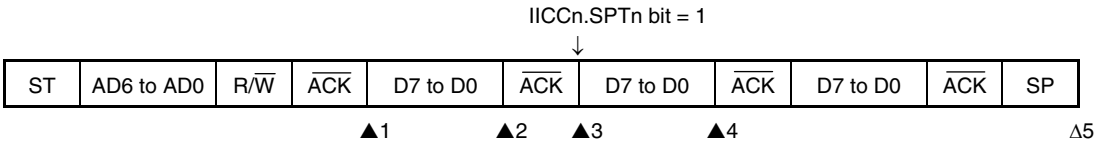
IICX0	IICCL0			Selection Clock	Transfer Clock	Settable Main Clock Frequency (f_{XX}) Range	Operating Mode
Bit 0	Bit 3	Bit 1	Bit 0				
CLX0	SMC0	CL01	CL00				
0	0	0	0	f_{XX} (when OCKS0 = 18H set)	$f_{XX}/44$	2.50 MHz ≤ f_{XX} ≤ 4.19 MHz	Standard mode (SMC0 bit = 0)
				$f_{XX}/2$ (when OCKS0 = 10H set)	$f_{XX}/88$	4.00 MHz ≤ f_{XX} ≤ 8.38 MHz	
				$f_{XX}/3$ (when OCKS0 = 11H set)	$f_{XX}/132$	6.00 MHz ≤ f_{XX} ≤ 12.57 MHz	
				$f_{XX}/4$ (when OCKS0 = 12H set)	$f_{XX}/176$	8.00 MHz ≤ f_{XX} ≤ 16.76 MHz	
				$f_{XX}/5$ (when OCKS0 = 13H set)	$f_{XX}/220$	10.00 MHz ≤ f_{XX} ≤ 20.00 MHz	
0	0	0	1	f_{XX} (when OCKS0 = 18H set)	$f_{XX}/86$	4.19 MHz ≤ f_{XX} ≤ 8.38 MHz	
				$f_{XX}/2$ (when OCKS0 = 10H set)	$f_{XX}/172$	8.38 MHz ≤ f_{XX} ≤ 16.76 MHz	
				$f_{XX}/3$ (when OCKS0 = 11H set)	$f_{XX}/258$	12.57 MHz ≤ f_{XX} ≤ 20.00 MHz	
				$f_{XX}/4$ (when OCKS0 = 12H set)	$f_{XX}/344$	16.76 MHz ≤ f_{XX} ≤ 20.00 MHz	
0	0	1	0	f_{XX} Note	$f_{XX}/86$	4.19 MHz ≤ f_{XX} ≤ 8.38 MHz	
0	0	1	1	f_{XX} (when OCKS0 = 18H set)	$f_{XX}/66$	f_{XX} = 6.40 MHz	
				$f_{XX}/2$ (when OCKS0 = 10H set)	$f_{XX}/132$	f_{XX} = 12.80 MHz	
				$f_{XX}/3$ (when OCKS0 = 11H set)	$f_{XX}/198$	f_{XX} = 19.20 MHz	
0	1	0	×	f_{XX} (when OCKS0 = 18H set)	$f_{XX}/24$	4.19 MHz ≤ f_{XX} ≤ 8.38 MHz	High-speed mode (SMC0 bit = 1)
				$f_{XX}/2$ (when OCKS0 = 10H set)	$f_{XX}/48$	8.00 MHz ≤ f_{XX} ≤ 16.76 MHz	
				$f_{XX}/3$ (when OCKS0 = 11H set)	$f_{XX}/72$	12.00 MHz ≤ f_{XX} ≤ 20.00 MHz	
				$f_{XX}/4$ (when OCKS0 = 12H set)	$f_{XX}/96$	16.00 MHz ≤ f_{XX} ≤ 20.00 MHz	
0	1	1	0	f_{XX} Note	$f_{XX}/24$	4.00 MHz ≤ f_{XX} ≤ 8.38 MHz	
0	1	1	1	f_{XX} (when OCKS0 = 18H set)	$f_{XX}/18$	f_{XX} = 6.40 MHz	
				$f_{XX}/2$ (when OCKS0 = 10H set)	$f_{XX}/36$	f_{XX} = 12.80 MHz	
				$f_{XX}/3$ (when OCKS0 = 11H set)	$f_{XX}/54$	f_{XX} = 19.20 MHz	
1	1	0	×	f_{XX} (when OCKS0 = 18H set)	$f_{XX}/12$	4.00 MHz ≤ f_{XX} ≤ 4.19 MHz	
				$f_{XX}/2$ (when OCKS0 = 10H set)	$f_{XX}/24$	8.00 MHz ≤ f_{XX} ≤ 8.38 MHz	
				$f_{XX}/3$ (when OCKS0 = 11H set)	$f_{XX}/36$	12.00 MHz ≤ f_{XX} ≤ 12.57 MHz	
				$f_{XX}/4$ (when OCKS0 = 12H set)	$f_{XX}/48$	16.00 MHz ≤ f_{XX} ≤ 16.67 MHz	
				$f_{XX}/5$ (when OCKS0 = 13H set)	$f_{XX}/60$	f_{XX} = 20.00 MHz	
1	1	1	0	f_{XX} Note	$f_{XX}/12$	4.00 MHz ≤ f_{XX} ≤ 4.19 MHz	
Other than above				Setting prohibited	–	–	–

Note Since the selection clock is f_{XX} regardless of the value set to the OCKS0 register, clear the OCKS0 register to 00H (I^2C division clock stopped status).

Remark ×: don't care

(8) When arbitration loss occurs due to low level of SDA0n pin when attempting to generate a stop condition

<1> When WTIMn bit = 0



▲1: IICSn register = 1000X110B

▲2: IICSn register = 1000X000B (WTIMn bit = 1)

▲3: IICSn register = 1000XX00B (WTIMn bit = 0)

▲4: IICSn register = 01000000B (Example: When ALDn bit is read during interrupt servicing)

Δ 5: IICSn register = 00000001B

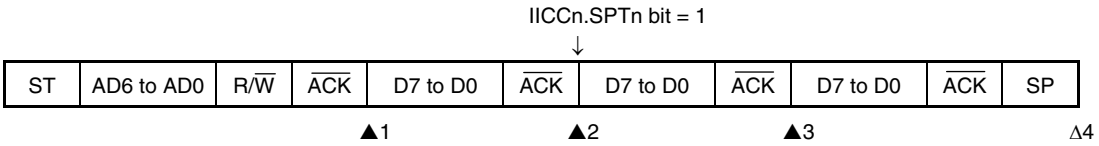
Remarks 1. ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

2. n = 0 to 2

<2> When WTIMn bit = 1



▲1: IICSn register = 1000X110B

▲2: IICSn register = 1000XX00B

▲3: IICSn register = 01000000B (Example: When ALDn bit is read during interrupt servicing)

Δ 4: IICSn register = 00000001B

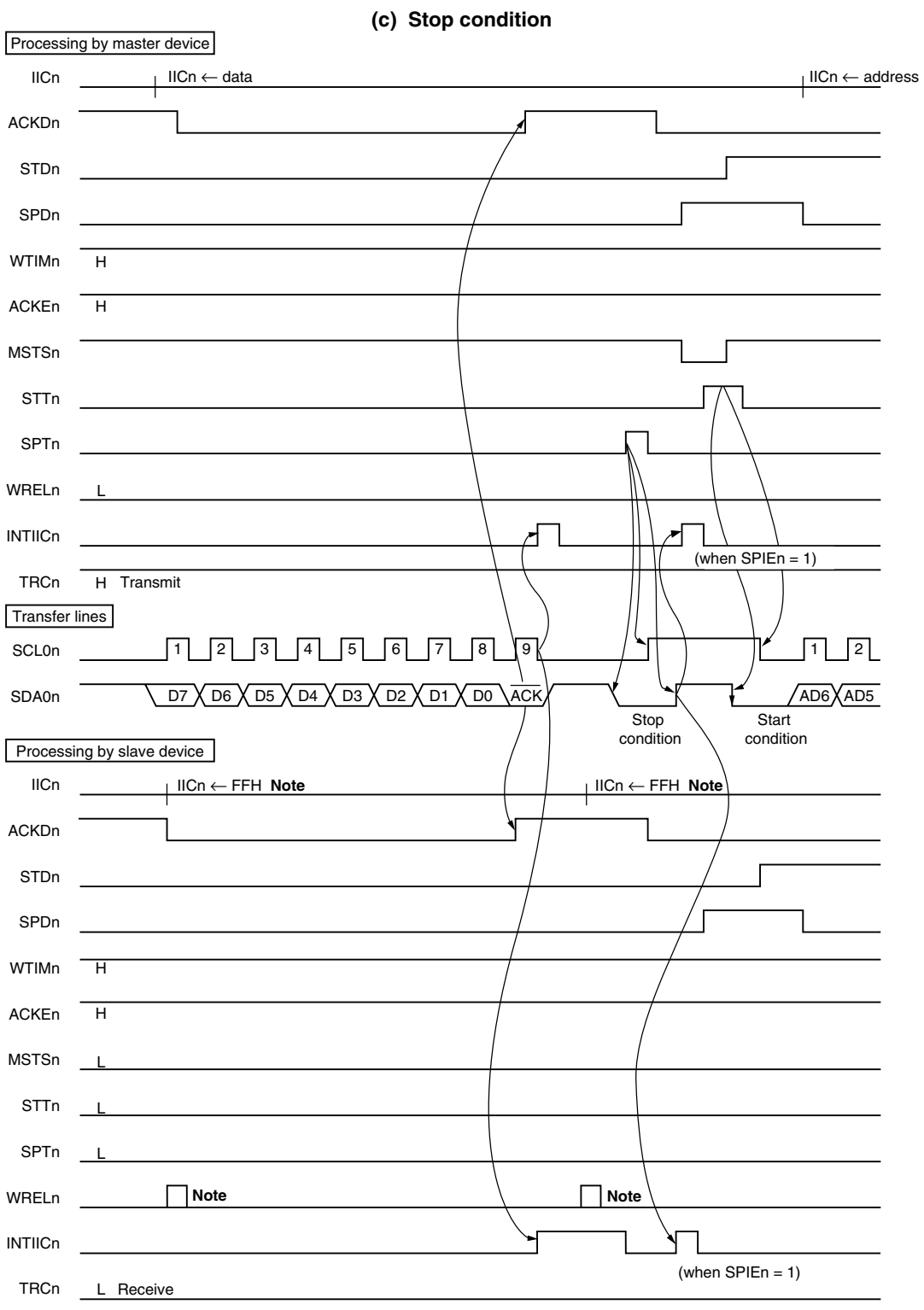
Remarks 1. ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

2. n = 0 to 2

Figure 19-23. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)



Note To cancel slave wait, write FFH to IICn or set WRELn.

Remark n = 0 to 2

22.4 Cautions

(1) If a low level is input to any of the KR0 to KR7 pins, the INTKR signal is not generated even if the falling edge is input to another pin.

(2) The RXDA1 and KR7 pins must not be used at the same time. When using the RXDA1 pin, do not use the KR7 pin. When using the KR7 pin, do not use the RXDA1 pin (it is recommended to set the PFC91 bit to 1 and clear PFCE91 bit to 0).

(3) If the KRM register is changed, an interrupt request signal (INTKR) may be generated. To prevent this, change the KRM register after disabling (DI) or masking interrupts, then clear the interrupt request flag (KRIC.KRIF bit) to 0, and enable (EI) or unmask interrupts.

(4) To use the key interrupt function, be sure to set the function of the port pin to “key return pin” and then enable the key interrupt function by using the KRM register. To switch the pin function from key return pin to port pin, disable the key interrupt function by using the KRM register and then set pin function to “port pin”.

<R>

Table 23-7. Operating Status in IDLE2 Mode

Setting of IDLE2 Mode / Item		Operating Status	
		When Subclock Is Not Used	When Subclock Is Used
LVI		Operable	
Main clock oscillator		Oscillates	
Subclock oscillator		–	Oscillates
Internal oscillator		Oscillation enabled	
PLL		Stops operation	
CPU		Stops operation	
DMA		Stops operation	
Interrupt controller		Stops operation (but standby mode release is possible)	
Timer P (TMP0 to TMP5)		Stops operation	
Timer Q (TMQ0)		Stops operation	
Timer M (TMM0)		Operable when f_R/8 is selected as the count clock	Operable when f_R/8 or f_{XT} is selected as the count clock
Watch timer(/RTC) Note1		Operable when f_X (divided BRG) is selected as the count clock	Operable
Watchdog timer 2		Operable when f_R/8 is selected as the count clock	Operable when f_R/8 or f_{XT} is selected as the count clock
Serial interface	CSIB0 to CSIB4	Operable when the $\overline{\text{SCKBn}}$ input clock is selected as the count clock (n = 0 to 4)	
	I^2C00 to I^2C02	Stops operation	
	UARTA0 to UARTA5	Stops operation (but UARTA0 is operable when the ASCKA0 input clock is selected)	
	UARTC0 Note1	Stops operation	
A/D converter		Holds operation (conversion result held) Note2	
D/A converter		Holds operation (output held Note2)	
Real-time output function (RTO)		Stops operation (output held)	
Key interrupt function (KR)		Operable	
CRC operation circuit		Stops operation	
External bus interface		See **2.2 Pin States**.	
Port function		Retains status before IDLE2 mode was set	
CPU register set		Retains status before IDLE2 mode was set	
Internal RAM			

Notes1. μPD70F3792, 70F3793 only

2. To realize low power consumption, stop the A/D and D/A converters before shifting to the IDLE2 mode.

31.3 ROM Security Function

31.3.1 Security ID

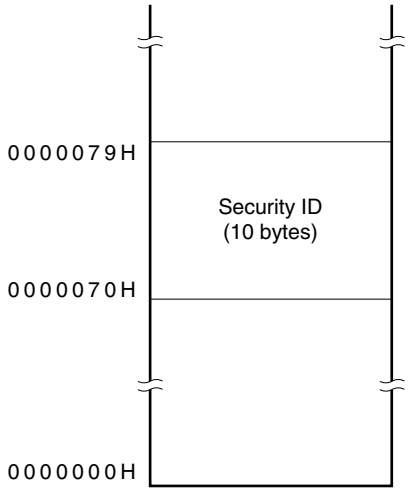
The flash memory versions of the V850ES/JG3-L perform authentication using a 10-byte ID code to prevent the contents of the flash memory from being read by an unauthorized person during on-chip debugging by the on-chip debug emulator.

Set the ID code in the 10-byte internal flash memory area from 0000070H to 0000079H to allow the debugger perform ID authentication.

If the IDs match, the security is released and reading the flash memory and using the on-chip debug emulator are enabled.

- Set the 10-byte ID code to 0000070H to 0000079H.
- Bit 7 of 0000079H is the on-chip debug emulator enable flag.
  (0: Disable, 1: Enable)
- When the on-chip debug emulator is started, the debugger requests ID input. When the ID code input to the debugger and the ID code set in 0000070H to 0000079H match, the debugger starts.
- Debugging cannot be performed if the on-chip debug emulator enable flag is 0, even if the ID codes match.

Figure 31-6. Security ID Area



Caution After the flash memory is erased, 1 is written to the entire area.

32.6 DC Characteristics

32.6.1 Pin characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.2 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	$\overline{RESET}$, FLMD0, P97 to P915	0.8EV_{DD}		EV_{DD}	V
	V_{IH2}	P02 to P06, P30 to P37, P42, P50 to P55, P92 to P96	0.8EV_{DD}		5.5	V
	V_{IH3}	P38, P39, P40, P41, P90, P91	0.7EV_{DD}		5.5	V
	V_{IH4}	PCM0 to PCM3, PCT0, PCT1, PCT4, PCT6, PDH0 to PDH5, PDL0 to PDL15	0.7EV_{DD}		EV_{DD}	V
	V_{IH5}	P70 to P711	0.7AV_{REF0}		AV_{REF0}	V
	V_{IH6}	P10, P11	0.7AV_{REF1}		AV_{REF1}	V
Input voltage, low	V_{IL1}	$\overline{RESET}$, FLMD0, P97 to P915	EV_{SS}		0.2EV_{DD}	V
	V_{IL2}	P02 to P06, P30 to P37, P42, P50 to P55, P92 to P96	EV_{SS}		0.2EV_{DD}	V
	V_{IL3}	P38, P39, P40, P41, P90, P91	EV_{SS}		0.3EV_{DD}	V
	V_{IL4}	PCM0 to PCM3, PCT0, PCT1, PCT4, PCT6, PDH0 to PDH5, PDL0 to PDL15	EV_{SS}		0.3EV_{DD}	V
	V_{IL5}	P70 to P711	AV_{SS}		0.3AV_{REF0}	V
	V_{IL6}	P10, P11	AV_{SS}		0.3AV_{REF1}	V
Input leakage current, high	I_{LIH}	V_I = V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}			5	μA
Input leakage current, low	I_{LIL}	V_I = 0 V			–5	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}			5	μA
Output leakage current, low	I_{LOL}	V_O = 0 V			–5	μA

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

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Symbol	Name	Unit	Page
DTFR2	DMA trigger factor register 2	DMAC	765
DTFR3	DMA trigger factor register 3	DMAC	765
DWC0	Data wait control register 0	BCU	197
ECR	Interrupt source register	CPU	59
EIPC	Interrupt status saving register	CPU	58
EIPSW	Interrupt status saving register	CPU	58
EXIMC	External bus interface mode control register	BCU	187
FEPC	NMI status saving register	CPU	59
FEPSW	NMI status saving register	CPU	59
IIC0	IIC shift register 0	I^2C	700
IIC1	IIC shift register 1	I^2C	700
IIC2	IIC shift register 2	I^2C	700
IICC0	IIC control register 0	I^2C	686
IICC1	IIC control register 1	I^2C	686
IICC2	IIC control register 2	I^2C	686
IICCL0	IIC clock select register 0	I^2C	696
IICCL1	IIC clock select register 1	I^2C	696
IICCL2	IIC clock select register 2	I^2C	696
IICF0	IIC flag register 0	I^2C	694
IICF1	IIC flag register 1	I^2C	694
IICF2	IIC flag register 2	I^2C	694
IICIC0	Interrupt control register	INTC	799
IICIC1	Interrupt control register	INTC	799
IICIC2	Interrupt control register	INTC	799
IICS0	IIC status register 0	I^2C	691
IICS1	IIC status register 1	I^2C	691
IICS2	IIC status register 2	I^2C	691
IICX0	IIC function expansion register 0	I^2C	697
IICX1	IIC function expansion register 1	I^2C	697
IICX2	IIC function expansion register 2	I^2C	697
IMR0	Interrupt mask register 0	INTC	801
IMR0H	Interrupt mask register 0H	INTC	801
IMR0L	Interrupt mask register 0L	INTC	801
IMR1	Interrupt mask register 1	INTC	801
IMR1H	Interrupt mask register 1H	INTC	801
IMR1L	Interrupt mask register 1L	INTC	801
IMR2	Interrupt mask register 2	INTC	801
IMR2H	Interrupt mask register 2H	INTC	801
IMR2L	Interrupt mask register 2L	INTC	801
IMR3	Interrupt mask register 3	INTC	801
IMR3H	Interrupt mask register 3H	INTC	801
IMR3L	Interrupt mask register 3L	INTC	801
INTF0	External interrupt falling edge specification register 0	INTC	815
INTF3	External interrupt falling edge specification register 3	INTC	816
INTF9H	External interrupt falling edge specification register 9H	INTC	817

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Edition	Description	Applied to:
3rd	• Addition of products μPD70F3737F1-GC-CAH-A, 70F3738F1-CAH-A	Throughout
	Modification of **Table 1-1. V850ES/Jx3-L Product List**	**CHAPTER 1 INTRODUCTION**
	Addition of **Figure 3-10 Sign Extension in Data Space**	**CHAPTER 3 CPU FUNCTION**
	Modification of **Table 5-3 Pin Statuses When Internal ROM, Internal RAM, or On-Chip Peripheral I/O Is Accessed**	**CHAPTER 5 BUS CONTROL FUNCTION**
	Addition of **5.11 SRAM Connection Examples**	
	Addition of **6.4.3 External clock signal input**	**CHAPTER 6 CLOCK GENERATOR**
	Addition of **6.6 How to Connect a Resonator**	
	Addition of **7.2.1 Pins used by TMPn**	**CHAPTER 7 16-BIT TIMER/EVENT COUNTER P (TMP)**
	Addition of **7.2.2 Interrupts**	
	Addition of **7.4 (1) Basic counter operation**	
	Addition of **7.4 (2) Anytime write and batch write**	
	Addition of **7.4.1 (3) Operation of interval timer based on input of external event count**	
	Modification of **Figure 7-28 Register Settings in External Trigger Pulse Output Mode**	
	Modification of **Figure 7-40 Register Settings in One-Shot Pulse Output Mode**	
	Addition of **8.2.1 Pins used by TMQ0**	**CHAPTER 8 16-BIT TIMER/EVENT COUNTER Q (TMQ)**
	Addition of **8.2.2 Interrupts**	
	Addition of **8.4 (1) Basic counter operation**	
	Addition of **8.4 (2) Anytime write and batch write**	
	Addition of **8.4.1 (3) Operation of interval timer based on input of external event count**	
	Modification of **Figure 8-28 Register Settings in External Trigger Pulse Output Mode**	
	Modification of **Figure 8-40 Register Settings in One-Shot Pulse Output Mode**	
	Modification of **Figure 13-4 Example of Timing in Continuous Select Mode (ADA0S Register = 01H)**	**CHAPTER 13 A/D CONVERTER**
	Modification of **Figure 13-5 Example of Timing in Continuous Scan Mode (ADA0S Register = 03H)**	
	Modification of **Figure 13-6 Example of Timing in One-Shot Select Mode (ADA0S Register = 01H)**	
	Modification of **Figure 13-7 Example of Timing in One-Shot Scan Mode (ADA0S Register = 03H)**	
	Modification of **Figure 13-8 Example of Timing in Continuous Select Mode (When Power-Fail Comparison Is Made: ADA0PFM.ADA0PFC bit = 0, ADA0S Register = 01H)**	
	Modification of **Figure 13-9 Example of Timing in Continuous Scan Mode (When Power-Fail Comparison Is Made: ADA0PFM.ADA0PFC bit = 0, ADA0S Register = 03H)**	
	Modification of **Figure 13-10 Example of Timing in One-Shot Select Mode (When Power-Fail Comparison Is Made: ADA0PFM.ADA0PFC bit = 1, ADA0S Register = 01H)**	
	Modification of **Figure 13-11 Example of Timing in One-Shot Scan Mode (When Power-Fail Comparison Is Made: ADA0PFM.ADA0PFC bit = 0, ADA0S Register = 03H)**	