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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

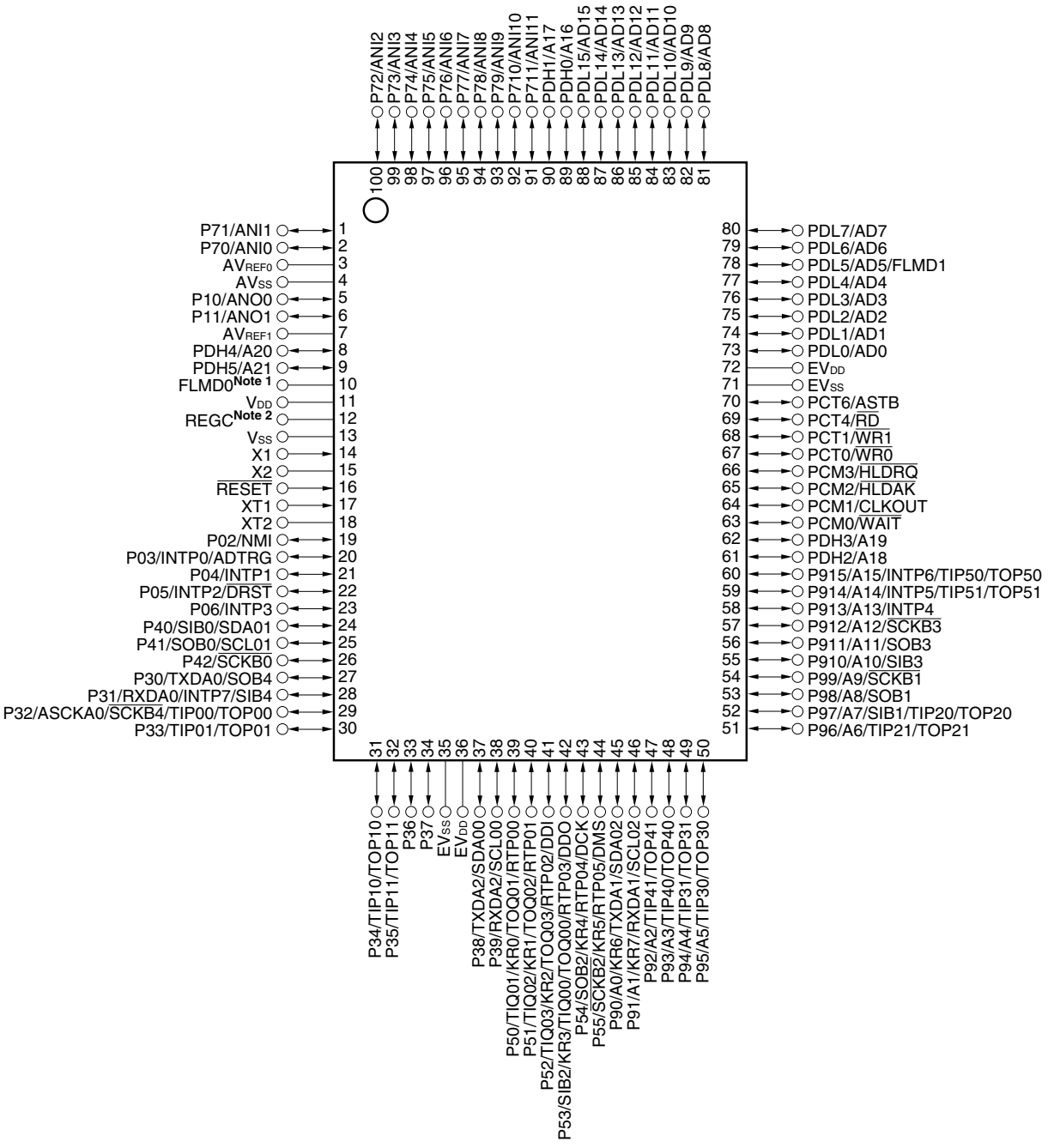
Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	83
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-LFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3792f1-cah-a

1.5 Pin Configuration (Top View)

100-pin plastic LQFP (14 × 20)

μPD70F3737GF-GAS-AX[Note] μPD70F3738GF-GAS-AX[Note]

Note Under development



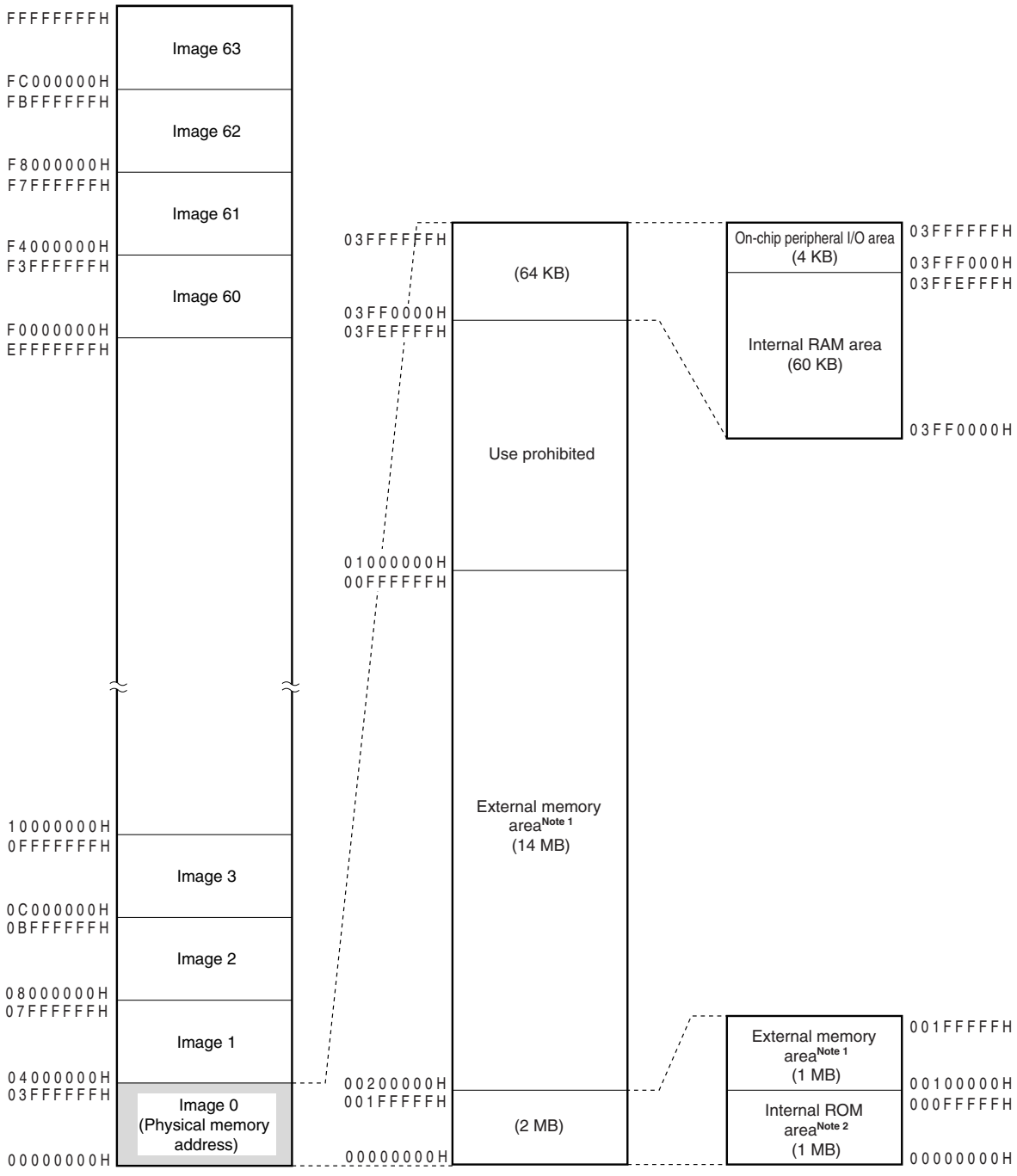
Notes 1. The FLMD0 pin is used in flash programming. Connect this pin to V_{SS} in the normal operation mode.

2. Connect the REGC pin to V_{SS} via a 4.7 μF (recommended value) capacitor.

3.4.2 Memory map

The areas shown below are reserved in the V850ES/JG3-L.

Figure 3-2. Data Memory Map (Physical Addresses)



Notes 1. The V850ES/JG3-L has 22 address pins, so the external memory area appears as a repeated 4 MB image.

2. Fetch and read accesses to addresses 00000000H to 000FFFFFH are made to the internal ROM area. However, data write accesses to these addresses are made to the external memory area.

(7) Port 0 function register (PF0)

After reset: 00H R/W Address: FFFFFC60H

	7	6	5	4	3	2	1	0
PF0	0	PF06	PF05	PF04	PF03	PF02	0	0

PF0n	Specification of normal output (CMOS output) or N-ch open-drain output (n = 2 to 6)
0	Normal output (CMOS output)
1	N-ch open-drain output

Caution When an output pin is pulled up to EV_{DD} or higher, be sure to set the PF0n bit to 1.

(2) Port 1 mode register (PM1)

After reset: FFH R/W Address: FFFFF422H

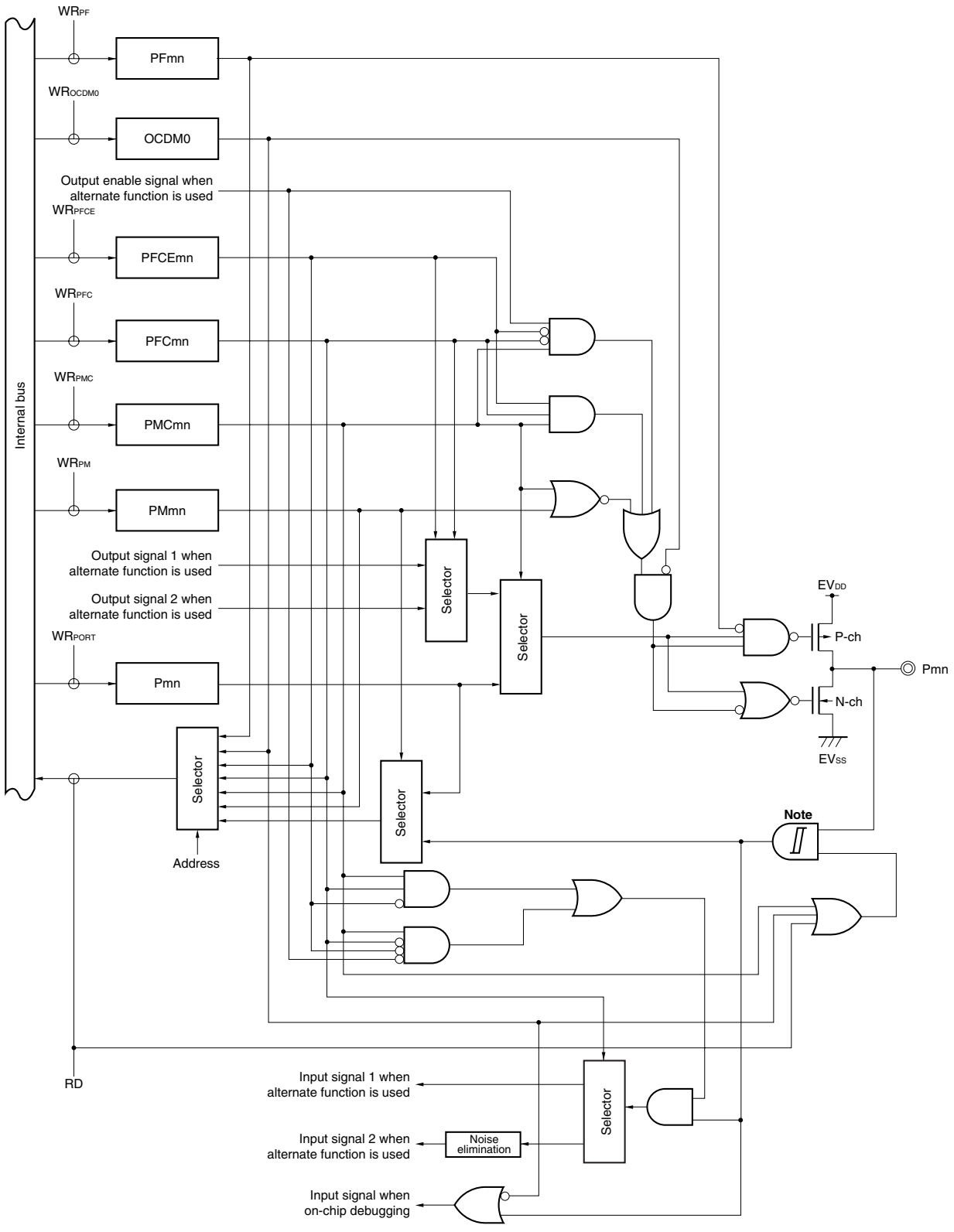
	7	6	5	4	3	2	1	0
PM1	1	1	1	1	1	1	PM11	PM10

PM1n	I/O mode control (n = 0, 1)
0	Output mode
1	Input mode

Cautions 1. When using P1n as the alternate function (ANOn pin output), specify the input mode (PM1n bit = 1).

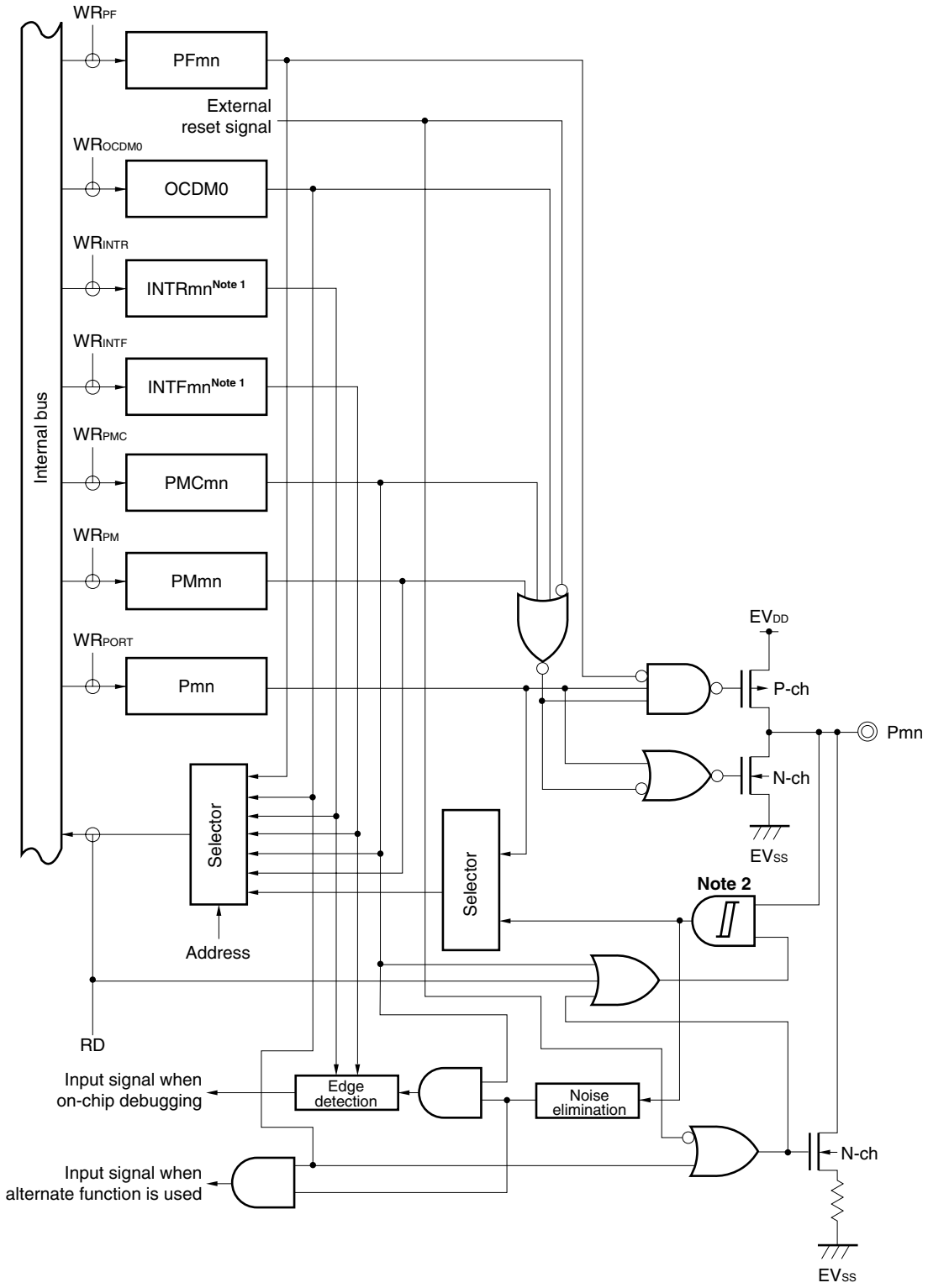
2. When using one of the P10 and P11 pins as an I/O port and the other as a D/A output pin, do so in an application where the port I/O level does not change during D/A output.

Figure 4-25. Block Diagram of Type U-9



Note There are no hysteresis characteristics in port mode.

Figure 4-33. Block Diagram of Type AA-1

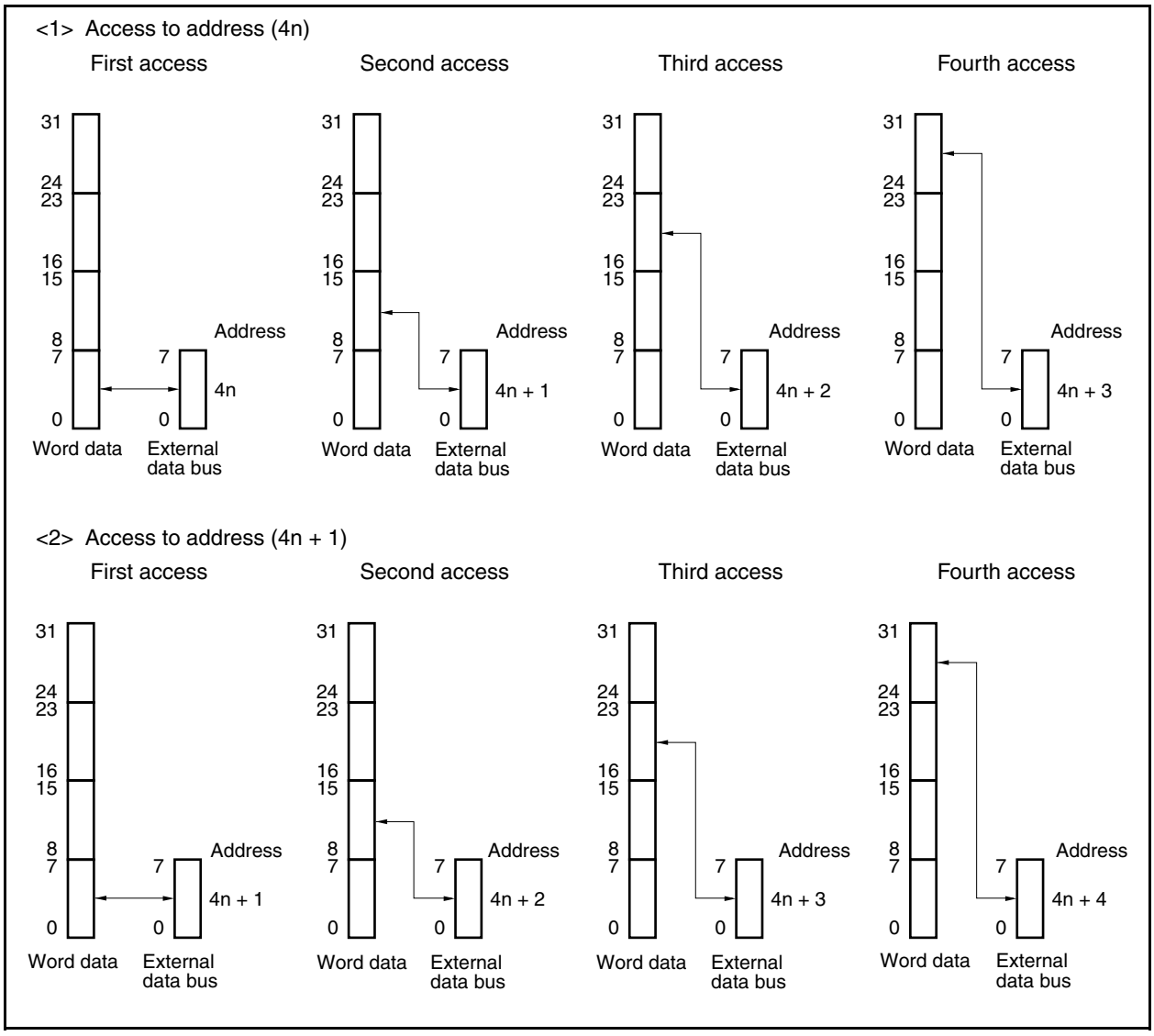


Notes 1. See **21.7 External Interrupt Request Input Pins (NMI and INTP0 to INTP7)**.

2. There are no hysteresis characteristics in port mode.

(b) 8-bit data bus width (1/2)

32-bit data is transmitted/received via an 8-bit bus. Therefore, the data is transmitted/received in four accesses. The data is transmitted/received to/from the specified even/odd address of the external data bus.



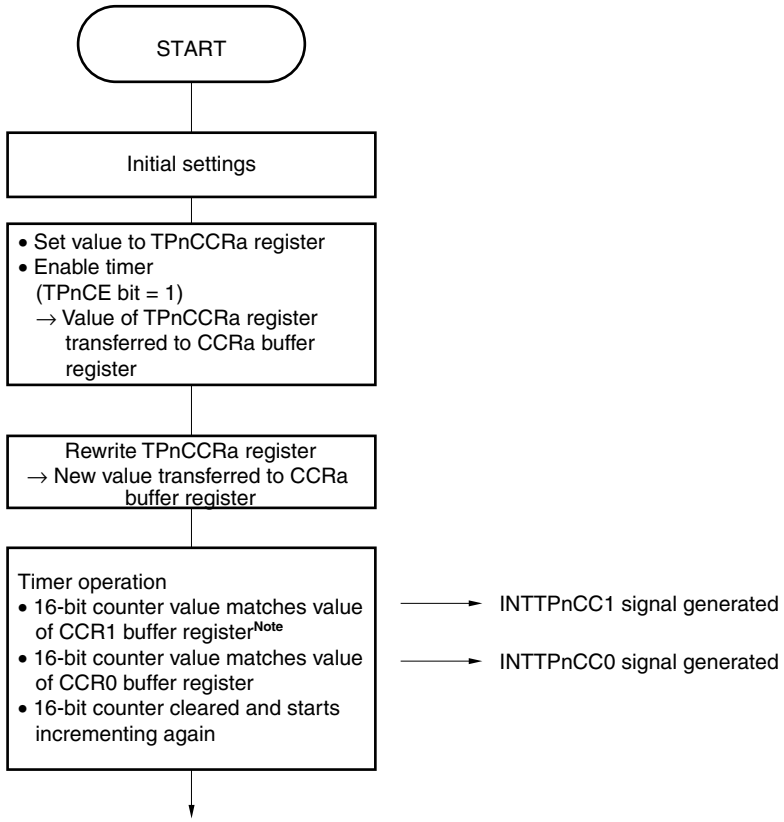
/(2) Anytime write and batch write

The TPnCCR0 and TPnCCR1 registers can be written even while TMPn is operating (that is, while the TPnCTL0.TPnCE bit is 1), but the way the CCR0 and CCR1 buffer registers are written differs depending on the mode. The two writing methods are anytime write and batch write.

(a) Anytime write

This writing method is used to transfer data from the TPnCCR0 and TPnCCR1 registers to the CCR0 and CCR1 buffer registers any time while TMPn is operating.

Figure 7-2. Flowchart Showing Basic Anytime Write Operation



Note The 16-bit counter is only cleared when its value matches the value of the CCR0 buffer register, not the CCR1 buffer register.

Remarks 1. The flowchart applies to the case when TMPn is being used as an interval timer.

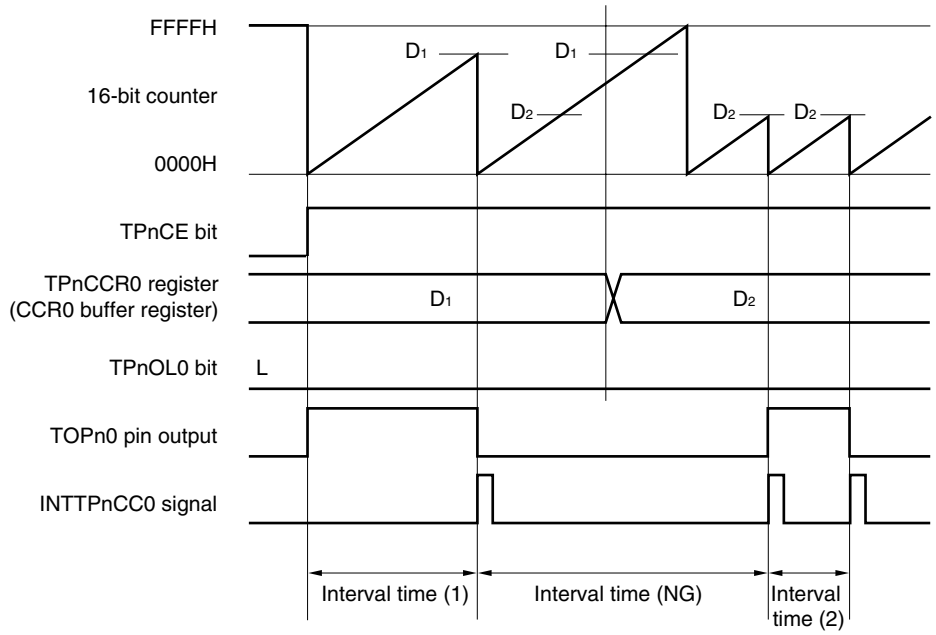
2. a = 0, 1
n = 0 to 5

(c) Notes on rewriting TPnCCR0 register

When rewriting the value of the TPnCCR0 register to a smaller value, stop counting first and then change the set value.

If the value of the TPnCCR0 register is rewritten to a smaller value during counting, the 16-bit counter may overflow.

Figure 7-12. Rewriting TPnCCR0 Register



Remarks 1. Interval time (1): $(D_1 + 1) \times$ Count clock cycle
Interval time (NG): $(10000H + D_2 + 1) \times$ Count clock cycle
Interval time (2): $(D_2 + 1) \times$ Count clock cycle

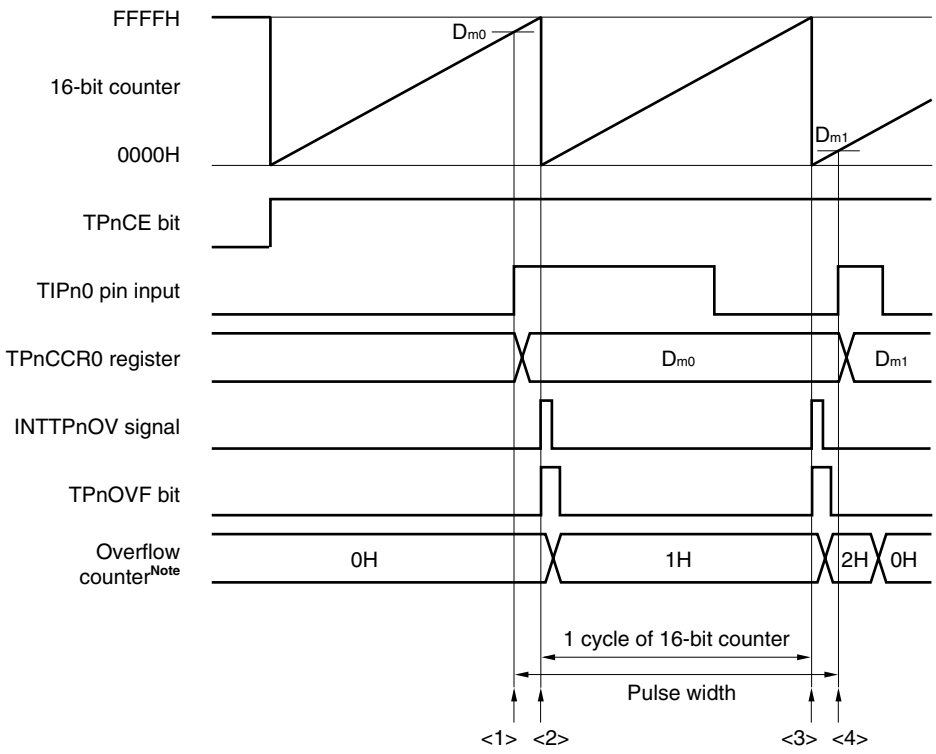
2. n = 0 to 5

If the value of the TPnCCR0 register is changed from D_1 to D_2 while the counter value is greater than D_2 but less than D_1, the TPnCCR0 register value is transferred to the CCR0 buffer register as soon as the register has been rewritten. Consequently, the value that is compared with the 16-bit counter value is D_2.

Because the counter value has already exceeded D_2, however, the 16-bit counter counts up to FFFFH, overflows, and then counts up again from 0000H. When the counter value matches D_2, the INTTPnCC0 signal is generated and the output of the TOPn0 pin is inverted.

Therefore, the INTTPnCC0 signal may not be generated at the interval "$(D_1 + 1) \times$ Count clock cycle" or "$(D_2 + 1) \times$ Count clock cycle" as originally expected, but instead may be generated at an interval of "$(10000H + D_2 + 1) \times$ Count clock cycle".

Figure 7-64. Example of Using Software Processing to Resolve Problem When Capture Trigger Interval Is Long (When Using TIPn0)



Note The overflow counter is set on the internal RAM by software.

<1> The TPnCCR0 register is read (the default value of the TIPn0 pin input is set).

<2> An overflow occurs. The overflow counter is incremented and the TPnOVF bit is cleared to 0 in the overflow interrupt servicing.

<3> An overflow occurs a second time. The overflow counter is incremented and the TPnOVF bit is cleared to 0 in the overflow interrupt servicing.

<4> The TPnCCR0 register is read.

The overflow counter is read.

→ If the overflow counter is N, the pulse width can be calculated by ($N \times 10000H + D_{a1} - D_{a0}$).
In this example, because an overflow occurred twice, the pulse width is calculated as ($20000H + D_{a1} - D_{a0}$).

The overflow counter is cleared to 0H.

Remark n = 0 to 5

(e) Clearing the overflow flag (TPnOVF)

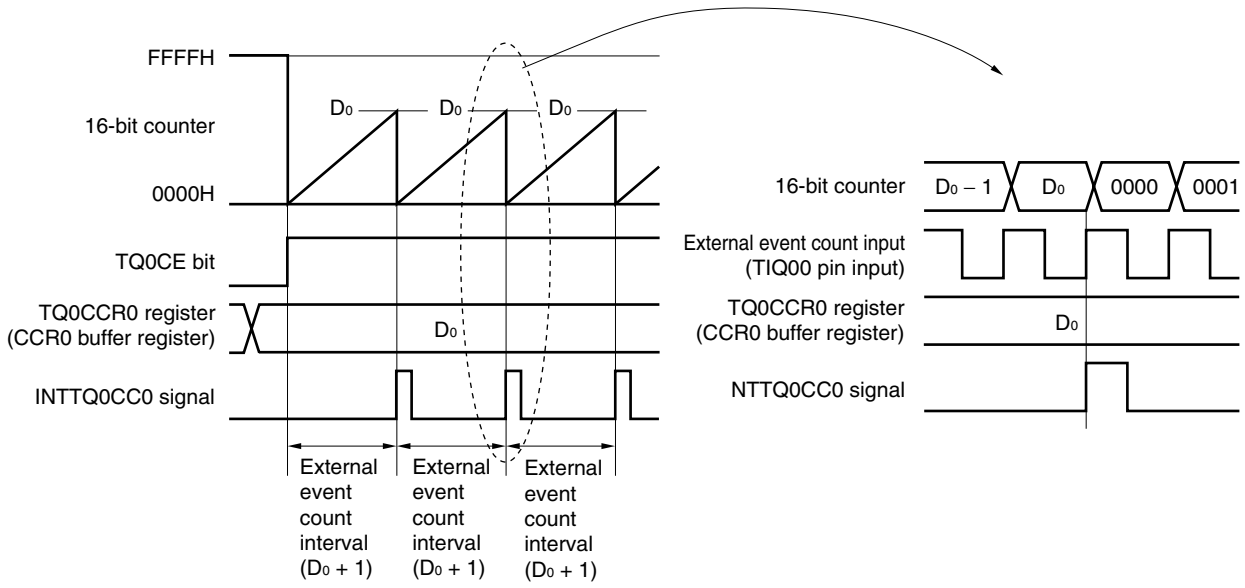
The overflow flag (TPnOVF) can be cleared to 0 by reading the TPnOVF bit and, if its value is 1, either clearing the bit to 0 by using the CLR1 instruction or by writing 8-bit data (with bit 0 as 0) to the TPnOPT0 register.

When the TQ0CE bit is set to 1, the value of the 16-bit counter is cleared from FFFFH to 0000H. The counter increments each time the valid edge of the external event count input is detected, and the value of the TQ0CCR0 register is transferred to the CCR0 buffer register.

When the value of the 16-bit counter matches the value of the CCR0 buffer register, the 16-bit counter is cleared to 0000H, and a compare match interrupt request signal (INTTQ0CC0) is generated.

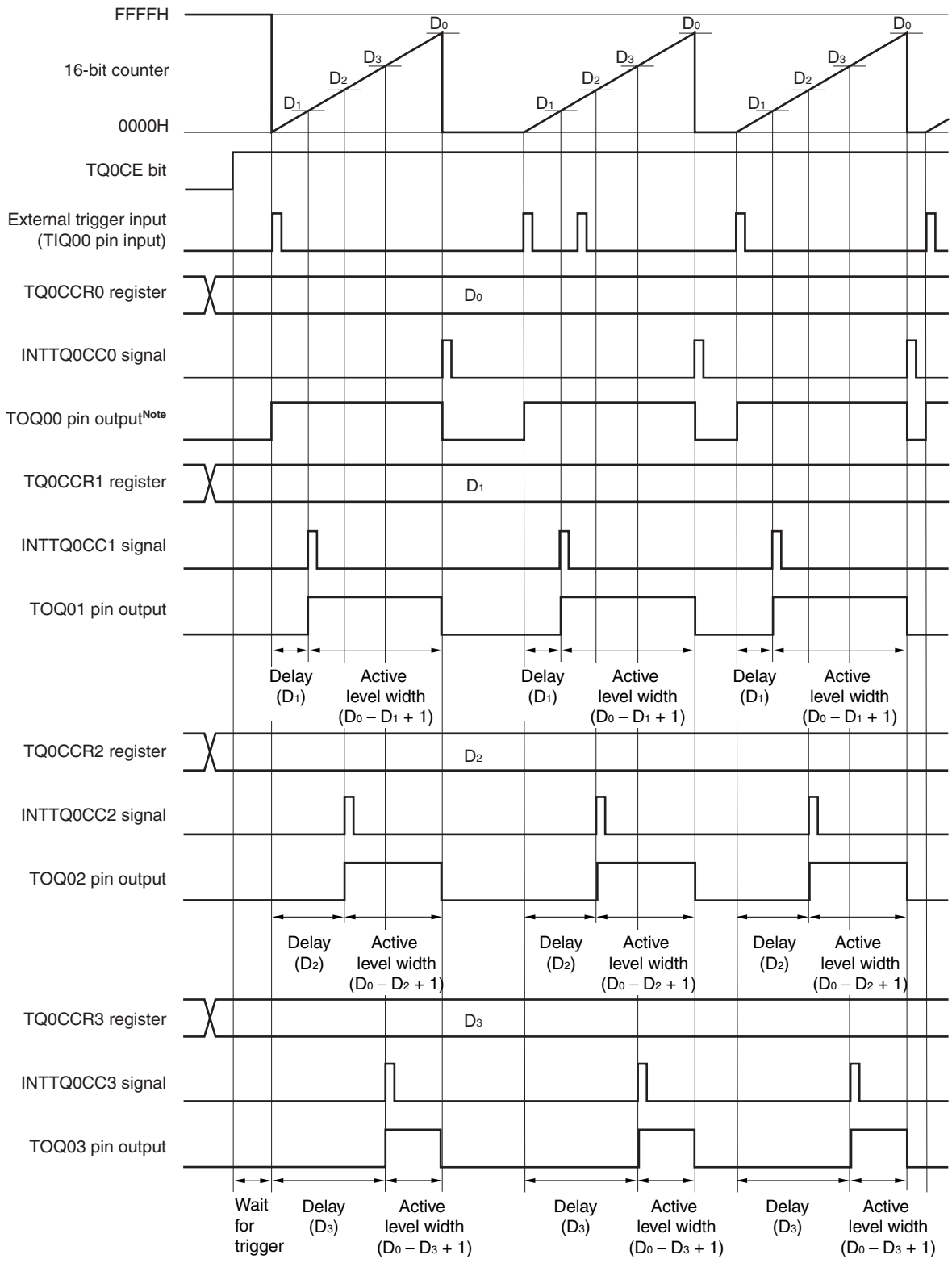
The INTTQ0CC0 signal is generated each time the valid edge of the external event count input has been detected the specified number of times (that is, the value of the TQ0CCR0 register + 1).

Figure 8-18. Basic Timing of Operations in External Event Count Mode



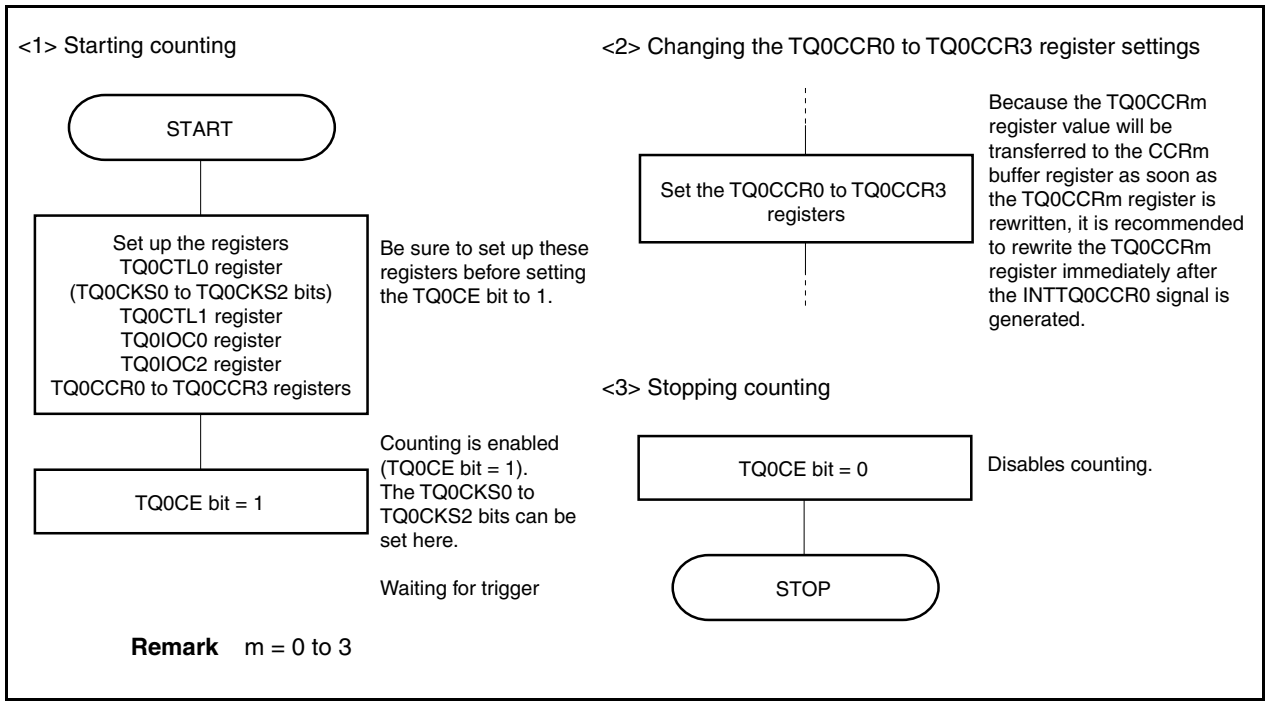
Remark This figure shows the basic timing when the rising edge is specified as the valid edge of the external event count input.

Figure 8-39. Basic Timing of Operations in One-Shot Pulse Output Mode



Note The output from the TOQ00 pin can also be used as the input to the TIQ00 pin. When using the output from the TOQ00 pin as the input to the TIQ00 pin, use a software trigger instead of an external trigger.

Figure 8-41. Timing and Processing of Operations in One-Shot Pulse Output Mode (2/2)

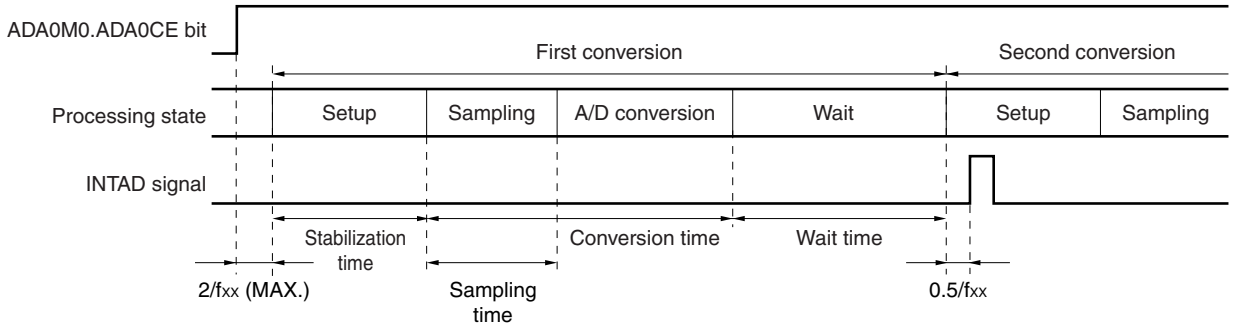


Remark m = 0 to 3

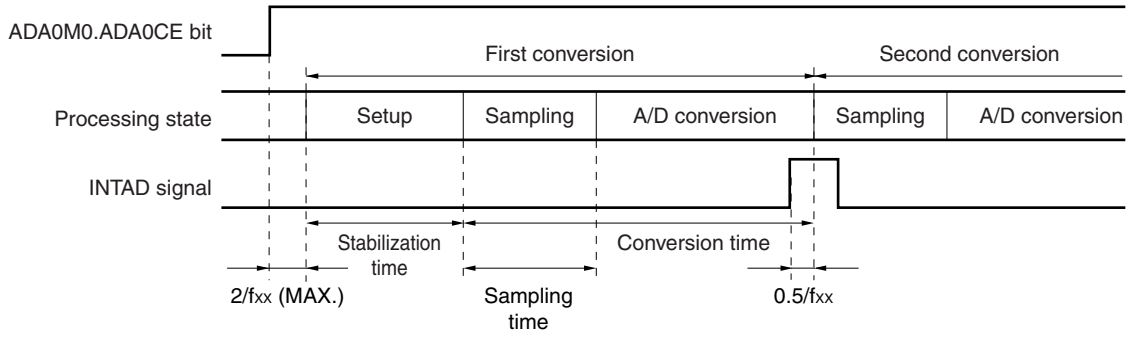
14.5.2 Conversion timing

Figure 14-3. Conversion Timing (Continuous Conversion)

(1) Operation in normal conversion mode (ADA0HS1 bit = 0)



(2) Operation in high-speed conversion mode (ADA0HS1 bit = 1)

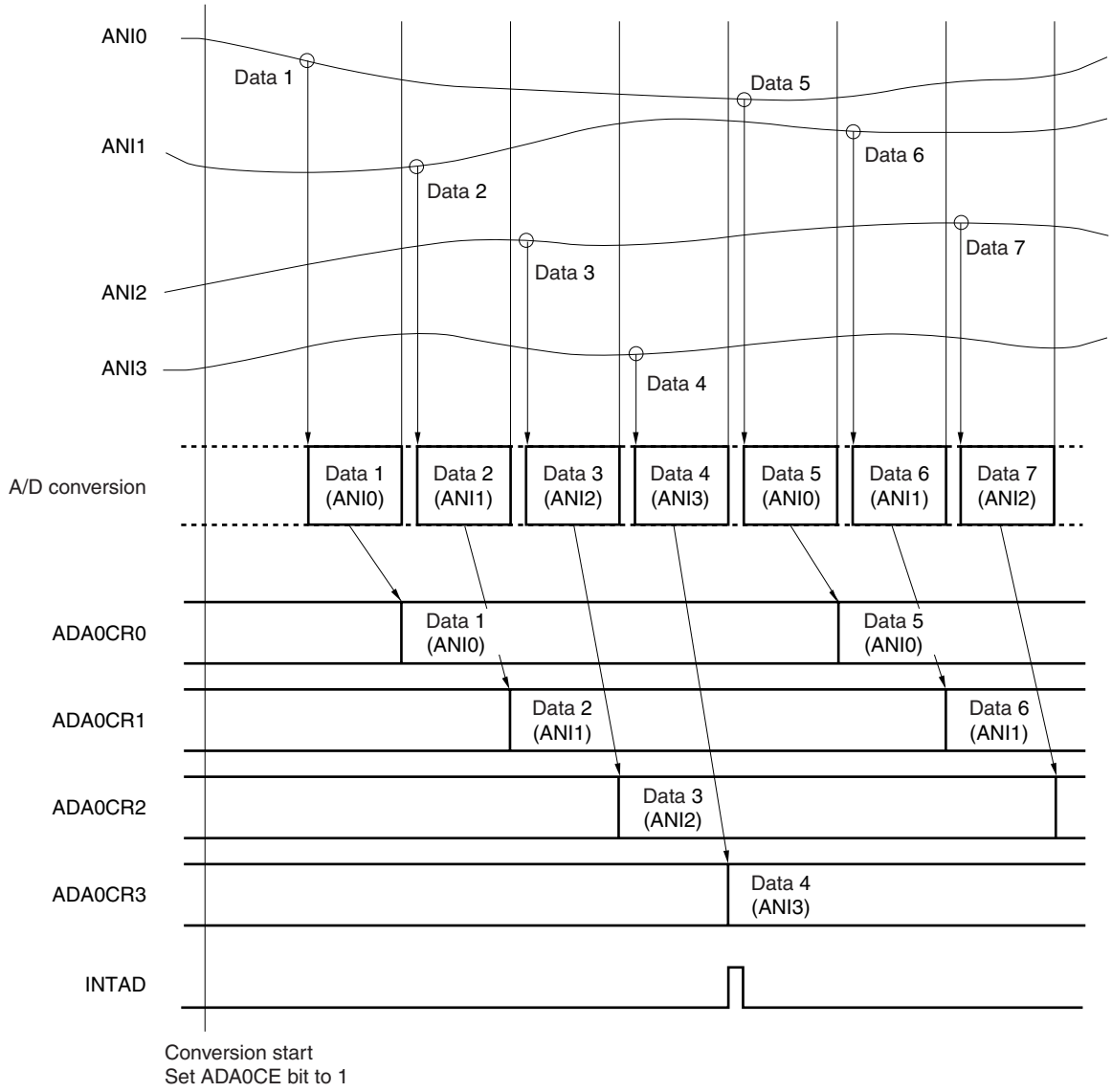


ADA0FR2 to ADA0FR0 Bits	Stabilization Time	Conversion Time (Sampling Time)	Wait Time	Trigger Response Time
000	13/fxx	26/fxx (8/fxx)	27/fxx	3/fxx
001	26/fxx	52/fxx (16/fxx)	53/fxx	3/fxx
010	39/fxx	78/fxx (24/fxx)	79/fxx	3/fxx
011	50/fxx	104/fxx (32/fxx)	105/fxx	3/fxx
100	50/fxx	130/fxx (40/fxx)	131/fxx	3/fxx
101	50/fxx	156/fxx (48/fxx)	157/fxx	3/fxx
110	50/fxx	182/fxx (56/fxx)	183/fxx	3/fxx
111	50/fxx	208/fxx (64/fxx)	209/fxx	3/fxx

Remark The above timings apply to the software trigger mode. In the external trigger mode/timer trigger mode, a trigger response time is inserted.

Figure 14-5. Example of Timing in Continuous Scan Mode (ADA0S Register = 03H) (1/2)

(a) Timing example

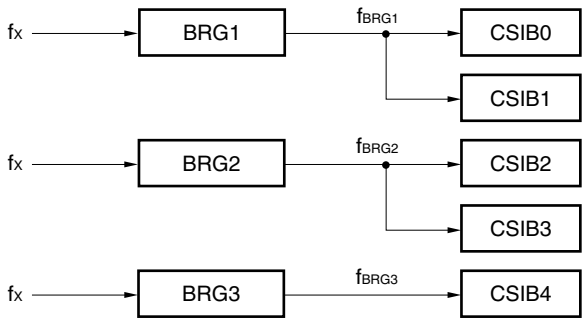


Remark The above timing applies to the software trigger mode (ADA0M0.AD0TMD bit = 0) or the high-speed conversion mode (ADA0M1.ADA0HS1 bit = 1).

18.8 Baud Rate Generator

The BRG1 to BRG3 and CSIB0 to CSIB4 baud rate generators are connected as shown in the following block diagram.

Figure 18-31. Baud Rate Generator Connection



(1) Prescaler mode registers 1 to 3 (PRSM1 to PRSM3)

The PRSM1 to PRSM3 registers control generation of the baud rate signal for CSIBn.

These registers can be read or written in 8-bit or 1-bit units.

Reset sets these registers to 00H.

After reset: 00H R/W Address: PRSM1 FFFFF320H, PRSM2 FFFFF324H, PRSM3 FFFFF328H

PRSMm (m = 1 to 3)

7	6	5	<4>	3	2	1	0
0	0	0	BGCEm	0	0	BGCSm1	BGCSm0

BGCEm	Baud rate output
0	Disabled
1	Enabled

BGCSm1	BGCSm0	Input clock selection (f_{BGCSm})	Setting value (k)
0	0	f_{XX}	0
0	1	$f_{XX}/2$	1
1	0	$f_{XX}/4$	2
1	1	$f_{XX}/8$	3

Cautions 1. Do not rewrite the PRSMm register during operation.

2. Before setting the BGCEm bit to 1, set the BGCSm1 and BGCSm0 bits and prescaler compare registers 1 to 3 (PRSCM1 to PRSCM3).

3. Be sure to clear bits 7 to 5, 3 and 2 to "0".

21.6 Multiple Interrupt Servicing Control

In multiple interrupt servicing control, the servicing of an interrupt is stopped if an interrupt request signal that has a higher priority level is generated. The higher priority interrupt request signal is then acknowledged and the interrupt is serviced.

If an interrupt request signal with a lower or equal priority level is generated while an interrupt is being serviced, the newly generated interrupt request signal will be held pending.

Multiple interrupt servicing control is performed when interrupts are enabled (PSW.ID bit = 0). Even in an interrupt service routine, multiple interrupt control must be performed while interrupts are enabled (ID bit = 0). If a maskable interrupt or software exception occurs in a maskable interrupt or software exception service program, EIPC and EIPSW must be saved.

The following example shows the procedure for servicing multiple interrupts.

(1) To acknowledge maskable interrupt request signals in a service program

Service program for maskable interrupt or exception

```
    …
    …
• EIPC saved to memory or register
• EIPSW saved to memory or register
• EI instruction (enables interrupt acknowledgment)
    …
    …                          ←Acknowledges maskable interrupt
    …
    …
• DI instruction (disables interrupt acknowledgment)
• Saved value restored to EIPSW
• Saved value restored to EIPC
• RETI instruction
```

CHAPTER 27 CRC FUNCTION

27.1 Functions

- Generation of CRC (Cyclic Redundancy Check) code for detecting errors in communication data
- Generation of CRC code for detecting errors in data blocks
- Generation of 16-bit CRC code using a CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) generation polynomial for blocks of data of any length in 8-bit units
- CRC code is set to the CRC data register each time 1-byte data is transferred to the CRCIN register, after the initial value is set to the CRCD register.

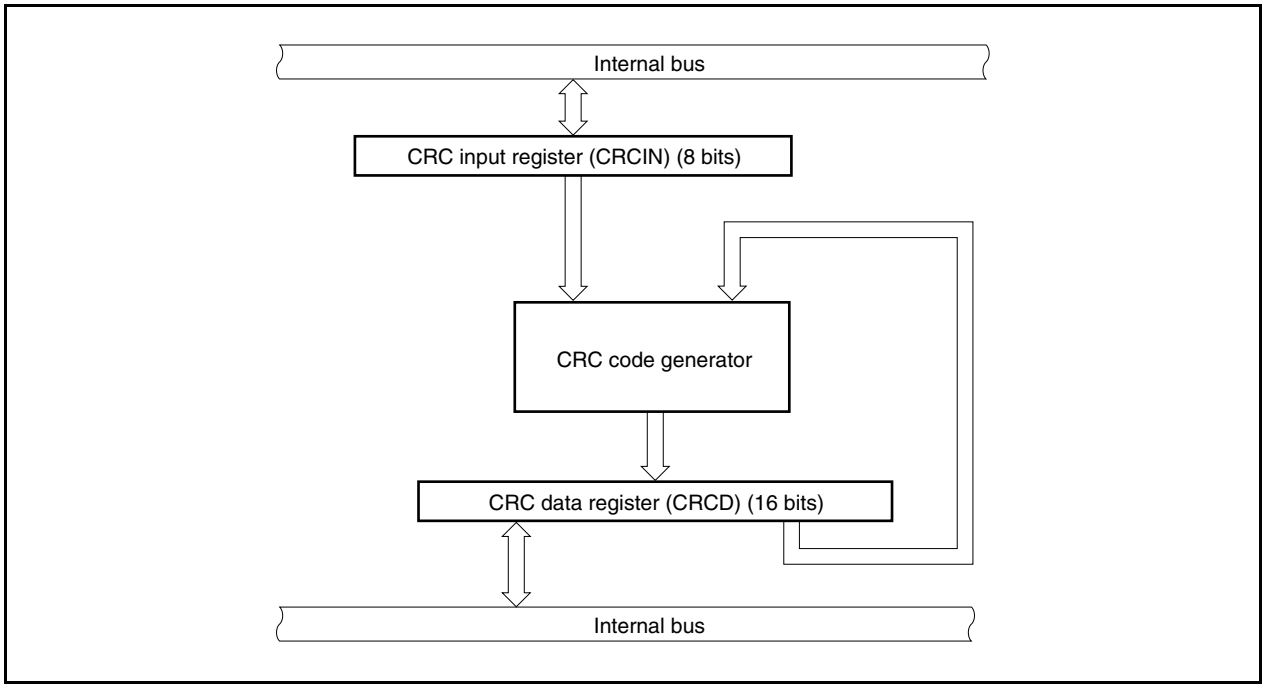
27.2 Configuration

The CRC function includes the following hardware.

Table 27-1. CRC Configuration

Item	Configuration
Control registers	CRC input register (CRCIN) CRC data register (CRCD)

Figure 27-1. Block Diagram of CRC Function



31.2.4 Cautions

(1) Handling of device that was used for debugging

Do not mount a device that was used for debugging on a mass-produced product, because the flash memory was rewritten during debugging and the number of rewrites of the flash memory cannot be guaranteed. Moreover, do not embed the debug monitor program into mass-produced products.

(2) When breaks cannot be executed

Forced breaks cannot be executed if one of the following conditions is satisfied.

- Interrupts are disabled (DI)
- Interrupts issued for the serial interface, which is used for communication between MINICUBE2 and the target device, are masked
- Standby mode is entered while standby release by a maskable interrupt is prohibited
- Mode for communication between MINICUBE2 and the target device is UARTA0, and the main clock has been stopped

(3) When pseudo real-time RAM monitor (RRM) function and DMM function do not operate

The pseudo RRM function and DMM function do not operate if one of the following conditions is satisfied.

- Interrupts are disabled (DI)
- Interrupts issued for the serial interface, which is used for communication between MINICUBE2 and the target device, are masked
- Standby mode is entered while standby release by a maskable interrupt is prohibited
- Mode for communication between MINICUBE2 and the target device is UARTA0, and the main clock has been stopped
- Mode for communication between MINICUBE2 and the target device is UARTA0, and a clock different from the one specified in the debugger is used for communication

(4) Standby release with pseudo RRM and DMM functions enabled

The standby mode is released by the pseudo RRM function and DMM function if one of the following conditions is satisfied.

- Mode for communication between MINICUBE2 and the target device is CSIB0 or CSIB3
- Mode for communication between MINICUBE2 and the target device is UARTA0, and the main clock has been supplied.

(5) Writing to peripheral I/O registers that require a specific sequence, using DMM function

Peripheral I/O registers that require a specific sequence cannot be written by using the DMM function.

(6) Flash self programming

If the space where the debug monitor program is allocated is rewritten by flash self programming, the debugger can no longer operate normally.

(7) On-chip debugging can be used when the supply voltage (V_{DD}) is in a range of 2.7 to 3.6 V. It cannot be used at less than 2.7 V.

A.7 Flash Memory Writing Tools

Flashpro IV (part number: PG-FP4) Flashpro V (part number: PG-FP5) Flash memory programmer	Flash memory programmer dedicated to microcontrollers with internal flash memory.
QB-MINI2 (MINICUBE2)	On-chip debug emulator with programming function.
FA-100GC-UEU-B FA-100GF-GAS-B Flash memory writing adapter	Flash memory writing adapter used connected to the Flashpro IV, Flashpro V, etc. (not wired). • FA-100GC-UEU-B: 100-pin plastic LQFP (GC-UEU type) • FA-100GF-GAS-B: 100-pin plastic LQFP (GF-GAS type)
<R> FA-70F3738GC-UEU-RX <R> FA-70F3738GF-GAS-RX <R> FA-70F3738F1-CAH-RX <R> FA-70F3793F1-CAH-RX (Tentative name : Under development) <R> FA-70F3793GC-UEU-RX (Tentative name : Under development) Flash memory writing adapter	Flash memory writing adapter used connected to the Flashpro IV, Flashpro V, etc. (already wired). • FA-70F3738GC-UEU-RX: 100-pin plastic LQFP (GC-UEU type) • FA-70F3738GF-GAS-RX: 100-pin plastic LQFP (GF-GAS type) • FA-70F3738F1-CAH-RX: 121-pin plastic FBGA (F1-CAH type of μPD70F3737, 70F3738) • FA-70F3793F1-CAH-RX (Tentative name : Under development): 121-pin plastic FBGA (F1-CAH type of μPD70F3792, 70F3793) • FA-70F3793GC-UEU-RX (Tentative name : Under development): 100-pin plastic LQFP (GC-UEU type of μPD70F3792, 70F3793)

Remark FA-100GC-UEU-B, FA-100GF-GAS-B, FA-70F3738GC-UEU-RX, FA-70F3738GF-GAS-RX, FA-70F3738F1-CAH-RX, FA-70F3793F1-CAH-RX and FA-70F3793GC-UEU-RX are products of Naito Densei Machida Mfg. Co., Ltd.
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