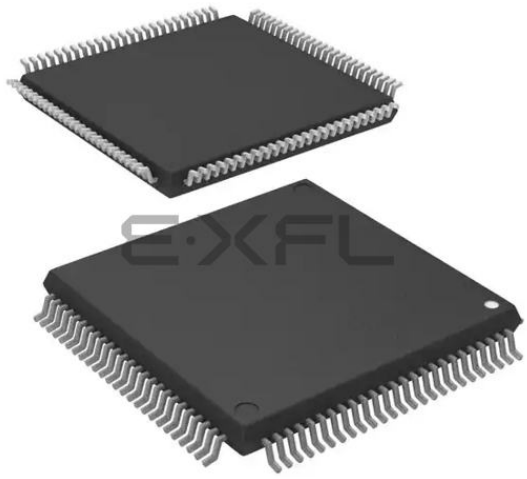
Renesas Electronics America Inc - UPD70F3792GC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	83
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3792gc-ueu-ax

CHAPTER 1 INTRODUCTION

The V850ES/JG3-L is one of the products in the NEC Electronics V850 single-chip microcontroller series designed for low-power operation for real-time control applications.

1.1 General

The V850ES/JG3-L is a 32-bit single-chip microcontroller that includes the V850ES CPU core and peripheral functions such as ROM/RAM, timer/counters, serial interfaces, an A/D converter, and a D/A converter.

In addition to high real-time response characteristics and 1-clock-pitch basic instructions, the V850ES/JG3-L features multiply instructions, saturated operation instructions, bit manipulation instructions, etc., realized by a hardware multiplier, as optimum instructions for digital servo control applications. Moreover, as a real-time control system, the V850ES/JG3-L enables an extremely high cost-performance for applications that require super low power consumption, such as digital cameras, electrical power meters, and mobile terminals.

Table 1-1 lists the products of the V850ES/JG3-L and V850ES/JF3-L.

The V850ES/JF3-L is a model of the V850ES/JG3-L with reduced I/O, timer/counter, and serial interface functions.

<R> **(2) Non-port functions**

(1/6)

Function	Pin No.			I/O	Description	Alternate Function
	GF	GC	F1			
A0	45	43	H8	Output	Address bus for external memory (when using separate bus) N-ch open-drain output selectable. 5 V tolerant.	P90/KR6/TXDA1/SDA02
A1	46	44	L9			P91/KR7/RXDA1/SCL02
A2	47	45	K9			P92/TIP41/TOP41 (/TXDA4)Note1
A3	48	46	J9			P93/TIP40/TOP40 (/RXDA4)Note1
A4	49	47	L10			P94/TIP31/TOP31(/TXDA5)Note1
A5	50	48	K10			P95/TIP30/TOP30 (/RXDA5)Note1
A6	51	49	K11			P96 (/TXDC0)Note1/TIP21/TOP21
A7	52	50	J11			P97/SIB1 (/RXDC0)Note1/TIP20/TOP20
A8	53	51	J10			P98/SOB1
A9	54	52	H11			P99/$\overline{\text{SCKB1}}$
A10	55	53	H10			P910/SIB3
A11	56	54	H9			P911/SOB3
A12	57	55	G11			P912/$\overline{\text{SCKB3}}$
A13	58	56	G10			P913/INTP4
A14	59	57	G9			P914/INTP5/TIP51/TOP51
A15	60	58	G8			P915/INTP6/TIP50/TOP50
A16	89	87	C6	Output	Address bus for external memory	PDH0
A17	90	88	D6			PDH1
A18	61	59	F9			PDH2
A19	62	60	F8			PDH3
A20	8	6	F4			PDH4
A21	9	7	J2, G4Note1			P02/NMINote1 PDH5Note2
AD0	73	71	C11	I/O	Address bus/data bus for external memory	PDL0
AD1	74	72	C10			PDL1
AD2	75	73	C9			PDL2
AD3	76	74	B11			PDL3
AD4	77	75	B10			PDL4
AD5	78	76	A10			PDL5/FLMD1
AD6	79	77	A9			PDL6
AD7	80	78	B9			PDL7
AD8	81	79	A8			PDL8
AD9	82	80	B8			PDL9
AD10	83	81	C8			PDL10
AD11	84	82	A7			PDL11
AD12	85	83	B7			PDL12
AD13	86	84	C7			PDL13
AD14	87	85	D7			PDL14
AD15	88	86	B6			PDL15

Notes1. μPD70F3792, 70F3793 only.

2. μPD70F3737, 70F3738 only.

Remark GF: 100-pin plastic LQFP (14 × 20) (μPD70F3737, 70F3738 only)
GC: 100-pin plastic LQFP (fine pitch) (14 × 14)
F1: 121-pin plastic FBGA (8 × 8)

(1) Port n register (Pn)

Data I/O with external devices is performed by writing to and reading from the Pn register. The Pn register is made up of a port latch that retains the output data and a circuit that reads the pin status.

Each bit of the Pn register corresponds to one pin of port n and can be read or written in 1-bit units.

After reset: 00H[Note] (output latch) R/W

	7	6	5	7	3	2	1	0
Pn	Pn7	Pn6	Pn5	Pn4	Pn3	Pn2	Pn1	Pn0

Pnm	Control of output data (in output mode)
0	0 is output.
1	1 is output.

Note This value is undefined for input-only ports.

The operation when writing or reading the Pn register differs depending on the specified mode.

Table 4-3. Reading and Writing Pn Register

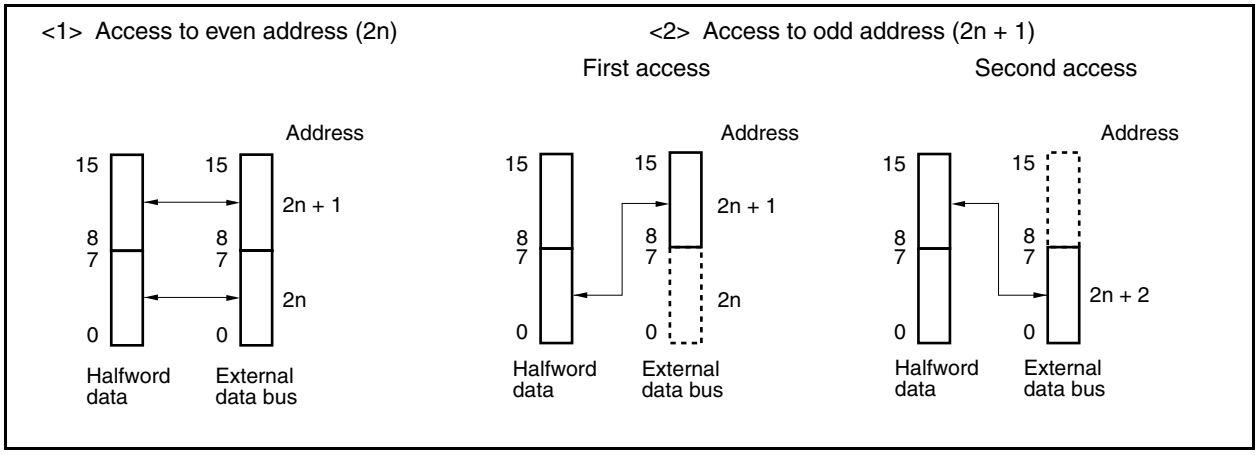
PMCn Register Setting	PMn Register Setting	Writing Pn Register	Reading Pn Register
Port mode (PMCnm bit = 0)	Output mode (PMnm bit = 0)	Write to the output latch[Note]. The contents of the output latch are output from the pin.	The value of the output latch is read.
	Input mode (PMnm bit = 1)	Write to the output latch[Note]. The status of the pin is not affected.	The pin status is read.
Alternate-function mode (PMCnm bit = 1)	Output mode (PMnm bit = 0)	Write to the output latch[Note]. The status of the pin is not affected. The pin operates as an alternate-function pin.	The value of the output latch is read.
	Input mode (PMnm bit = 1)	Write to the output latch[Note]. The status of the pin is not affected. The pin operates as an alternate-function pin.	The pin status is read.

Note The value written to the output latch is retained until a new value is written to the output latch. The output latch value is cleared by a reset.

(3) Halfword access (16 bits)

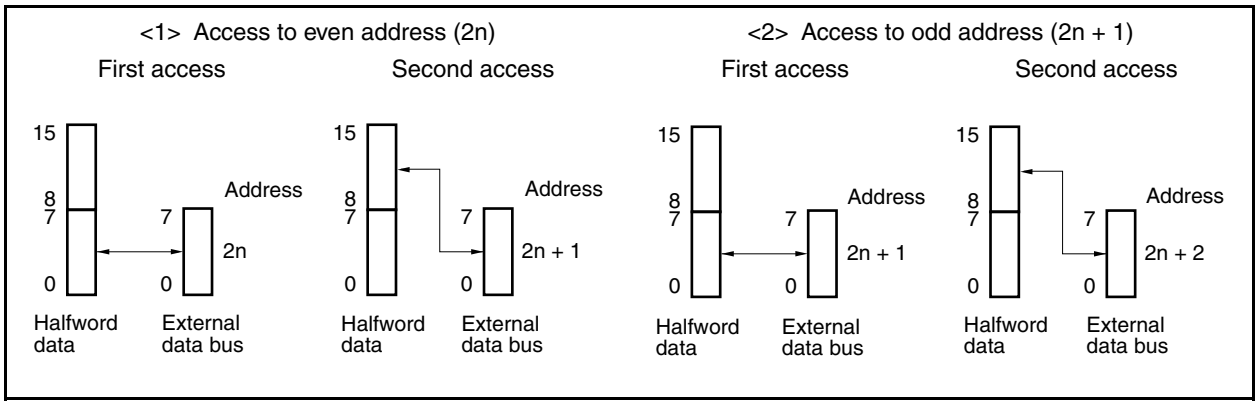
(a) 16-bit data bus width

16-bit data is transmitted/received via a 16-bit bus. Therefore, if an even address is specified, the lower and higher bytes of the external data bus address are accessed at the same time. If an odd address is specified, the lower byte of the data is transmitted/received to/from an odd address via the higher byte of the external data bus address in the first access. In the second access, the higher byte of the data is transmitted/received to/from an odd address via the lower byte of the external data bus address.



(b) 8-bit data bus width

16-bit data is transmitted/received via an 8-bit bus. Therefore, the data is transmitted/received in two accesses. The lower/higher byte of the data is transmitted/received to/from the corresponding lower/higher byte of the external bus address.



(1) TMPn control register 0 (TPnCTL0)

The TPnCTL0 register is an 8-bit register that controls the operation of TMPn.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

The same value can always be written to the TPnCTL0 register by software.

After reset: 00H R/W Address: TP0CTL0 FFFFF590H, TP1CTL0 FFFFF5A0H, TP2CTL0 FFFFF5B0H, TP3CTL0 FFFFF5C0H, TP4CTL0 FFFFF5D0H, TP5CTL0 FFFFF5E0H

TPnCTL0 (n = 0 to 5)

<7>	6	5	4	3	2	1	0
TPnCE	0	0	0	0	TPnCKS2	TPnCKS1	TPnCKS0

TPnCE	TMPn operation control
0	TMPn operation disabled (TMPn reset asynchronously[Note]).
1	TMPn operation enabled. TMPn operation started.

TPnCKS2	TPnCKS1	TPnCKS0	Internal count clock selection	
			n = 0, 2, 4	n = 1, 3, 5
0	0	0	f_{XX}	
0	0	1	$f_{XX}/2$	
0	1	0	$f_{XX}/4$	
0	1	1	$f_{XX}/8$	
1	0	0	$f_{XX}/16$	
1	0	1	$f_{XX}/32$	
1	1	0	$f_{XX}/64$	$f_{XX}/256$
1	1	1	$f_{XX}/128$	$f_{XX}/512$

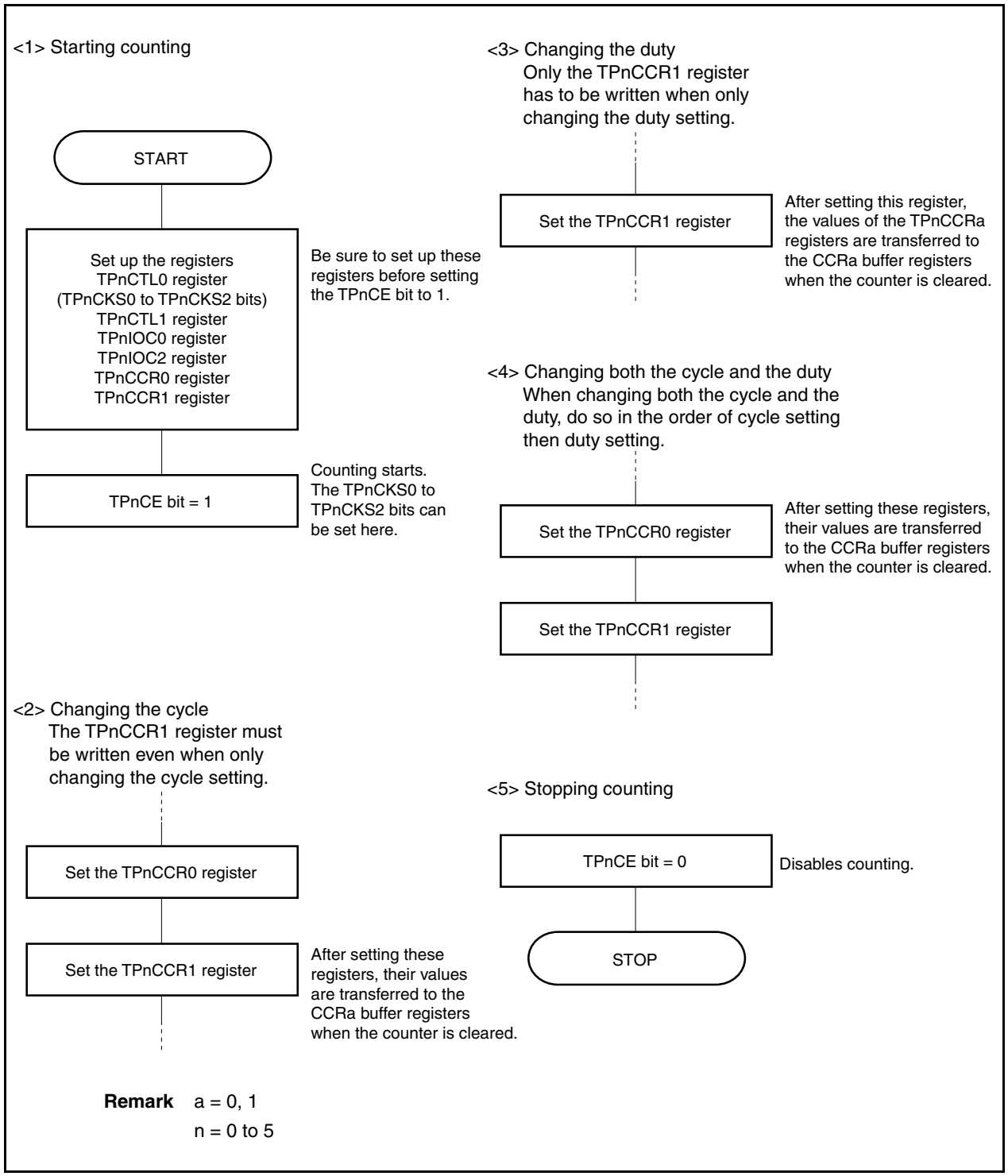
Note TPnOPT0.TPnOVF bit, 16-bit counter, timer output (TOPn0, TOPn1 pins)

Cautions 1. Set the TPnCKS2 to TPnCKS0 bits when the TPnCE bit = 0. When the value of the TPnCE bit is changed from 0 to 1, the TPnCKS2 to TPnCKS0 bits can be set simultaneously.

2. Be sure to clear bits 3 to 6 to "0".

Remark f_{XX}: Main clock frequency

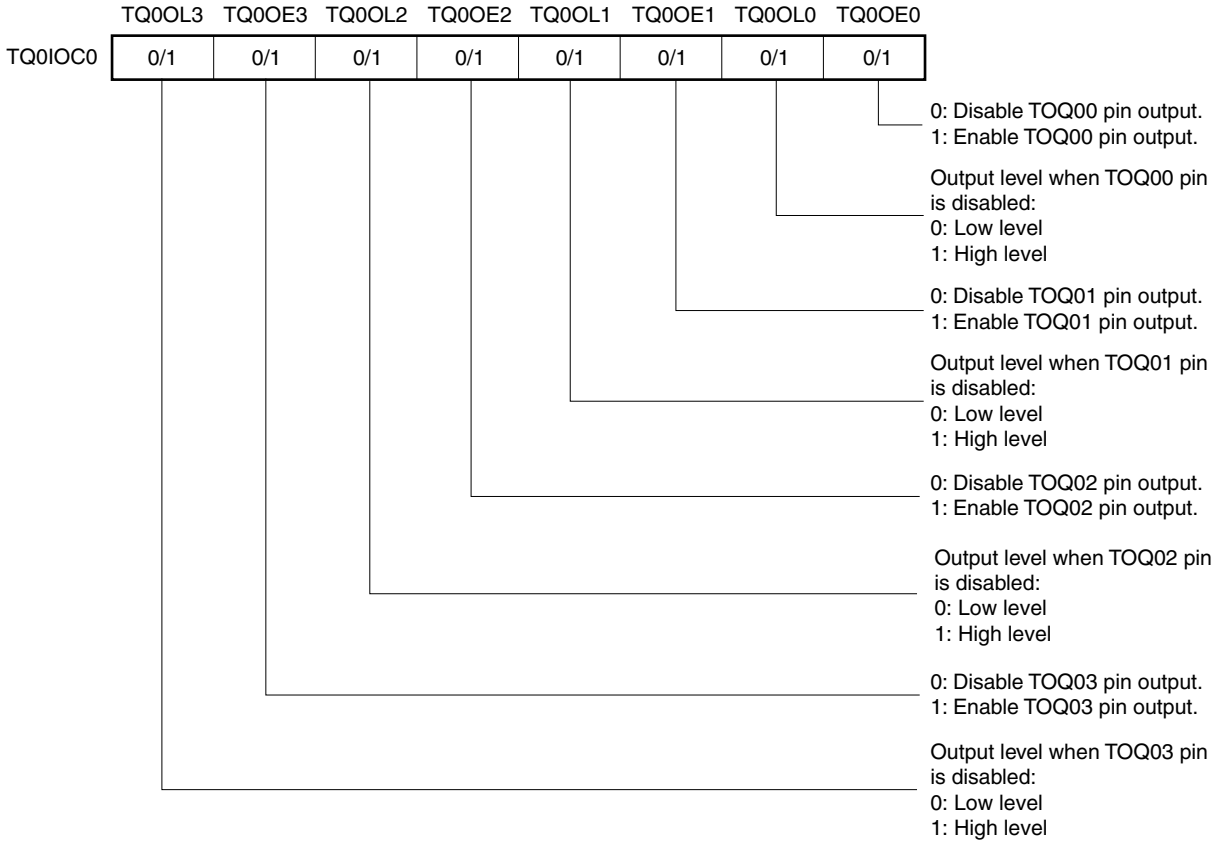
Figure 7-47. Timing and Processing of Operations in PWM Output Mode (2/2)



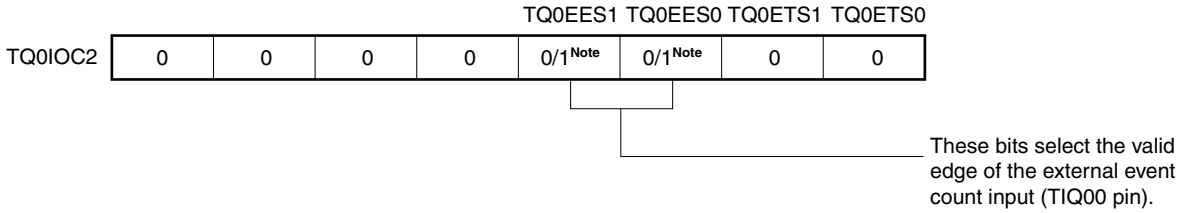
Remark a = 0, 1
n = 0 to 5

Figure 8-8. Register Settings in Interval Timer Mode (2/3)

(c) TMQ0 I/O control register 0 (TQ0IOC0)



(d) TMQ0 I/O control register 2 (TQ0IOC2)



Note The TQ0EES1 and TQ0EES0 bits can only be set to 1 when the timer output (TOQ01 to TOQ03) is used. Note that when setting these bits to 1, the TQ0CCR0 to TQ0CCR3 registers must be set to the same value (that is, the same value as the value already specified for these registers).

(e) TMQ0 counter read buffer register (TQ0CNT)

The value of the 16-bit counter can be read by reading this register.

(f) TMQ0 capture/compare register 0 (TQ0CCR0)

If the TQ0CCR0 register is set to D_0, the interval is as follows:

Interval = $(D_0 + 1) \times$ Count clock cycle

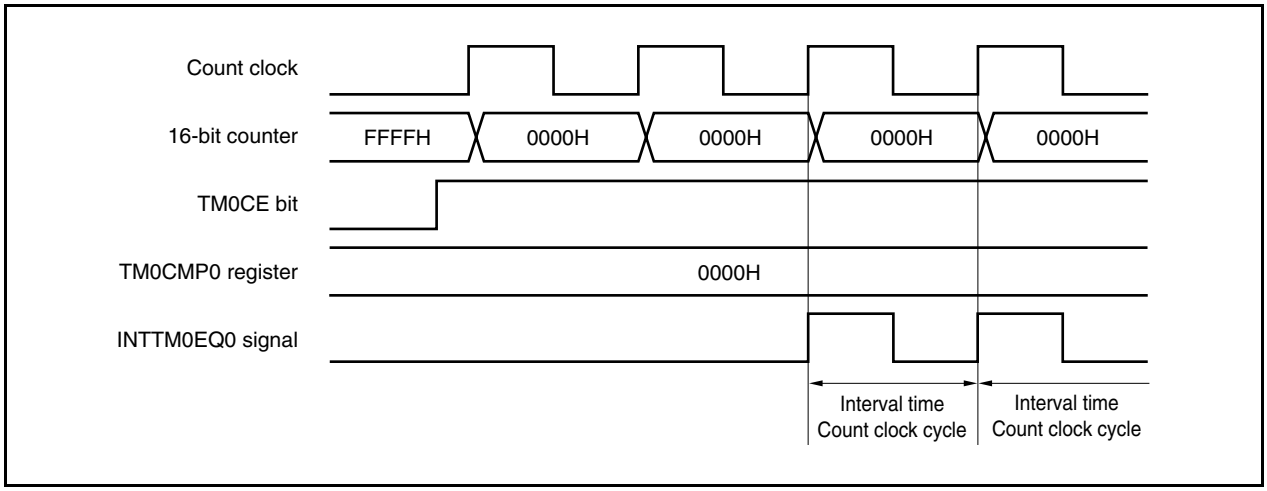
(2) Using interval timer mode

(a) Operation when TM0CMP0 register is set to 0000H

When the TM0CMP0 register is set to 0000H, the INTTM0EQ0 signal is generated for each count clock cycle.

The value of the 16-bit counter is always 0000H.

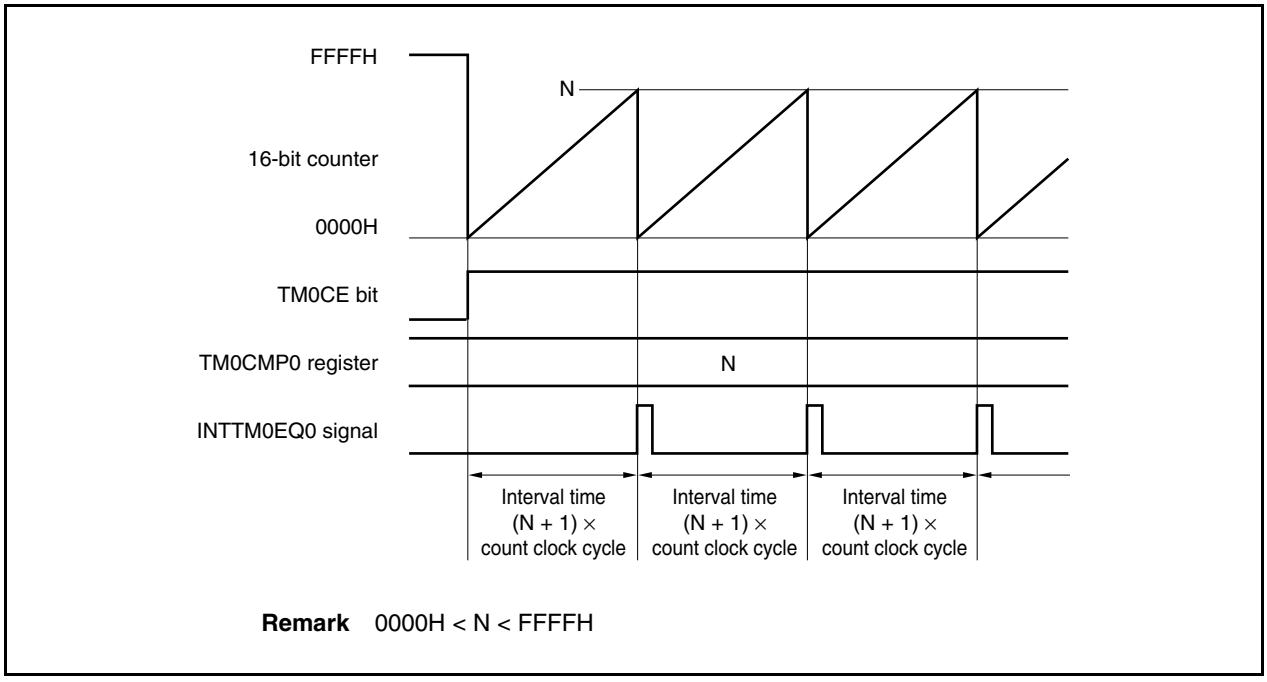
Figure 9-6. Operation of Interval Timer When TM0CMP0 Register Is Set to 0000H



(b) Operation when TM0CMP0 register is set to *N*

When the TM0CMP0 register is set to *N*, the 16-bit counter increments up to *N* and is reset to 0000H in synchronization with the next increment timing. The INTTM0EQ0 signal is then generated.

Figure 9-7. Operation of Interval Timer When TM0CMP0 Register is Set to Other Than 0000H, FFFFH



Remark 0000H < N < FFFFH

CHAPTER 10 WATCH TIMER

10.1 Functions

The watch timer has the following functions.

- Watch timer: An interrupt request signal (INTWT) is generated at intervals of 0.5 or 0.25 seconds by using the main clock or subclock.
- Interval timer: An interrupt request signal (INTWTI) is generated at set intervals.

The watch timer and interval timer functions can be used at the same time.

Caution INTWTI interrupt of the watch timer and INTRTC2 interrupt of RTC, and INTWT interrupt of the watch timer and INTRTC0 interrupt of RTC are alternate interrupt signals, and therefore cannot be used simultaneously. (μPD70F3792, 70F3793 only.)

16.3.3 UARTA2 and I²C00 mode switching

In the V850ES/JG3-L, UARTA2 and I²C00 share pins and therefore cannot be used simultaneously. To use the UARTA2 function, specify the UARTA2 mode in advance by using the PMC3 and PFC3 registers.

Switching the operation mode between UARTA2 and I²C00 are described below.

Caution Transmission and reception by UARTA2 and I²C00 are not guaranteed if these operation modes are switched during transmission or reception. Be sure to stop the serial interface that is not being used.

Figure 16-4. Switching UARTA2 and I²C00 Operation Modes

After reset: 0000H R/W Address: FFFFF446H, FFFFF447H

	15	14	13	12	11	10	9	8
PMC3	0	0	0	0	0	0	PMC39	PMC38

7	6	5	4	3	2	1	0
0	0	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30

After reset: 0000H R/W Address: FFFFF466H, FFFFF467H

	15	14	13	12	11	10	9	8
PFC3	0	0	0	0	0	0	PFC39	PFC38

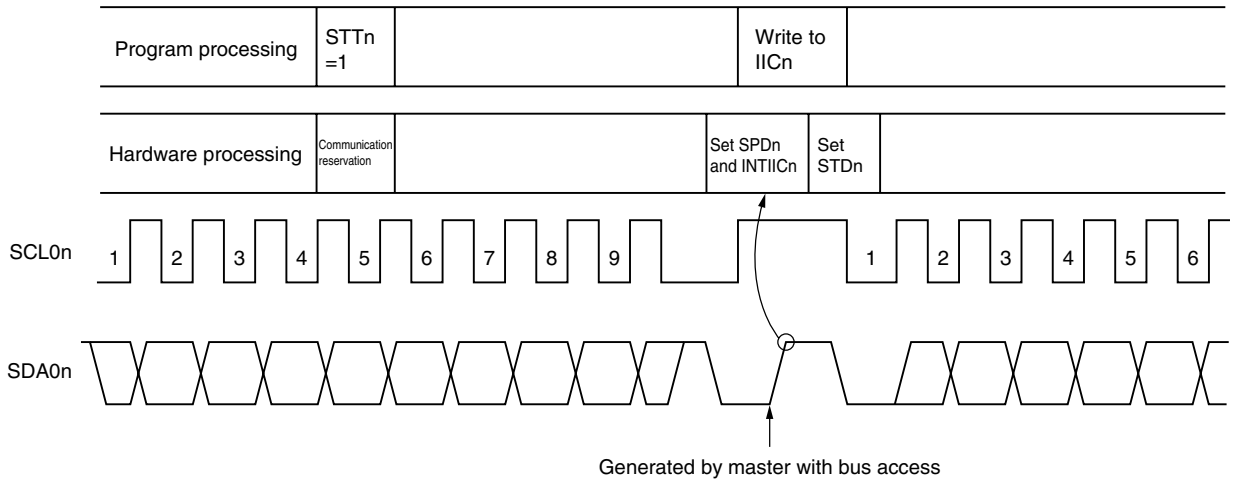
7	6	5	4	3	2	1	0
0	0	PFC35	PFC34	PFC33	PFC32	PFC31	PFC30

PMC3n	PFC3n	Operation mode
0	×	Port I/O mode
1	0	UARTA2 mode
1	1	I²C00 mode

Remarks 1. n = 8, 9

2. × = don't care

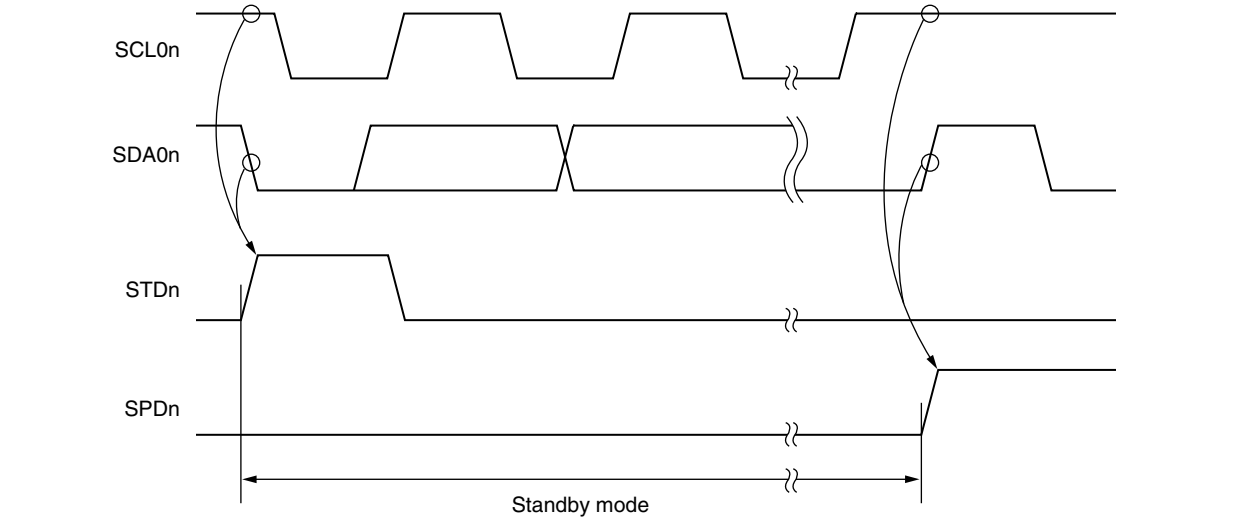
Figure 19-15. Communication Reservation Timing



Remark n = 0 to 2
STTn: Bit of IICCn register
STDn: Bit of IICSn register
SPDn: Bit of IICSn register

Communication reservations are accepted at the following timing. After the IICSn.STDn bit is set to 1, a communication reservation can be made by setting the IICCn.STTn bit to 1 before a stop condition is detected (n = 0 to 2).

Figure 19-16. Timing for Accepting Communication Reservations

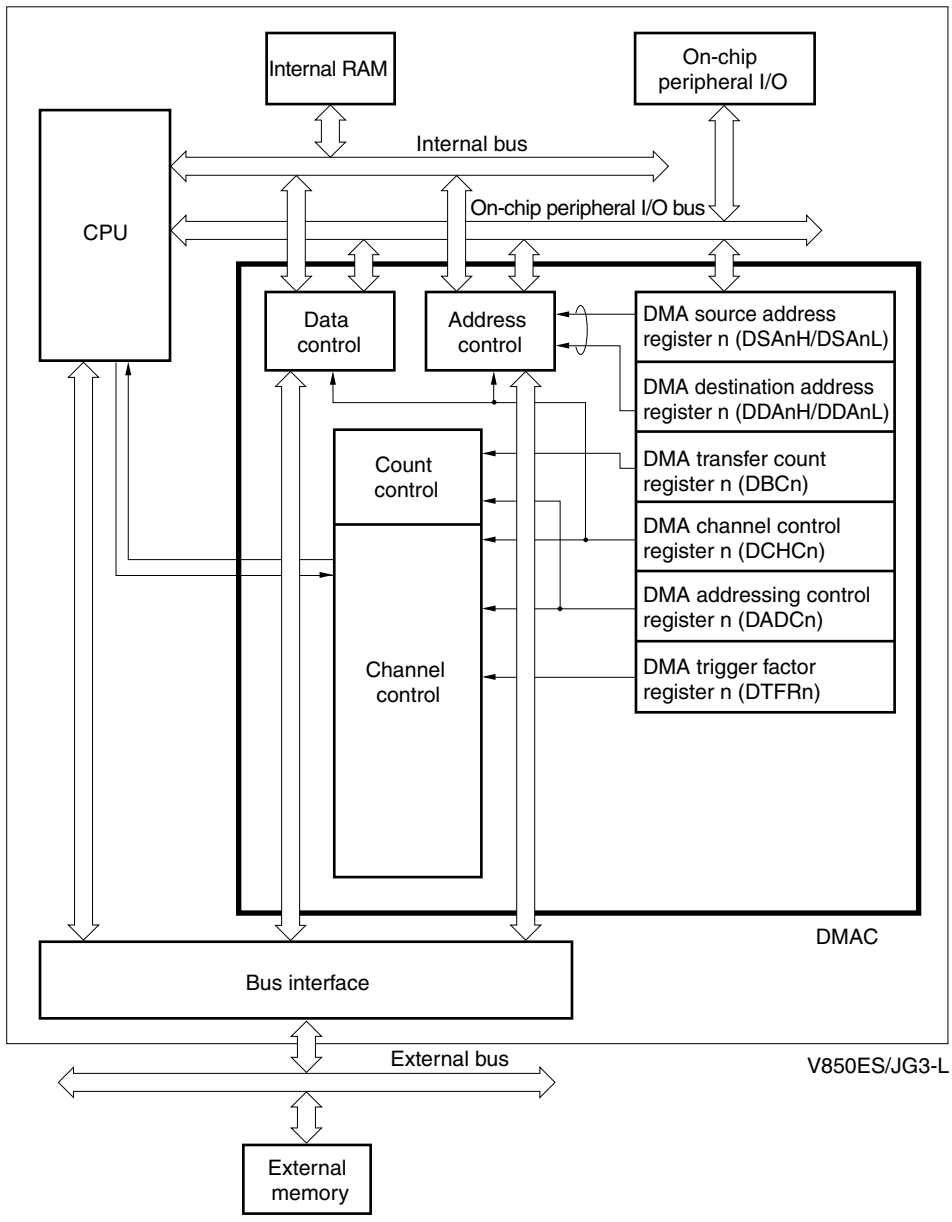


Remark n = 0 to 2

20.2 Configuration

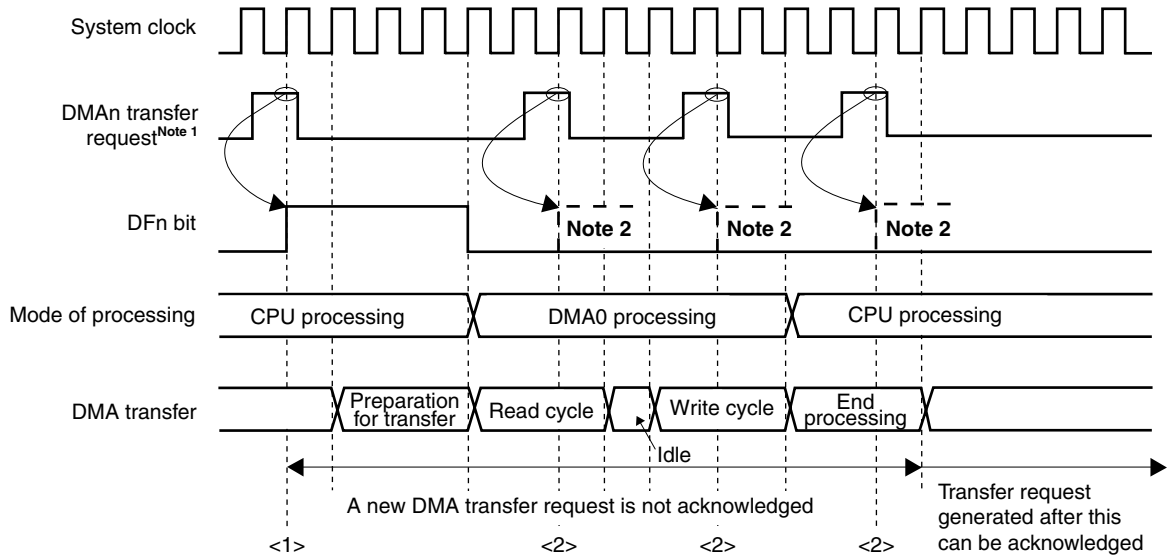
The block diagram of the DMAC is shown below.

Figure 20-1. Block Diagram of DMAC



Remark n = 0 to 3

Figure 20-6. Period in Which DMA Transfer Request Is Ignored (1)



<1> When a DMA transfer request is generated, the corresponding DF bit is set (1).

<2> A new DMA transfer request is ignored because the preceding transfer is not complete.

Notes 1. Interrupt from on-chip peripheral I/O, or software trigger (DCHCn.STGn bit)

2. A new DMA request for the same channel is ignored between when the transfer request is generated and the end processing.

Remark In the case of transfer between external memory spaces (multiplexed bus, no wait)

27.3 Registers

(1) CRC input register (CRCIN)

The CRCIN register is an 8-bit register for setting data.

This register can be read or written in 8-bit units.

Reset sets this register to 00H.

After reset: 00H R/W Address: FFFFF310H

	7	6	5	4	3	2	1	0
CRCIN								

(2) CRC data register (CRCD)

The CRCD register is a 16-bit register that stores the CRC-CCITT operation results.

This register can be read or written in 16-bit units.

Reset sets this register to 0000H.

Caution Accessing the CRCD register is prohibited in the following statuses. If a wait cycle is generated, it can only be cleared by a reset. For details, see 3.4.9 (1) Accessing specific on-chip peripheral I/O registers.

- **When the CPU operates on the subclock and main clock oscillation is stopped**
- **When the CPU operates on the internal oscillator clock**

After reset: 0000H R/W Address: FFFFF312H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCD																

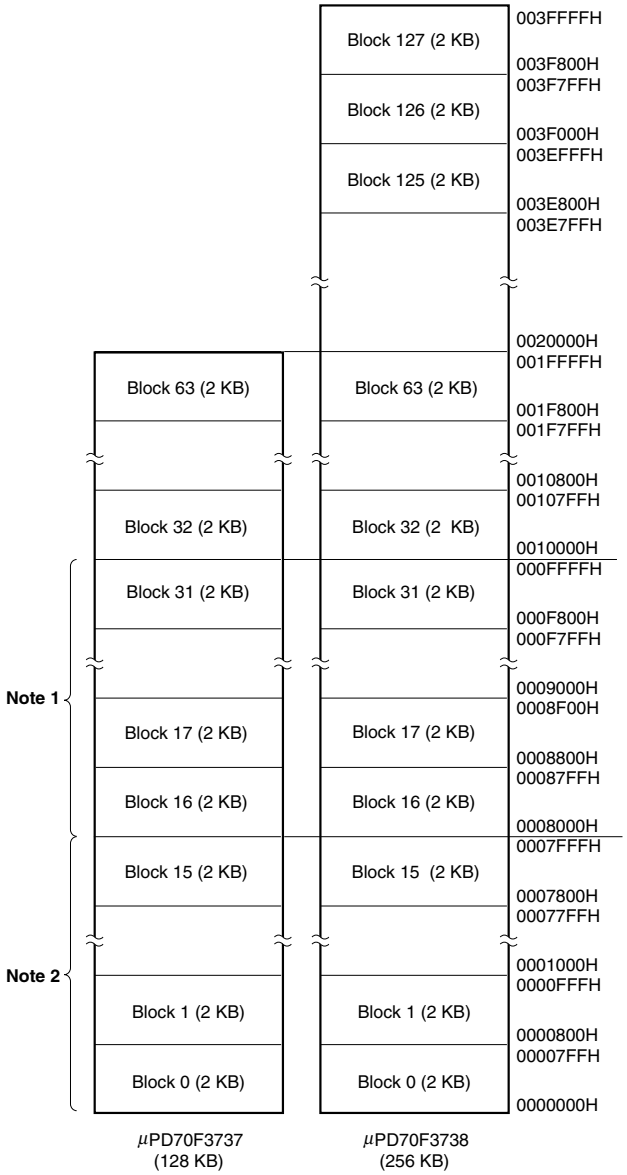
30.2 Memory Configuration

The V850ES/JG3-L internal flash memory area is divided into 64 or 96 or 128 blocks and can be erased in block units. All the blocks can also be erased at once.

When the boot swap function is used, the physical memory located at the addresses of blocks 0 to 15 is replaced by the physical memory located at the addresses of blocks 16 to 31. For details of the boot swap function, see **30.5 Rewriting by Self Programming**.

Figure 30-1. Flash Memory Mapping (1/2)

(a) μPD70F3737, 70F3738



Notes 1. Area to be replaced with the boot area by the boot swap function

2. Boot area

31.1.5 Operation

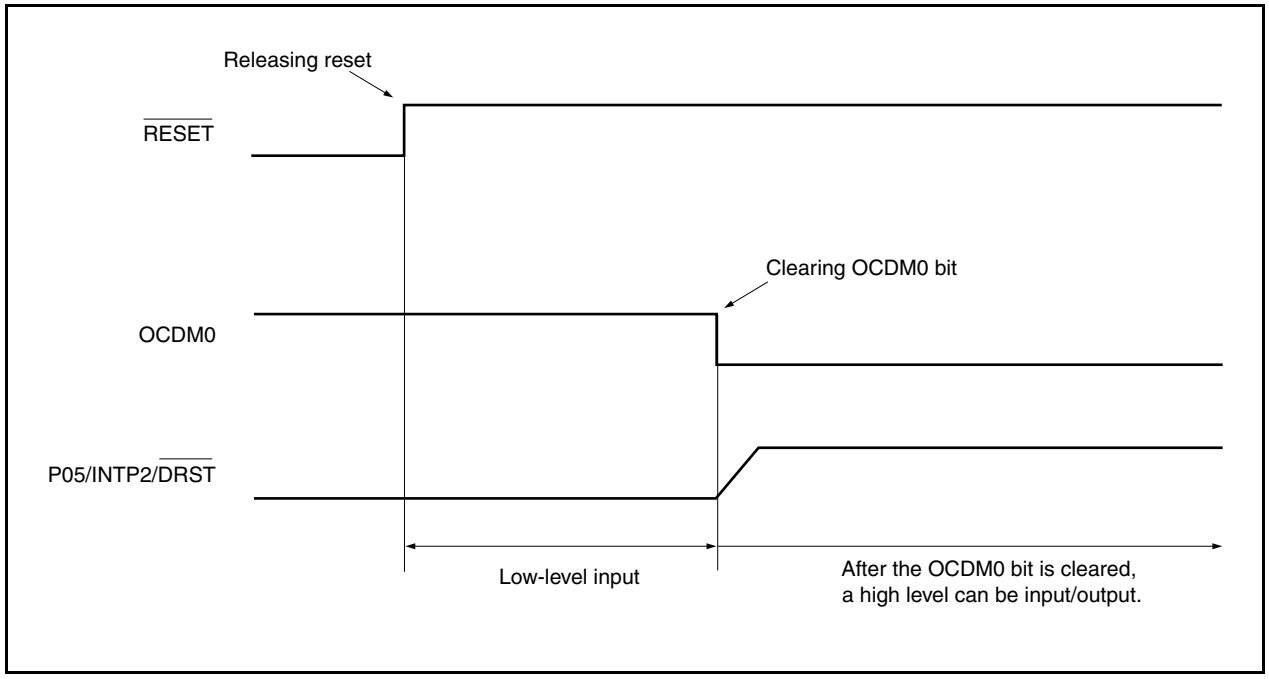
The on-chip debug function is made invalid under the conditions shown in the table below.

When this function is not used, keep the $\overline{\text{DRST}}$ pin low until the OCDM.OCDM0 flag is cleared to 0.

OCDM0 Flag / $\overline{\text{DRST}}$ Pin	0	1
L	Invalid	Invalid
H	Invalid	Valid

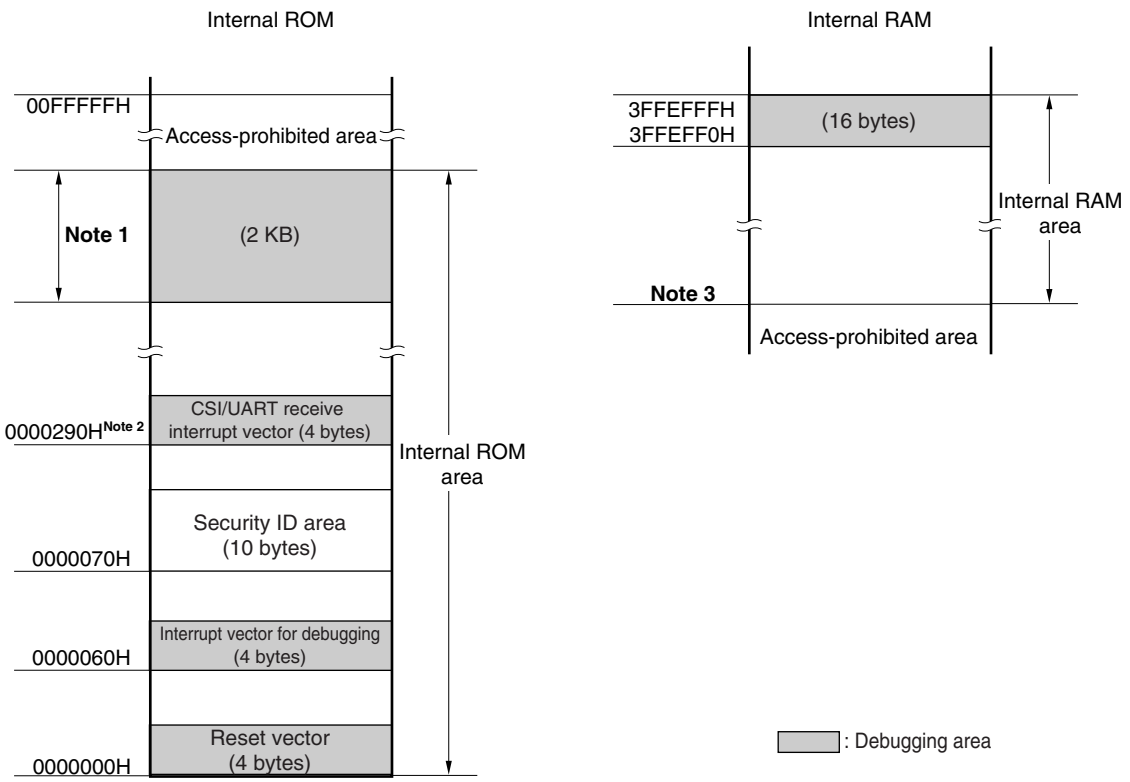
Remark L: Low-level input
H: High-level input

Figure 31-3. Timing When On-Chip Debug Function Is Not Used



<R>

Figure 31-5. Memory Spaces Where Debug Monitor Programs Are Allocated



Notes 1. The address values vary depending on the product.

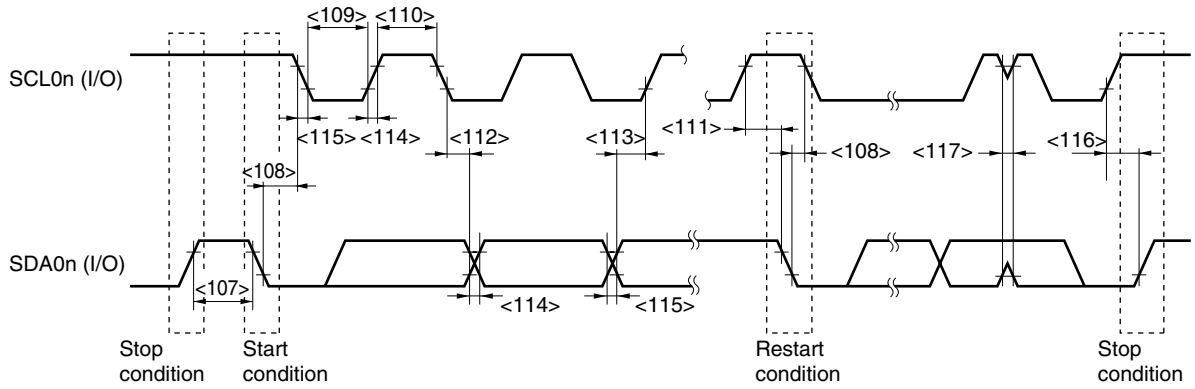
	Internal ROM Size	Address Value
μPD70F3737	128 KB	001F800H to 001FFFFH
μPD70F3738	256 KB	003F800H to 003FFFFH
μPD70F3792	384 KB	005F800H to 005FFFFH
μPD70F3793	512 KB	007F800H to 007FFFFH

2. This is the address when CSIB0 is used. This value is 00002F0H when CSIB3 is used, and 0000310H when UARTA0 is used.

3. The address values vary depending on the product.

	Internal RAM Size	Address Value
μPD70F3737	8 KB	3FFD000H
μPD70F3738	16 KB	3FFB000H
μPD70F3792	32 KB	3FF7000H
μPD70F3793	40 KB	3FF5000H

I²C Bus Timing



Remark n = 0 to 2

33.8.7 A/D converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, 2.7 V ≤ AV_{REF0} = AV_{REF1} ≤ 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		2.7 V ≤ AV_{REF0} ≤ 3.6 V			±0.6	%FSR
A/D conversion time	t_{CONV}	3.0 V ≤ AV_{REF0} ≤ 3.6 V	2.6		24	μs
		2.7 V ≤ AV_{REF0} ≤ 3.0 V	3.9		24	μs
Zero scale error					±0.5	%FSR
Full scale error					±0.5	%FSR
Non-linearity error					±4.0	LSB
Differential linearity error					±4.0	LSB
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		3.6	V
AV_{REF0} current	AI_{REF0}	Normal conversion mode		3	6.5	mA
		High-speed conversion mode		4	10	mA
		When A/D converter unused			5	μA

Note Excluding quantization error (±0.05 %FSR).

Caution Do not set (read/write) alternate-function ports during A/D conversion; otherwise the conversion resolution may be degraded.

Remark LSB: Least Significant Bit
FSR: Full Scale Range

Table B-3. Major Differences Between V850ES/JG3-L Products

Major Difference			μPD70F3792	μPD70F3793	μPD70F3737	μPD70F3738
Internal memory	Flash memory		384 KB	512 KB	128 KB	256 KB
	RAM		32 KB	40 KB	8 KB	16 KB
Port number			83		84	
Interrupt request signal	Interrupt number		64 (External interrupt : 9)		57 (External interrupt : 9)	
	RTC	INTRTC0	Available		None	
		INTRCT1	Available		None	
		INTRTC2	Available		None	
	UARTA3	INTTUA3R	Available		None	
		INTTUA3T	Available		None	
	UARTA4	INTTUA4R	Available		None	
		INTTUA4T	Available		None	
	UARTA5	INTTUA5R	Available		None	
		INTTUA5T	Available		None	
	UARTC1	INTTUC1R	Available		None	
		INTTUC1T	Available		None	
RTC			Available		None	
RTC backup mode			Available		None	
UARTA			6 channels		3 channels	
UARTC			Available		None	
DMA Start Factors	INTRTC1		Available		None	
	INTUA3R		Available		None	
	INTUA3T		Available		None	
	INTUA4R		Available		None	
	INTUA4T		Available		None	
	INTUA5R		Available		None	
	INTUA5T		Available		None	
LVI detection level			3 levels		2 levels	
Package	100-pinQFP (14x20)		None		Available	
Operation power supply voltage	2.0 to 3.6 V@2.5 MHz		Available		None	