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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-LFBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3793f1-cah-a

(19) DCU (debug control unit)

An on-chip debug function that uses the JTAG (Joint Test Action Group) communication specifications is provided. Switching between the normal port function and on-chip debugging function is done with the control pin input level and the OCDM register.

(20) Ports

The following general-purpose port functions and control pin functions are available.

<R>

Table 1-2. Port Functions

Port	I/O	Alternate Function
P0	5-bit I/O	NMI, external interrupt, A/D converter trigger, debug reset, Real time counter output Note 1
P1	2-bit I/O	D/A converter analog output
P3	10-bit I/O	External interrupt, serial interface, timer I/O
P4	3-bit I/O	Serial interface
P5	6-bit I/O	Timer I/O, real-time output, key interrupt input, serial interface, debug I/O
P7	12-bit I/O	A/D converter analog input
P9	16-bit I/O	External address bus, serial interface, key interrupt input, timer I/O, external interrupt
PCM	4-bit I/O	External control signal
PCT	4-bit I/O	External control signal
PDH	6-bit I/O Note 2, 5-bit I/O Note 1	External address bus
PDL	16-bit I/O	External address/data bus

Notes1. μPD70F3792, 70F3793 only

2. μPD70F3737, 70F3738 only

Note Five NOP instructions or more must be inserted immediately after setting the IDLE1 mode, IDLE2 mode, or STOP mode (by setting the PSC.STP bit to 1).

Caution When a store instruction is executed to store data in the command register, interrupts are not acknowledged. This is because it is assumed that steps <3> and <4> above are performed by successive store instructions. If another instruction is placed between <3> and <4>, and if an interrupt is acknowledged by that instruction, the above sequence may not be established, causing malfunction.

Remark Although dummy data is written to the PRCMD register, use the same general-purpose register used to set the special register (<4> in the example) to write data to the PRCMD register (<3> in the example). The same applies when a general-purpose register is used for addressing.

(2) Command register (PRCMD)

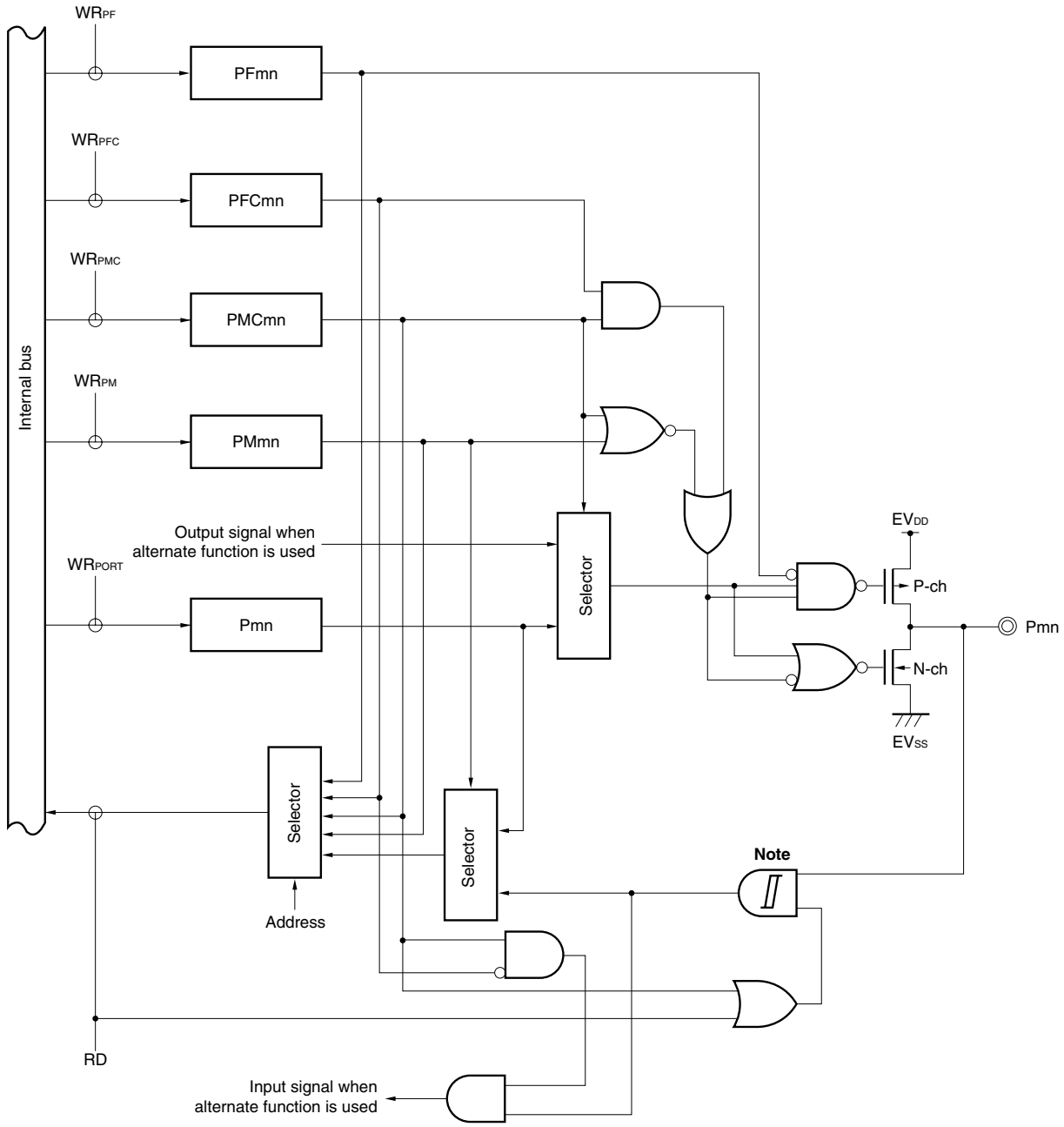
The PRCMD register is an 8-bit register that protects the registers that may seriously affect the application system from being written, so that the system does not inadvertently stop due to a program hang-up. The first write access to a special register is valid after data has been written in advance to the PRCMD register. In this way, the value of the special register can be rewritten only in a specific sequence, so as to protect the register from an illegal write access.

The PRCMD register is write-only, in 8-bit units (undefined data is read when this register is read).

After reset: Undefined W Address: FFFFF1FCH

	7	6	5	4	3	2	1	0
PRCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

Figure 4-10. Block Diagram of Type G-1



Note There are no hysteresis characteristics in port mode.

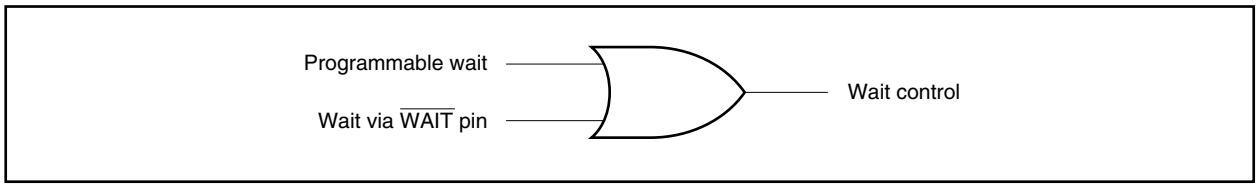
Table 4-15. Settings When Pins Are Used for Alternate Functions (2/7)

Function Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCEnx Bit of PFCEn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Name	I/O						
P34	TIP10	Input	P34 = Setting not required	PM34 = Setting not required	PMC34 = 1	–	PFC34 = 0	
	TOP10	Output	P34 = Setting not required	PM34 = Setting not required	PMC34 = 1	–	PFC34 = 1	
P35	TIP11	Input	P35 = Setting not required	PM35 = Setting not required	PMC35 = 1	–	PFC35 = 0	
	TOP11	Output	P35 = Setting not required	PM35 = Setting not required	PMC35 = 1	–	PFC35 = 1	
P36	TXDA3[Note]	Outpt	P36 = Setting not required	PM36 = Setting not required	PMC36 = 1	–	–	
P37	RXDA3[Note]	Input	P37 = Setting not required	PM37 = Setting not required	PMC37 = 1	–	–	
P38	TXDA2	Output	P38 = Setting not required	PM38 = Setting not required	PMC38 = 1	–	PFC38 = 0	
	SDA00	I/O	P38 = Setting not required	PM38 = Setting not required	PMC38 = 1	–	PFC38 = 1	PF38 (PF3) = 1
P39	RXDA2	Input	P39 = Setting not required	PM39 = Setting not required	PMC39 = 1	–	PFC39 = 0	
	SCL00	I/O	P39 = Setting not required	PM39 = Setting not required	PMC39 = 1	–	PFC39 = 1	PF39 (PF3) = 1
P40	SIB0	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	–	PFC40 = 0	
	SDA01	I/O	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	–	PFC40 = 1	PF40 (PF4) = 1
P41	$\overline{\text{SOB0}}$	Output	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PFC41 = 0	
	SCL01	I/O	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PFC41 = 1	PF41 (PF4) = 1
P42	SCKB0	I/O	P42 = Setting not required	PM42 = Setting not required	PMC42 = 1	–	–	
P50	TIQ01	Input	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFCE50 = 0	PFC50 = 1	KRM0 (KRM) = 0
	KR0	Input	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFCE50 = 0	PFC50 = 1	TQ0TIG2, TQ0TIG3 (TQ0IOC1) = 0
	TOQ01	Output	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFCE50 = 1	PFC50 = 0	
	RTP00	Output	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFCE50 = 1	PFC50 = 1	

Note. μPD70F3792, 70F3793 only

5.6.3 Relationship between programmable wait and external wait

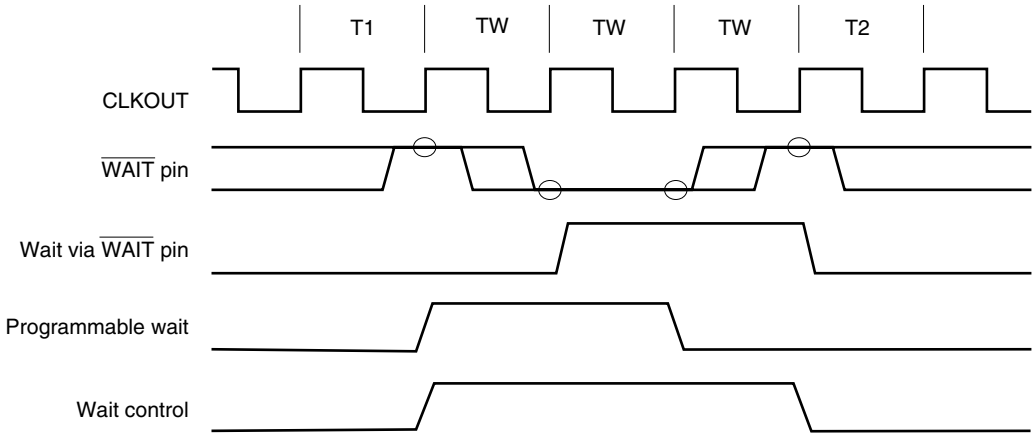
Wait cycles are inserted as the result of an OR operation between the wait cycles specified by the set programmable wait value and the wait cycles controlled by the $\overline{\text{WAIT}}$ pin.



For example, if the timing of the programmable wait and the $\overline{\text{WAIT}}$ pin signal is as shown in the Figure 5-3, three wait states will be inserted in the bus cycle. If wait insertion is controlled by the $\overline{\text{WAIT}}$ pin, wait states might not be inserted at the expected timing. In this case, adjust the insertion timing by specifying a programmable wait value.

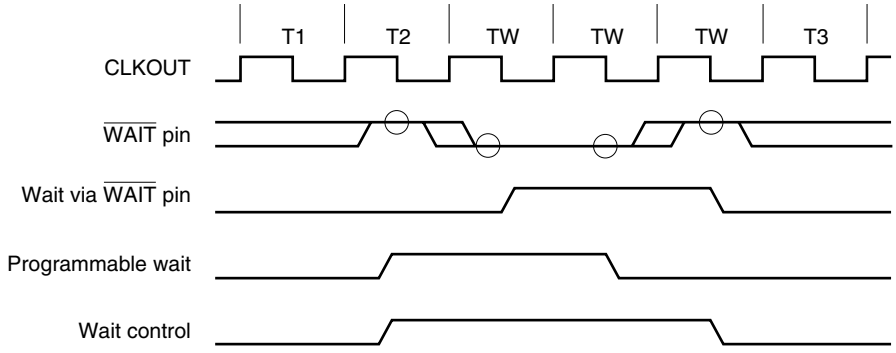
Figure 5-3. Example of Inserting Wait States

(a) In separate bus mode



Remark The circles indicate the sampling timing.

(b) In multiplexed bus mode



Remark The circles indicate the sampling timing.

5.8 Bus Hold Function

5.8.1 Functional outline

The $\overline{\text{HLDRQ}}$ and $\overline{\text{HLDAK}}$ signals are valid if the PCM2 and PCM3 pins are set to the control mode.

When the $\overline{\text{HLDRQ}}$ signal is asserted (low level), indicating that another bus master has requested bus mastership, the external address/data bus goes into a high-impedance state, the $\overline{\text{HLDAK}}$ signal is asserted (low level), and the bus is released (bus hold status). If the request for the bus mastership is cleared and the $\overline{\text{HLDRQ}}$ signal is deasserted (high level), driving these signals is started again.

During the bus hold period, the CPU continues executing the program in the internal ROM and internal RAM until an on-chip peripheral I/O register or the external memory is accessed.

The bus hold function enables the configuration of multi-processor type systems in which two or more bus masters exist.

Note that a bus hold request is not acknowledged during a multiple-access cycle initiated by the bus sizing function or a bit manipulation instruction. The timing at which a bus hold request is not acknowledged is shown below.

Table 5-6. Timing at Which Bus Hold Request Is Not Acknowledged

Status	Data Bus Width	Access Type	Timing at Which Bus Hold Request Is Not Acknowledged
CPU bus lock	16 bits	Word access to even address	Between first and second access
		Word access to odd address	Between first and second access
			Between second and third access
		Halfword access to odd address	Between first and second access
	8 bits	Word access	Between first and second access
			Between second and third access
			Between third and fourth access
		Halfword access	Between first and second access
Read-modify-write access by bit manipulation instruction	–	–	Between read access and write access

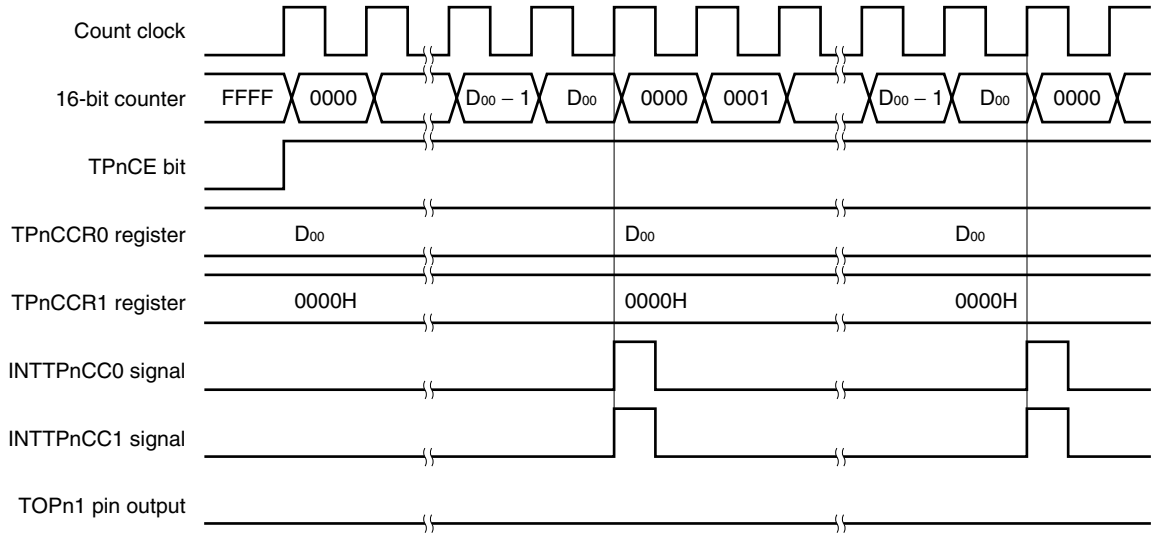
Caution To rewrite the TPnCCR0 or TPnCCR1 register after writing the TPnCCR1 register, do so after the INTTPnCC0 signal has been generated; otherwise, the value of the CCRa buffer register may become undefined because the timing of transferring data from the TPnCCRa register to the CCRa buffer register conflicts with writing the TPnCCRa register.

Remark a = 0, 1
n = 0 to 5

(b) Outputting a 0% or 100% PWM waveform

To output a 0% waveform, clear the TPnCCR1 register to 0000H.

Figure 7-49. Outputting 0% PWM Waveform



Remark n = 0 to 5

(2) Using external trigger pulse output mode

How to change the PWM waveform in the external trigger pulse output mode is described below.

(a) Changing the PWM waveform while the counter is incrementing

To change the PWM waveform while the counter is incrementing, write to the TQ0CCR1 register after changing the waveform setting. When rewriting the TQ0CCRk register after writing to the TQ0CCR1 register, do so after the INTTQ0CC0 signal has been detected.

(3) DEV bit

The DEV bit determines when the setting by the F6 to F0 bits is enabled.

The value set by the F6 to F0 bits is reflected upon the next timing, but not to the RC1SUBC count value every time.

Table 11-6. DVE Bit Setting

DEV Bit Value	Timing of Reflecting Value to RC1SUBC
0	When RC1SEC is 00, 20, or 40 seconds.
1	When RC1SEC is 00 seconds.

[Example when 0010101B is set to F6 to F0 bits]

- If the DEV bit is 0

  The RC1SUBC count value is 32,808 at 00, 20, or 40 seconds.

  Otherwise, it is 32,768.

- IF DEV bit is 1

  The RC1SUBC count value is 32,808 at 00 seconds.

  Otherwise, it is 32,768.

As described above, the RC1SUBC count value is corrected every 20 seconds or 60 seconds, instead of every second, in order to match the RC1SUBC count value with the deviation width of the resonator.

The range in which the resonator frequency can be actually corrected is shown below.

- If the DEV bit is 0: 32.76180000 kHz to 32.77420000 kHz
- If the DEV bit is 1: 32.76593333 kHz to 32.77006667 kHz

The range in which the frequency can be corrected when the DEV bit is 0 is three times wider than when the DEV bit is 1.

However, the accuracy of setting the frequency when the DEV bit is 1 is three times that when the DEV bit is 0.

Tables 11-7 and 11-8 show the setting values of the DEV, and F6 to F0 bits, and the corresponding frequencies that can be corrected.

Table 11-7. Range of Frequencies That Can Be Corrected When DEV Bit = 0

F6	F5 to F0	RC1SUBC Correction Value	Frequency of Connected Clock (Including Steady-State Deviation)
0	000000	No correction	–
0	000001	No correction	–
0	000010	Increments RC1SUBC count value by 2 once every 20 seconds	32.76810000 kHz
0	000011	Increments RC1SUBC count value by 4 once every 20 seconds	32.76820000 kHz
0	000100	Increments RC1SUBC count value by 6 once every 20 seconds	32.76830000 kHz
		⋮	
0	111011	Increments RC1SUBC count value by 120 once every 20 seconds	32.77400000 kHz
0	111110	Increments RC1SUBC count value by 122 once every 20 seconds	32.77410000 kHz
0	111111	Increments RC1SUBC count value by 124 once every 20 seconds	32.77420000 kHz (upper limit)
1	000000	No correction	–
1	000001	No correction	–
1	000010	Decrements RC1SUBC count value by 124 once every 20 seconds	32.76180000 kHz (lower limit)
1	000011	Decrements RC1SUBC count value by 122 once every 20 seconds	32.76190000 kHz
1	000100	Decrements RC1SUBC count value by 120 once every 20 seconds	32.76200000 kHz
		⋮	
1	11011	Decrements RC1SUBC count value by 6 once every 20 seconds	32.76770000 kHz
1	11110	Decrements RC1SUBC count value by 4 once every 20 seconds	32.76780000 kHz
1	11111	Decrements RC1SUBC count value by 2 once every 20 seconds	32.76790000 kHz

Table 11-8. Range of Frequencies That Can Be Corrected When DEV Bit = 1

F6	F5 to F0	RC1SUBC Correction Value	Frequency of Connected Clock (Including Steady-State Deviation)
0	000000	No correction	–
0	000001	No correction	–
0	000010	Increments RC1SUBC count value by 2 once every 60 seconds	32.76803333 kHz
0	000011	Increments RC1SUBC count value by 4 once every 60 seconds	32.76806667 kHz
0	000100	Increments RC1SUBC count value by 6 once every 60 seconds	32.76810000 kHz
		⋮	
0	111011	Increments RC1SUBC count value by 120 once every 60 seconds	32.77000000 kHz
0	111110	Increments RC1SUBC count value by 122 once every 60 seconds	32.77003333 kHz
0	111111	Increments RC1SUBC count value by 124 once every 60 seconds	32.77006667 kHz (upper limit)
1	000000	No correction	–
1	000001	No correction	–
1	000010	Decrements RC1SUBC count value by 124 once every 60 seconds	32.76593333 kHz (lower limit)
1	000011	Decrements RC1SUBC count value by 122 once every 60 seconds	32.76596667 kHz
1	000100	Decrements RC1SUBC count value by 120 once every 60 seconds	32.76600000 kHz
		⋮	
1	11011	Decrements RC1SUBC count value by 6 once every 60 seconds	32.76790000 kHz
1	11110	Decrements RC1SUBC count value by 4 once every 60 seconds	32.76793333 kHz
1	11111	Decrements RC1SUBC count value by 2 once every 60 seconds	32.76796667 kHz

(1) ANI0 to ANI11 pins

These are analog input pins for the 12 A/D converter channels and are used to input analog signals to be converted into digital signals. Pins other than the ones selected as analog input pins by the ADA0S register can be used as I/O port pins.

Caution Make sure that the voltages input to the ANI0 to ANI11 pins do not exceed the rated values. In particular if a voltage of AV_{REF0} or higher is input to a channel, the conversion value of that channel becomes undefined, and the conversion values of the other channels may also be affected.

(2) Sample & hold circuit

The sample & hold circuit samples each of the analog input signals selected by the input circuit and sends the sampled data to the voltage comparator. This circuit also holds the sampled analog input signal voltage during A/D conversion.

(3) Compare voltage generation DAC

The compare voltage generation DAC is connected between AV_{REF0} and AV_{SS} and generates the voltage to be compared with the value that was sampled and held by the sample & hold circuit.

(4) Voltage comparator

The voltage comparator compares the voltage value that was sampled and held with the output voltage of the compare voltage generation DAC.

(5) Successive approximation register (SAR)

This register compares the voltage of the sampled analog input signal with the output voltage of the compare voltage generation DAC (compare voltage), and sequentially retains the comparison result bit by bit starting from the most significant bit (MSB).

When the comparison result has been held down to the least significant bit (LSB) (that is, when A/D conversion is complete), the contents of the SAR register are transferred to the ADA0CRn register.

Remark n = 0 to 11

(6) 10-bit AD conversion result register n (ADA0CRn)

The ADA0CRn register is a 16-bit register that stores the A/D conversion result. ADA0ARn consist of 12 registers and the A/D conversion result is stored in the 10 higher bits of the AD0CRn register corresponding to analog input. (The lower 6 bits are fixed to 0.)

(7) A/D conversion result register nH (ADA0CRnH)

This is a 8-bit register that stores the A/D conversion result. ADA0CRnH consists of 12 registers and the A/D conversion result is stored in the higher 8 bits of the ADA0CRnH register corresponding to the analog input signal.

(8) A/D converter mode register 0 (ADA0M0)

This register specifies the operation mode and controls conversion by the A/D converter.

(9) A/D converter mode register 1 (ADA0M1)

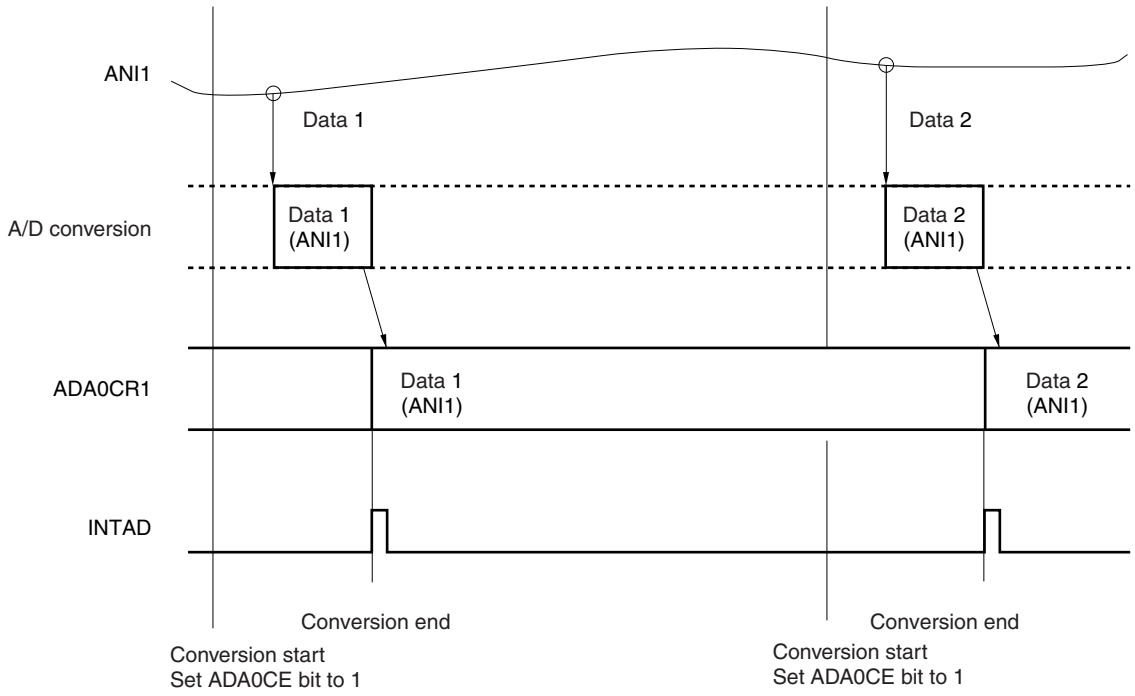
This register specifies the time required to convert an analog input signal to a digital signal.

(3) One-shot select mode

In this mode, the voltage of the analog input pin specified by the ADA0S register is converted into a digital value only once.

The conversion result is stored in the ADA0CRn register corresponding to the analog input pin. In this mode, an analog input pin and an ADA0CRn register correspond on a one-to-one basis. When A/D conversion has been completed once, the INTAD signal is generated. A/D conversion is stopped after it has been completed (n = 0 to 11).

Figure 14-6. Example of Timing in One-Shot Select Mode (ADA0S Register = 01H)



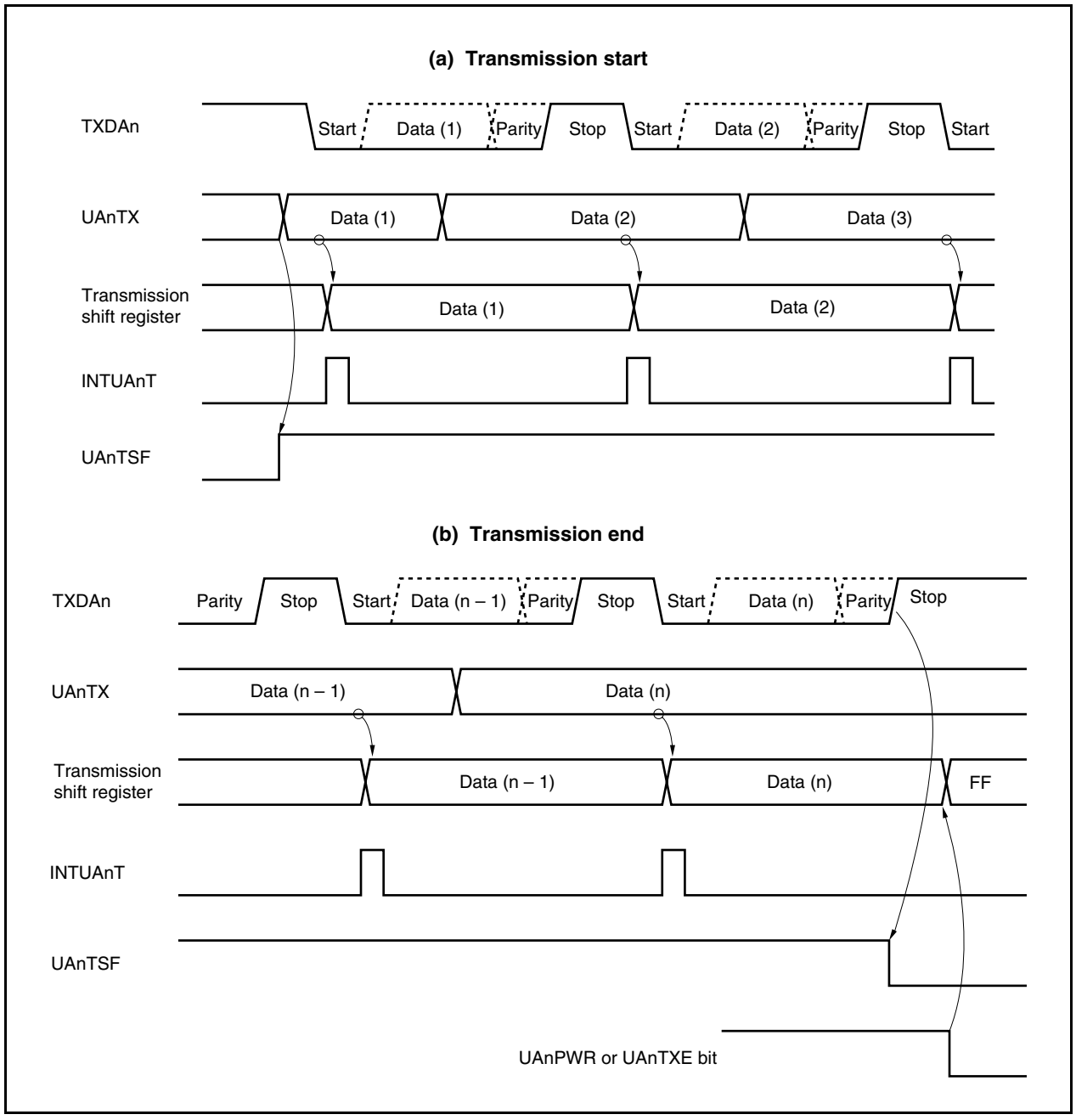
Remark The above timing applies to the software trigger mode (ADA0M0.AD0TMD bit = 0) or the high-speed conversion mode (ADA0M1.ADA0HS1 bit = 1).

(4) One-shot scan mode

In this mode, analog input pins are sequentially selected, from the ANI0 pin to the pin specified by the ADA0S register, and their values are converted into digital values .

Each conversion result is stored in the ADA0CRn register corresponding to the analog input pin. When conversion of the analog input pin specified by the ADA0S register is complete, the INTAD signal is generated. A/D conversion is stopped after it has been completed (n = 0 to 11).

Figure 16-8. Continuous Transmission Operation Timing



(9) Slave address registers 0 to 2 (SVA0 to SVA2)

The SVAn register holds the I²C bus's slave address.

These registers can be read or written in 8-bit units, but bit 0 should be fixed to 0. However, rewriting this register is prohibited when the IICSn.STDn bit = 1 (start condition detection).

Reset sets these registers to 00H.

After reset: 00H R/W Address: SVA0 FFFFFD83H, SVA1 FFFFFD93H, SVA2 FFFFFDA3H

	7	6	5	4	3	2	1	0
SVAn								0

(n = 0 to 2)

(4) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn bit = 0 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 Δ4

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X000B

▲3: IICSn register = 00000X10B

Δ 4: IICSn register = 00000001B

Remarks 1. ▲: Always generated

Δ: Generated only when SPIEn bit = 1

X: don't care

2. n = 0 to 2

<2> When WTIMn bit = 1 (after restart, address mismatch (= not extension code))

ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	ST	AD6 to AD0	R/$\overline{W}$	$\overline{ACK}$	D7 to D0	$\overline{ACK}$	SP

▲1 ▲2 ▲3 ▲4 Δ5

▲1: IICSn register = 0010X010B

▲2: IICSn register = 0010X110B

▲3: IICSn register = 0010XX00B

▲4: IICSn register = 00000X10B

Δ 5: IICSn register = 00000001B

Remarks 1. ▲: Always generated

Δ: Generated only when SPIEn bit = 1

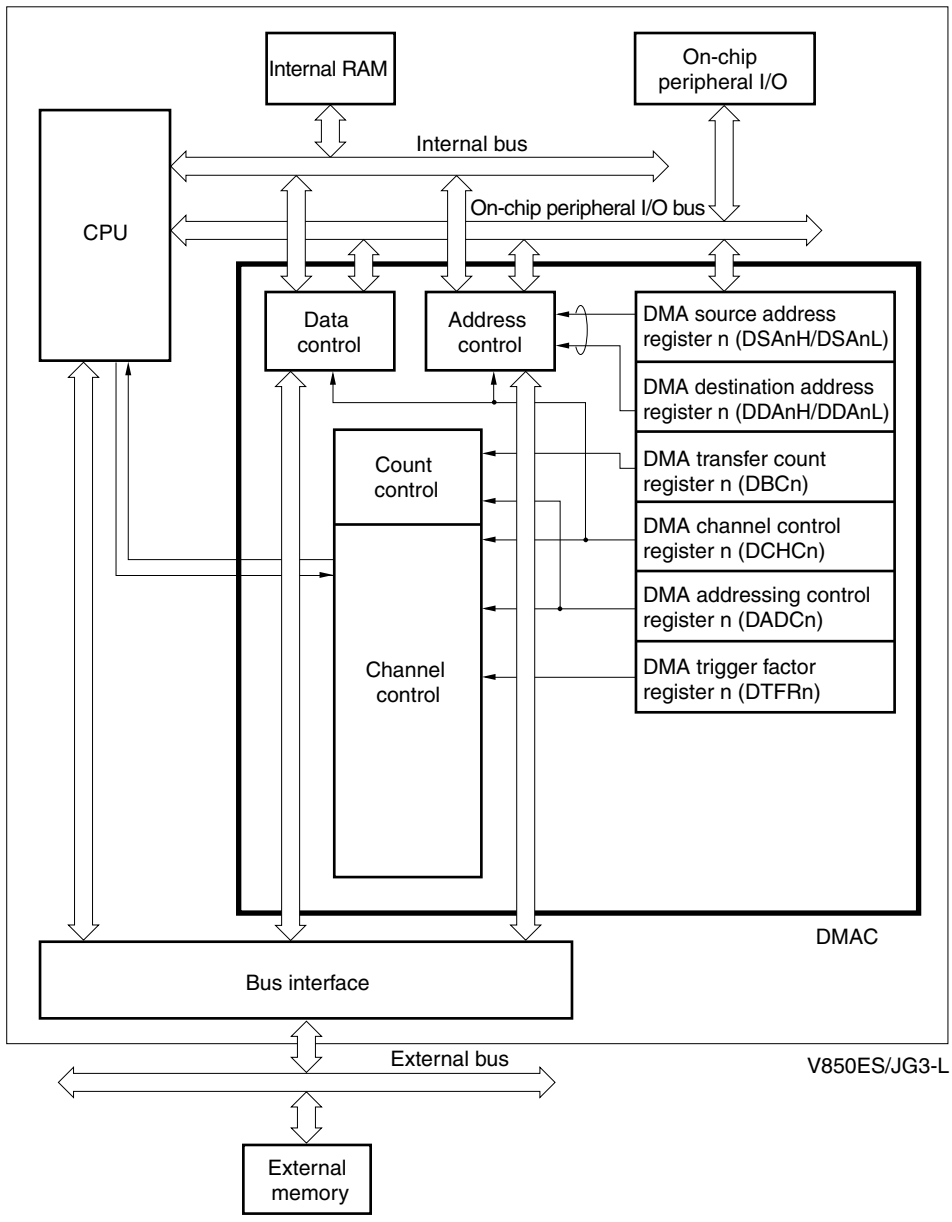
X: don't care

2. n = 0 to 2

20.2 Configuration

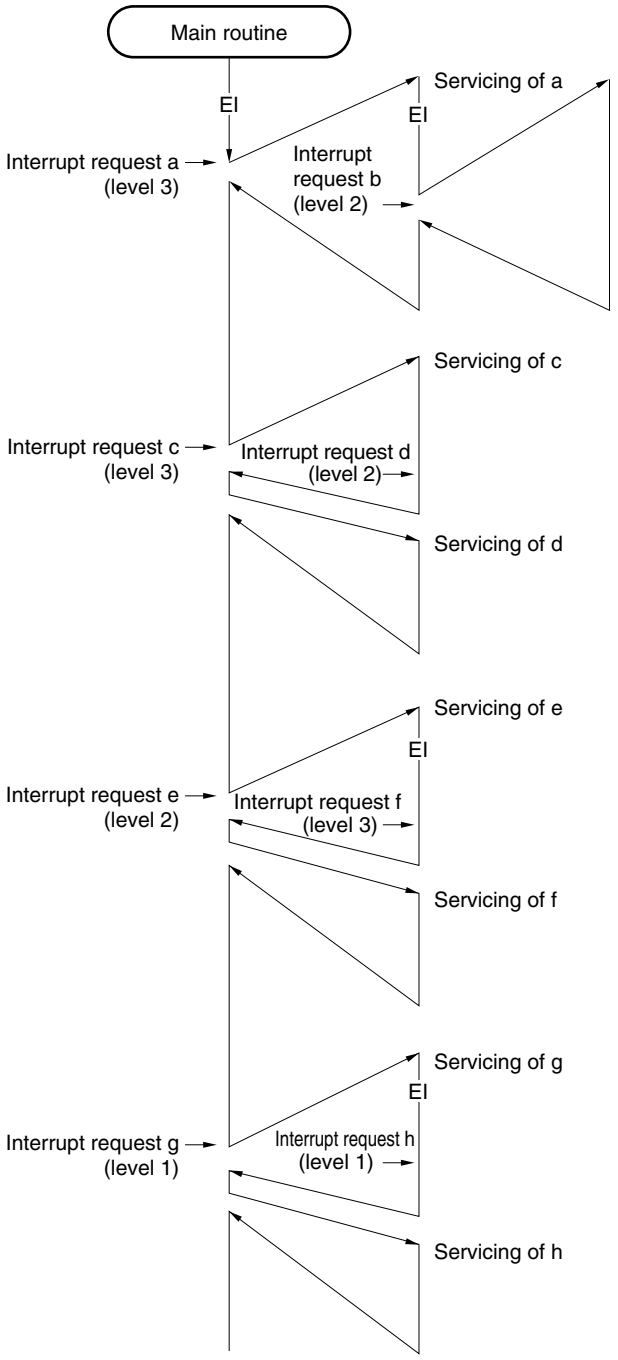
The block diagram of the DMAC is shown below.

Figure 20-1. Block Diagram of DMAC



Remark n = 0 to 3

Figure 21-7. Example of Processing in Which Another Interrupt Request Signal Is Issued While an Interrupt Is Being Serviced (1/2)



Caution To service multiple interrupts, the values of the EIPC and EIPSW registers must be saved before executing the EI instruction. When returning from multiple interrupt servicing, restore the values of EIPC and EIPSW after executing the DI instruction.

Remarks 1. a to u in the figure are the temporary names of interrupt request signals shown for the sake of explanation.

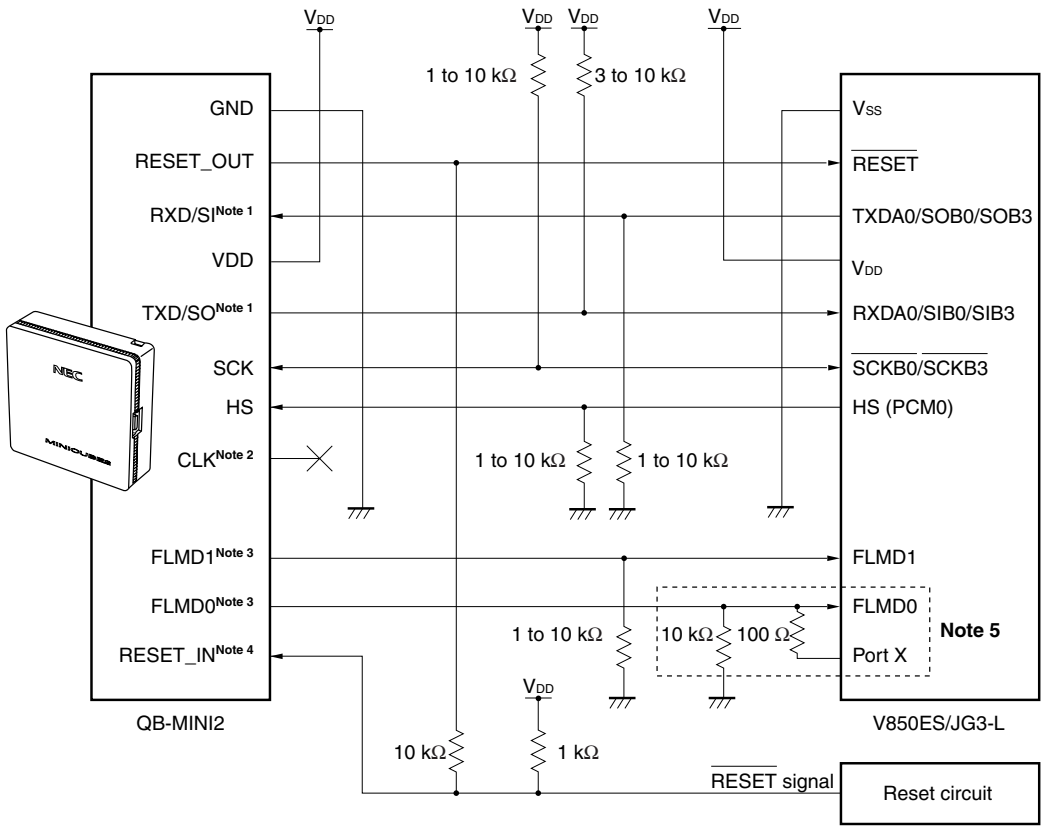
2. The default priority in the figure indicates the relative priority between two interrupt request signals.

31.2 Debugging Without Using DCU

The following describes how to implement an on-chip debug function using MINICUBE2 with pins for UARTA0 (RXDA0 and TXDA0), pins for CSIB0 (SIB0, SOB0, $\overline{SCKB0}$, and HS (PCM0)), or pins for CSIB3 (SIB3, SOB3, $\overline{SCKB3}$, and HS (PCM0)) as the debug interface, without using the DCU.

31.2.1 Circuit connection examples

Figure 31-4. Circuit Connection Example When UARTA0/CSIB0/CSIB3 Is Used for Communication Interface



Notes 1. Connect TXDA0/SOB0/SOB3 (transmit side) of the V850ES/JG3-L to RXD/SI (receive side) of the target connector, and TXD/SO (transmit side) of the target connector to RXDA0/SIB0/SIB3 (receive side) of the V850ES/JG3-L.

2. This pin is not used during on-chip debugging.

3. During debugging, this pin is used as an input (unused) pin and can be used for its alternate functions. A pull-down resistor of 100kΩ is connected to this pin in MINICUBE2.

4. This connection is designed assuming that the $\overline{RESET}$ signal is output from an N-ch open-drain buffer (output resistance: 100 Ω or less).

5. The circuit enclosed by a dashed line is designed for flash self programming and controls the FLMD0 pin via a port. Use a port for inputting or outputting the high level. When flash self programming is not performed, the pull-down resistance for the FLMD0 pin can be 1 to 10 kΩ.

Remark See **Table 31-3** for the pins used when UARTA0, CSIB0, or CSIB3 is used for communication interface.

(3) Bus hold

(a) Asynchronous to CLKOUT

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.7 to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

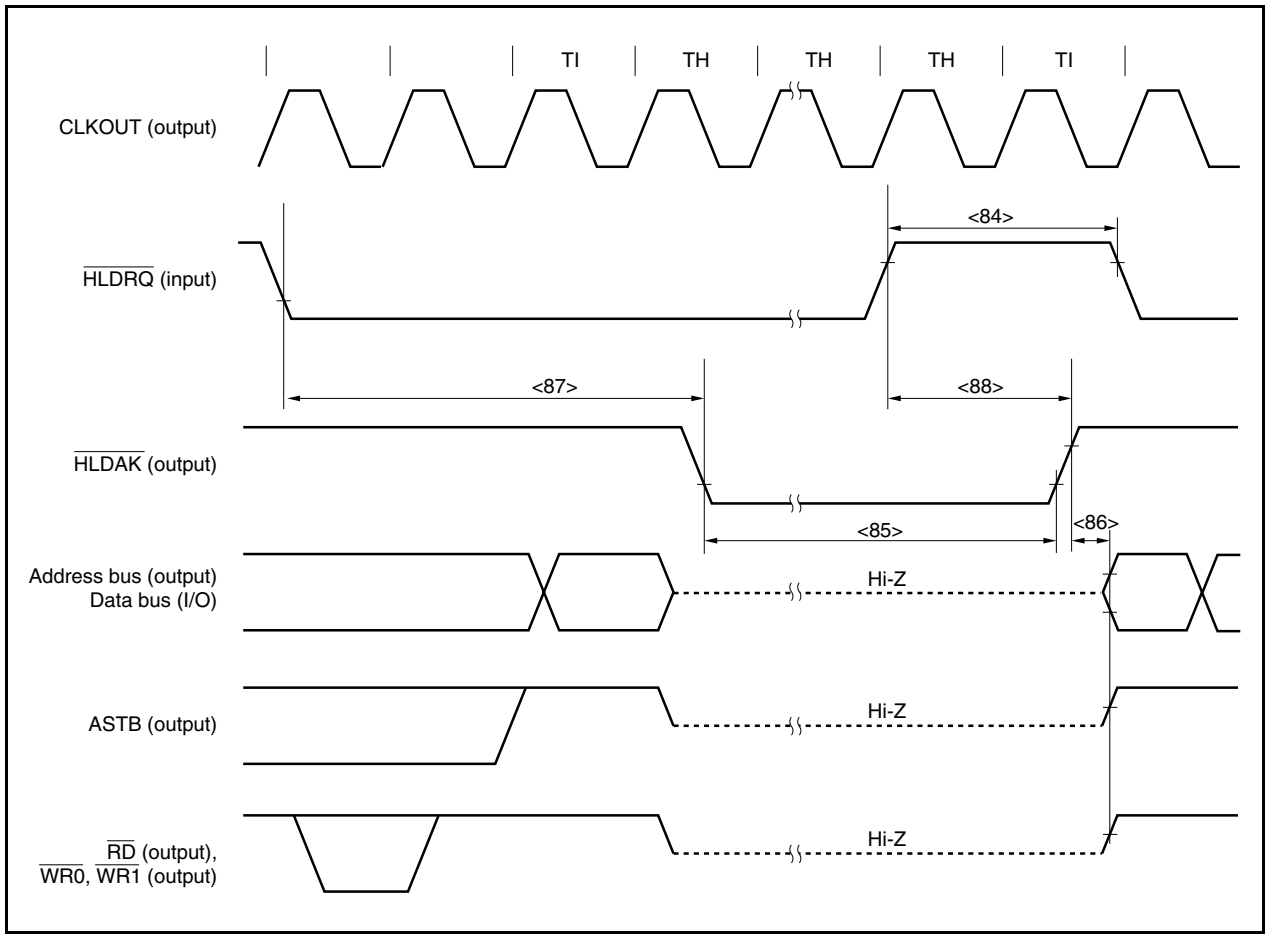
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ high-level width	t_{WHQH}	<84>		T + 10		ns
$\overline{\text{HLDAK}}$ low-level width	t_{WHAL}	<85>		T – 15		ns
Delay time from $\overline{\text{HLDAK}}\uparrow$ to bus output	t_{DHAC}	<86>		–3		ns
Delay time from $\overline{\text{HLDRQ}}\downarrow$ to $\overline{\text{HLDAK}}\downarrow$	t_{DHQHA1}	<87>			(2n + 7.5)T + 26	ns
Delay time from $\overline{\text{HLDRQ}}\uparrow$ to $\overline{\text{HLDAK}}\uparrow$	t_{DHQHA2}	<88>		0.5T	1.5T + 26	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle
The sampling timing changes when a programmable wait is inserted.

3. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Bus Hold (Asynchronous to CLKOUT)



(8/11)

Symbol	Name	Unit	Page
RTBH0	Real-time output buffer register 0H	RTP	496
RTBL0	Real-time output buffer register 0L	RTP	496
RTC0IC	Interrupt control register	INTC	799
RTC1IC	Interrupt control register	INTC	799
RTC2IC	Interrupt control register	INTC	799
RTCBUMCTL0	RTC backup control register 0	RTC	858
RTPC0	Real-time output port control register 0	RTP	498
RTPM0	Real-time output port mode register 0	RTP	497
SELCNT0	Selector operation control register 0	Timer	325
SOSCAMCTL	Subclock low-power operation control register	Standby	859
SVA0	Slave address register 0	I^2C	701
SVA1	Slave address register 1	I^2C	701
SVA2	Slave address register 2	I^2C	701
SYS	System status register	CPU	90
TM0CMP0	TMM0 compare register 0	Timer	441
TM0CTL0	TMM0 control register 0	Timer	440
TM0EQIC0	Interrupt control register	INTC	799
TP0CCIC0	Interrupt control register	INTC	799
TP0CCIC1	Interrupt control register	INTC	799
TP0CCR0	TMP0 capture/compare register 0	Timer	243
TP0CCR1	TMP0 capture/compare register 1	Timer	245
TP0CNT	TMP0 counter read buffer register	Timer	247
TP0CTL0	TMP0 control register 0	Timer	237
TP0CTL1	TMP0 control register 1	Timer	238
TP0IOC0	TMP0 I/O control register 0	Timer	239
TP0IOC1	TMP0 I/O control register 1	Timer	240
TP0IOC2	TMP0 I/O control register 2	Timer	241
TP0OPT0	TMP0 option register 0	Timer	242
TP0OVIC	Interrupt control register	INTC	799
TP1CCIC0	Interrupt control register	INTC	799
TP1CCIC1	Interrupt control register	INTC	799
TP1CCR0	TMP1 capture/compare register 0	Timer	243
TP1CCR1	TMP1 capture/compare register 1	Timer	245
TP1CNT	TMP1 counter read buffer register	Timer	247
TP1CTL0	TMP1 control register 0	Timer	237
TP1CTL1	TMP1 control register 1	Timer	238
TP1IOC0	TMP1 I/O control register 0	Timer	239
TP1IOC1	TMP1 I/O control register 1	Timer	240
TP1IOC2	TMP1 I/O control register 2	Timer	241
TP1OPT0	TMP1 option register 0	Timer	242
TP1OVIC	Interrupt control register	INTC	799
TP2CCIC0	Interrupt control register	INTC	799
TP2CCIC1	Interrupt control register	INTC	799
TP2CCR0	TMP2 capture/compare register 0	Timer	243
TP2CCR1	TMP2 capture/compare register 1	Timer	245