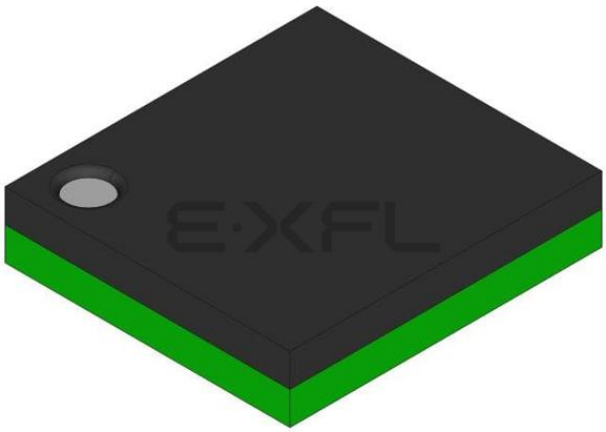

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	V850ES
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	CSI, EBI/EMI, I²C, UART/USART
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	83
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	40K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd70f3793gc-ueu-ax

(7) Port 0 function register (PF0)

After reset: 00H R/W Address: FFFFFC60H

	7	6	5	4	3	2	1	0
PF0	0	PF06	PF05	PF04	PF03	PF02	0	0

PF0n	Specification of normal output (CMOS output) or N-ch open-drain output (n = 2 to 6)
0	Normal output (CMOS output)
1	N-ch open-drain output

Caution When an output pin is pulled up to EV_{DD} or higher, be sure to set the PF0n bit to 1.

(7) Port 3 function register (PF3)

After reset: 0000H R/W Address: PF3 FFFFFC66H,
PF3L FFFFFC66H, PF3H FFFFFC67H

	15	14	13	12	11	10	9	8
PF3 (PF3H)	0	0	0	0	0	0	PF39	PF38

	7	6	5	4	3	2	1	0
(PF3L)	PF37	PF36	PF35	PF34	PF33	PF32	PF31	PF30

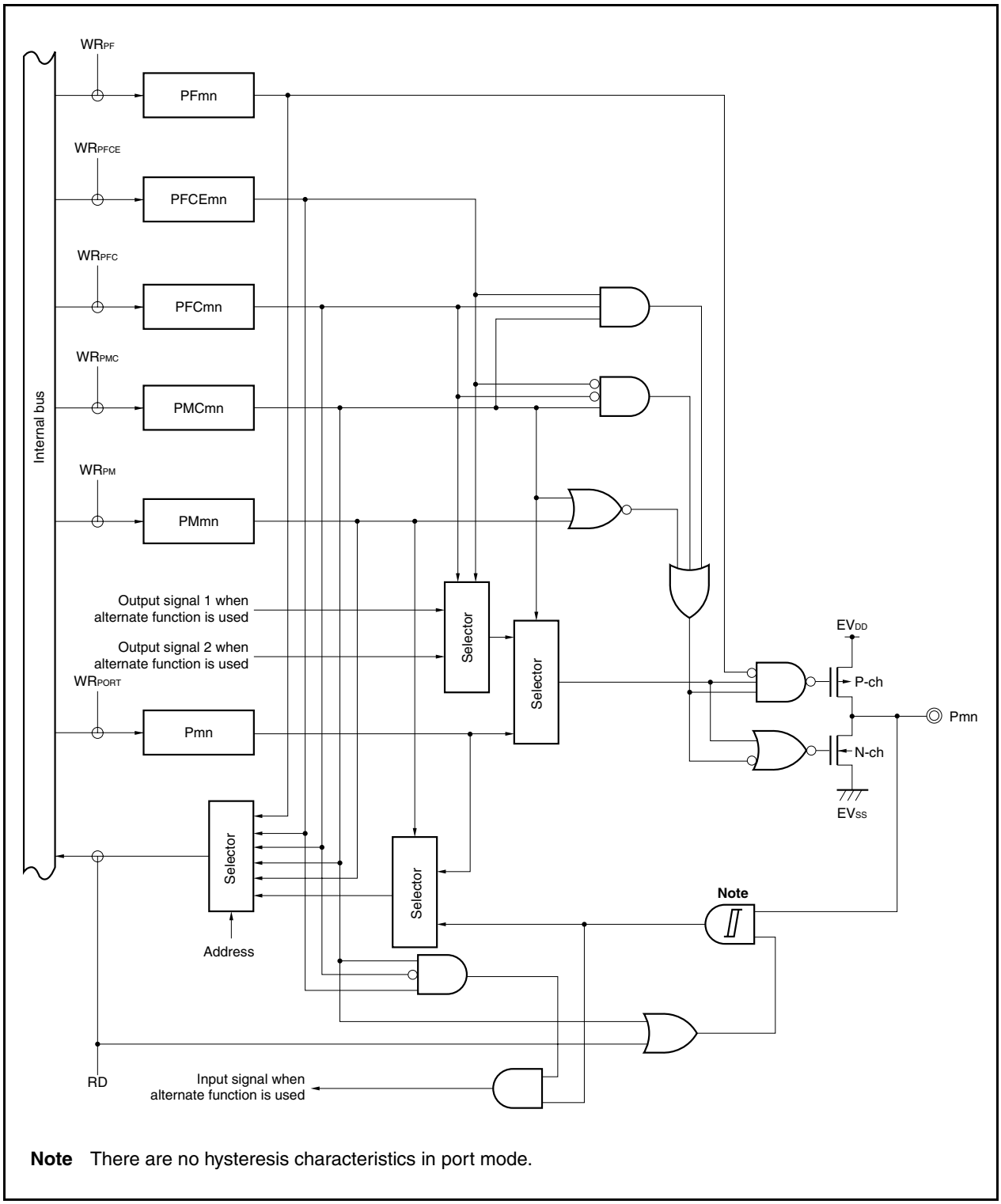
PF3n	Specification of normal output (CMOS output) or N-ch open-drain output (n = 0 to 9)
0	Normal output (CMOS output)
1	N-ch open-drain output

Caution When an output pin is pulled up to EV_{DD} or higher, be sure to set the PF3n bit to 1.

Remarks 1. The PF3 register can be read or written in 16-bit units.
However, when using the higher 8 bits of the PF3 register as the PF3H register and the lower 8 bits as the PF3L register, PF3 can be read or written in 8-bit or 1-bit units.

2. To read/write bits 8 to 15 of the PF3 register in 8-bit or 1-bit units, specify them as bits 0 to 7 of the PF3H register.

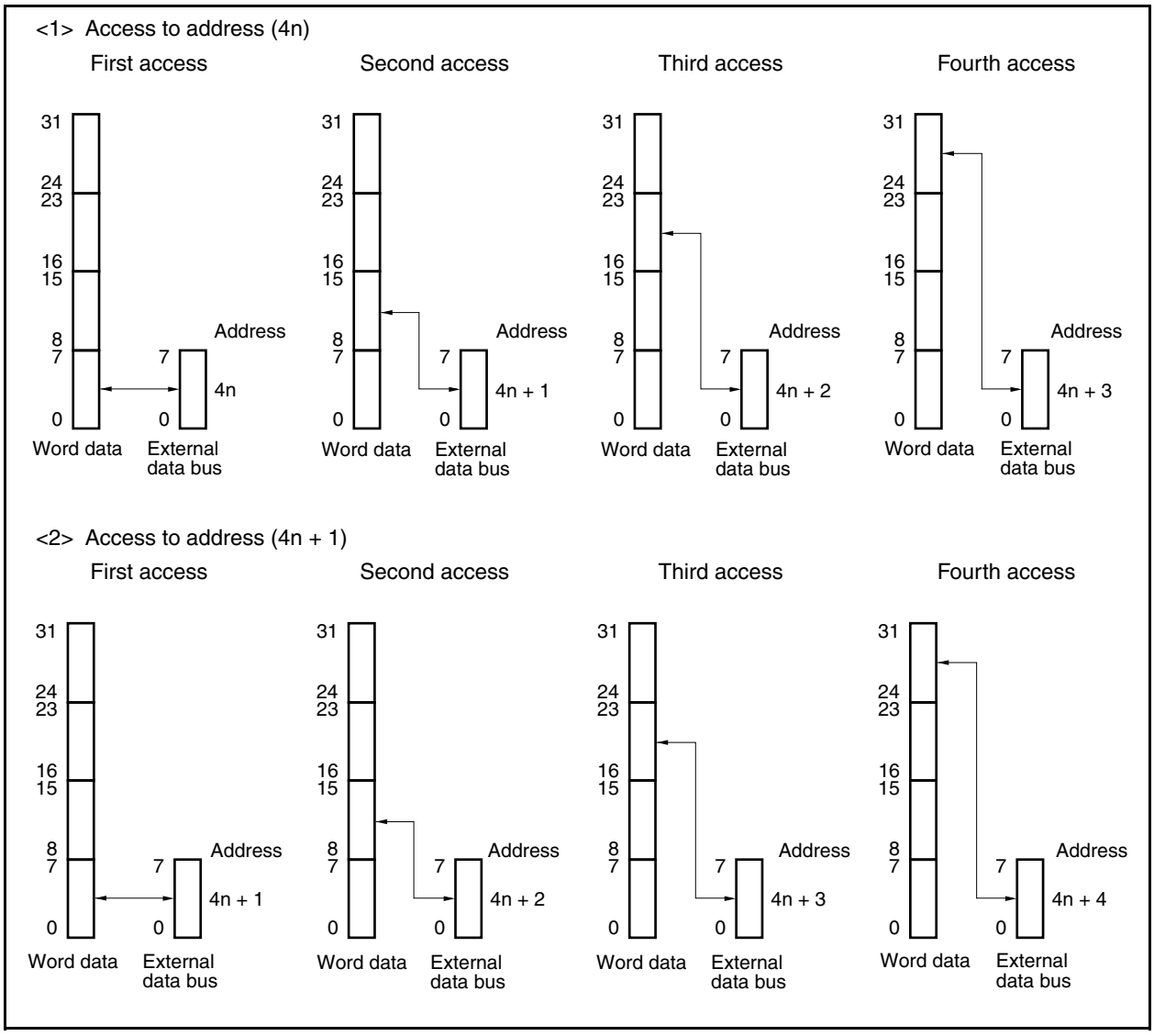
Figure 4-29. Block Diagram of Type U-13



Note There are no hysteresis characteristics in port mode.

(b) 8-bit data bus width (1/2)

32-bit data is transmitted/received via an 8-bit bus. Therefore, the data is transmitted/received in four accesses. The data is transmitted/received to/from the specified even/odd address of the external data bus.



7.3 Registers

The registers that control TMPn are as follows.

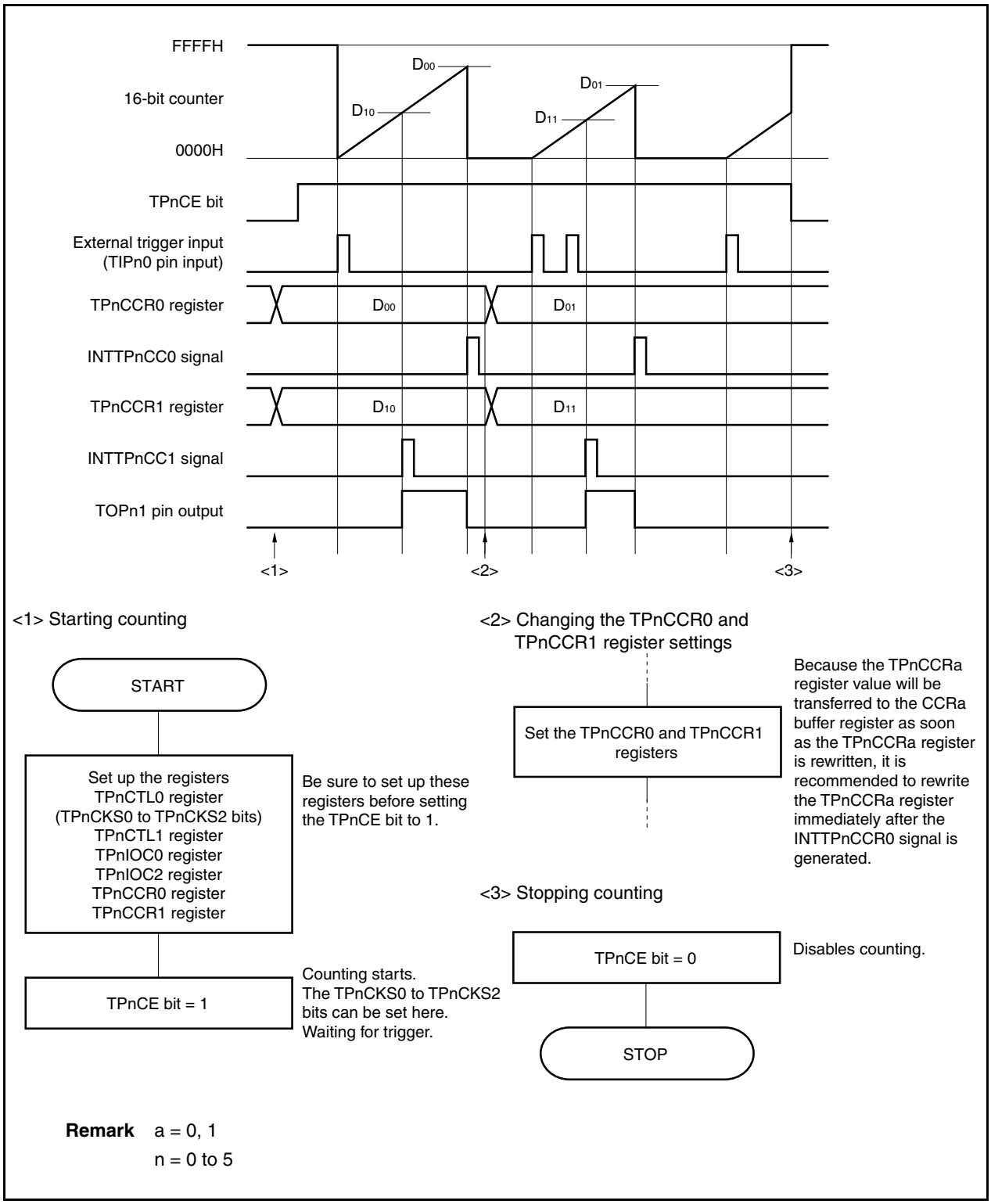
- TMPn control register 0 (TPnCTL0)
- TMPn control register 1 (TPnCTL1)
- TMPn I/O control register 0 (TPnIOC0)
- TMPn I/O control register 1 (TPnIOC1)
- TMPn I/O control register 2 (TPnIOC2)
- TMPn option register 0 (TPnOPT0)
- TMPn capture/compare register 0 (TPnCCR0)
- TMPn capture/compare register 1 (TPnCCR1)
- TMPn counter read buffer register (TPnCNT)

Remarks 1. When using the functions of the TIPn0, TIPn1, TOPn0, and TOPn1 pins, see **Table 4-15 Settings When Pins Are Used for Alternate Functions**.

2. n = 0 to 5

(1) Operations in one-shot pulse output mode

Figure 7-41. Timing and Processing of Operations in One-Shot Pulse Output Mode



Remark a = 0, 1
n = 0 to 5

Figure 8-28. Register Settings in External Trigger Pulse Output Mode (2/3)

(b) TMQ0 control register 1 (TQ0CTL1)

	TQ0EST	TQ0EEE			TQ0MD2	TQ0MD1	TQ0MD0
TQ0CTL1	0	0/1	0	0	0	0	1	0

0, 1, 0:
External trigger pulse output mode

Writing 1 generates a software trigger.

(c) TMQ0 I/O control register 0 (TQ0IOC0)

	TQ0OL3	TQ0OE3	TQ0OL2	TQ0OE2	TQ0OL1	TQ0OE1	TQ0OL0	TQ0OE0
TQ0IOC0	0/1	0/1	0/1	0/1	0/1	0/1	0/1[Note]	0/1[Note]

0: Disable TOQ00 pin output.
1: Enable TOQ00 pin output.

Output level when TOQ00 pin is disabled:
0: Low level
1: High level

0: Disable TOQ01 pin output.
1: Enable TOQ01 pin output.

Active level of TOQ01 pin output:
0: High level
1: Low level

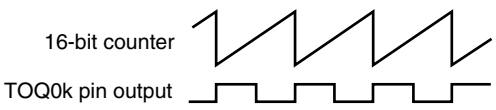
0: Disable TOQ02 pin output.
1: Enable TOQ02 pin output.

Active level of TOQ02 pin output:
0: High level
1: Low level

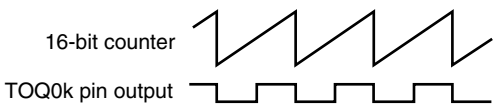
0: Disable TOQ03 pin output.
1: Enable TOQ03 pin output.

Active level of TOQ03 pin output:
0: High level
1: Low level

- When TQ0OLk bit is 0:

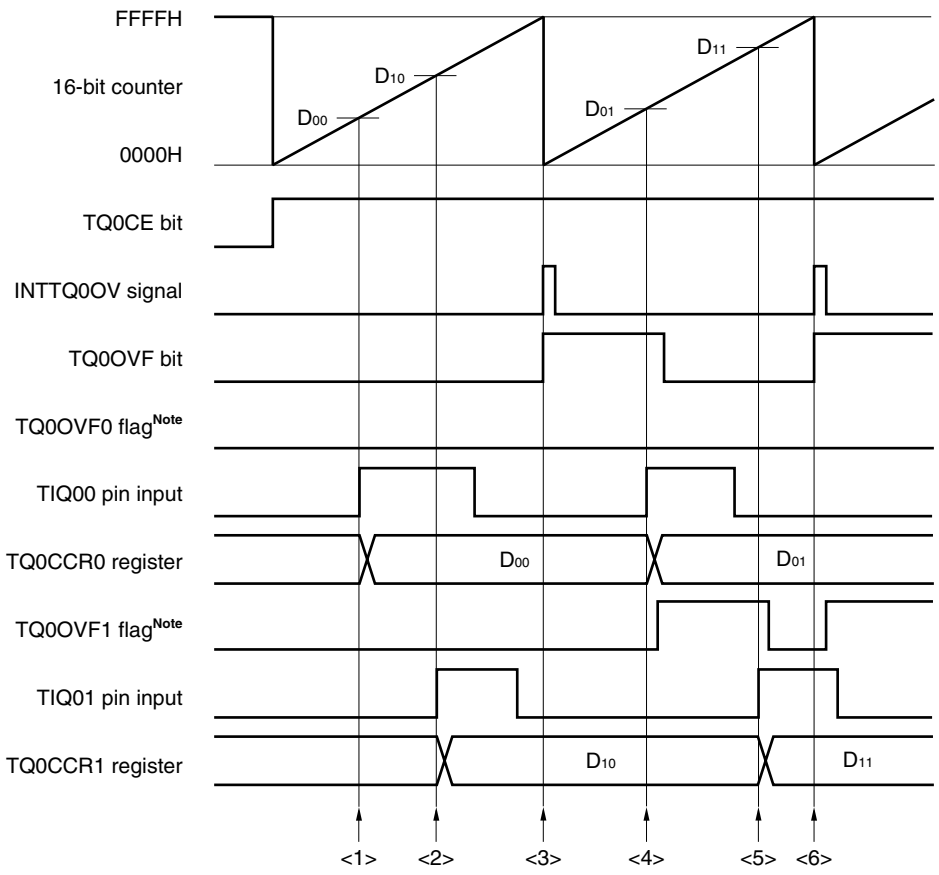


- When TQ0OLk bit is 1:



Note Set this bit to 0 when not using the TOQ00 pin in external trigger pulse output mode.

Figure 8-62. Example of Resolving Problem When Two or More Capture Registers Are Used Without Using Overflow Interrupt



Note The TQ0OVF0 and TQ0OVF1 flags are set on the internal RAM by software.

<1> The TQ0CCR0 register is read (the default value of the TIQ00 pin input is set).

<2> The TQ0CCR1 register is read (the default value of the TIQ01 pin input is set).

<3> An overflow occurs. There is no software processing.

<4> The TQ0CCR0 register is read.

The TQ0OVF bit is read. The TQ0OVF bit is 1, so only the TQ0OVF1 flag is set to 1; the TQ0OVF bit is cleared to 0.

Because the TQ0OVF bit is 1, the pulse width can be calculated by (10000H + $D_{01} - D_{00}$).

<5> The TQ0CCR1 register is read.

The TQ0OVF bit is read. The TQ0OVF bit was cleared to 0 in <4>, so 0 is read.

The TQ0OVF1 flag is read. The TQ0OVF1 flag is 1, so it is cleared to 0.

Because the TQ0OVF1 flag was 1, the pulse width can be calculated by (10000H + $D_{11} - D_{10}$) (correct).

<6> Same as <3>.

11.2 Configuration

The real-time counter includes the following hardware.

Table 11-1. Configuration of Real-Time Counter

Item	Configuration
Control registers	Real-time counter control register 0 (RC1CC0) Real-time counter control register 1 (RC1CC1) Real-time counter control register 2 (RC1CC2) Real-time counter control register 3 (RC1CC3) Sub-count register (RC1SUBC) Second count register (RC1SEC) Minute count register (RC1MIN) Hour count register (RC1HOUR) Day count register (RC1DAY) Day-of-week count register (RC1WEEK) Month count register (RC1MONTH) Year count register (RC1YEAR) Watch error correction register (RC1SUBU) Alarm minute register (RC1ALM) Alarm hour register (RC1ALH) Alarm week register (RC1ALW) Prescaler mode register 0 (PRSM0) Prescaler compare register 0 (PRSCM0)

(13) Watch error correction register (RC1SUBU)

The RC1SUBU register can be used to correct the watch with high accuracy when the watch is early or late, by changing the value (reference value: 7FFFH) overflowing from the sub-count register (RSUBC) to the second counter register.

This register can be read or written in 8-bit or 1-bit units.

Reset sets this register to 00H.

Remarks 1. The RC1SUBU register can be rewritten only when the real-time counter is set to its initial values. Be sure to see **11.4.1 Initial settings**.

2. See **11.4.9 Watch error correction example of real-time counter** for details of watch error correction.

After reset: 00H R/W Address: FFFFFAD9H

	7	6	5	4	3	2	1	0
RC1SUBU	DEV	F6	F5	F4	F3	F2	F1	F0

DEV	Setting of watch error correction timing
0	Corrects watch errors when RC1SEC (second counter) is at 00, 20, or 40 seconds (every 20 seconds).
1	Corrects watch errors when RC1SEC (second counter) is at 00 seconds (every 60 seconds).

F6	Setting of watch error correction value
0	Increments the RC1SUBC count value by the value set using the F5 to F0 bits (positive correction). Expression for calculating increment value: (Setting value of F5 to F0 bits − 1) × 2
1	Decrements the RC1SUBC count value by the value set using the F5 to F0 bits (negative correction). Expression for calculating decrement value: (Inverted value of setting value of F5 to F0 bits + 1) × 2
If the F6 to F0 bit values are {1/0, 0, 0, 0, 0, 0, 1/0}, watch error correction is not performed.	

Remark When RTC back up mode, Watch error correction is stop.

If the ADA0M0, ADA0M2, ADA0S, ADA0PFM, or ADA0PFT register is written during conversion, the conversion is aborted, and the A/D converter waits for the trigger again. However, writing to these registers is prohibited in the one-shot select mode/one-shot scan mode (n = 0 to 11).

Caution When selecting the external trigger mode, set the high-speed conversion mode. Do not input a trigger during the stabilization time that is inserted once after A/D conversion is enabled (ADA0M0.ADA0CE bit = 1).

Remark The trigger standby status means the status after the stabilization time has passed.

(3) Timer trigger mode

In this mode, converting the signal of the analog input pin (ANI0 to ANI11) specified by the ADA0S register is started by the compare match interrupt request signal (INTTP2CC0 or INTTP2CC1) of the capture/compare register connected to the timer. The INTTP2CC0 or INTTP2CC1 signal is selected by the ADA0TMD1 and ADA0TMD0 bits, and conversion is started at the rising edge of the specified compare match interrupt request signal. When the ADA0CE bit is set to 1, the A/D converter waits for a trigger, and starts conversion when the compare match interrupt request signal of the timer is input.

When conversion is completed, regardless of whether the continuous select, continuous scan, one-shot select, or one-shot scan mode is set as the operation mode by the ADA0MD1 and ADA0MD0 bits, the result of the conversion is stored in the ADA0CRn register. At the same time, the INTAD signal is generated, and the A/D converter waits for the trigger again.

When conversion is started, the ADA0EF bit is set to 1 (indicating that conversion is in progress). While the A/D converter is waiting for the trigger, however, the ADA0EF bit is cleared to 0 (indicating that conversion is stopped). If a valid trigger is input during conversion, the conversion is aborted and started again from the beginning.

If the ADA0M0, ADA0M2, ADA0S, ADA0PFM, or ADA0PFT register is written during conversion, the conversion is stopped and the A/D converter waits for the trigger again. However, writing to these registers is prohibited in the one-shot select mode/one-shot scan mode.

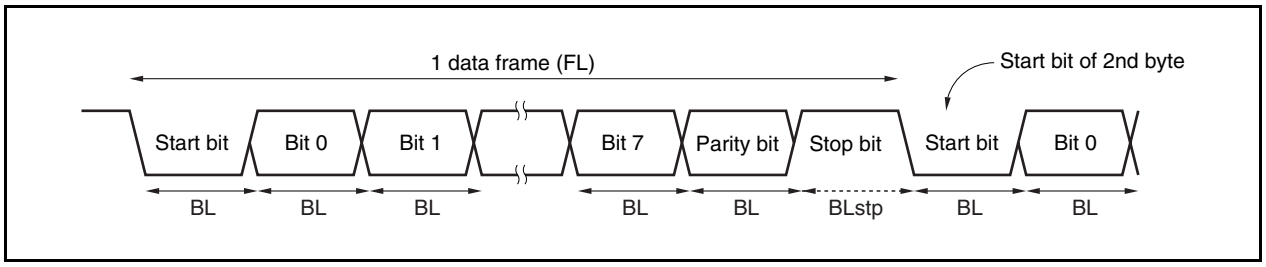
Caution When selecting the timer trigger mode, set the high-speed conversion mode. Do not input a trigger during the stabilization time that is inserted once after A/D conversion is enabled (ADA0M0.ADA0CE bit = 1).

Remark The trigger standby status means the status after the stabilization time has passed.

(6) Data frame length during continuous transmission

In continuous transmission, the data frame length from the stop bit to the next start bit is 2 base clock cycles longer than usual. However, timing initialization is performed via start bit detection by the receiving side, so this has no influence on the transfer result.

Figure 16-19. Data Frame Length During Continuous Transmission



Assuming a 1 bit data length of BL; a stop bit length of BLstp; and a base clock frequency of f_{UCLK}, we obtain the following equation.

$$BLstp = BL + 2/f_{UCLK}$$

Therefore, the transfer rate during continuous transmission is as follows.

$$\text{Data frame length} = 11 \times BL + (2/f_{UCLK})$$

(3/3)

CBnSCE	Specification of start transfer disable/enable
0	Communication start trigger invalid
1	Communication start trigger valid

This bit enables or disables the communication start trigger in reception mode.

- In master mode
  - (a) In single transmission or transmission/reception mode, or continuous transmission or continuous transmission/reception mode:
    The setting of the CBnSCE bit has no effect on communication.
  - (b) In single reception mode:
    Clear the CBnSCE bit to 0 before reading the last receive data to disable the start of reception because reception is started by reading the receive data (CBnRX register)[Note 1].
  - (c) In continuous reception mode
    Clear the CBnSCE bit to 0 one communication clock cycle before reception of the last data is completed to disable the start of reception after the last data is received[Note 2].
- In slave mode
  Set the CBnSCE bit to 1.

[Usage of CBnSCE bit]

- In single reception mode
  - <1> When reception of the last data is completed by INTCBnR interrupt servicing, clear the CBnSCE bit to 0 before reading the CBnRX register.
  - <2> After confirming that the CBnSTR.CBnTSF bit is 0, clear the CBnPWR and CBnRXE bits to 0 to disable reception.
    To receive data again, set the CBnSCE bit to 1 to start the next reception by dummy-reading the CBnRX register.
- In continuous reception mode
  - <1> Clear the CBnSCE bit to 0 in the INTCBnR interrupt servicing for the receive data immediately before the last one.
  - <2> Read the CBnRX register.
  - <3> Read the last reception data by reading the CBnRX register after acknowledging the CBnTIR interrupt.
  - <4> After confirming that the CBnSTR.CBnTSF bit is 0, clear the CBnPWR and CBnRXE bits to 0 to disable reception.
    To receive data again, set the CBnSCE bit to 1 to wait for the next reception by dummy-reading the CBnRX register.

Notes 1. If the CBnRX register is read with the CBnSCE bit set to 1, the next communication is started.

2. If the CBnSCE bit is not cleared to 0, one communication clock cycle before reception of the last data is completed, the next communication is automatically started.

Caution Be sure to clear bits 3 and 2 to "0".

After reset: 00H R/W[Note] Address: IICF0 FFFFFD8AH, IICF1 FFFFFD9AH, IICF2 FFFFFDAAH

	<7>	<6>	5	4	3	2	<1>	<0>
IICFn	STCFn	IICBSYn	0	0	0	0	STCENn	IICRSVn

(n = 0 to 2)

STCFn	STTn bit clear
0	Start condition issued
1	Start condition cannot be issued, STTn bit cleared

Condition for clearing (STCFn bit = 0)	Condition for setting (STCFn bit = 1)
• Cleared by IICCn.STTn bit = 1 • When the IICCn.IICEn bit = 0 • After reset	• When start condition is not issued and STTn flag is cleared to 0 during communication reservation is disabled (IICRSVn bit = 1).

IICBSYn	I²C0n bus status
0	Bus released status (default communication status when STCENn bit = 1)
1	Bus communication status (default communication status when STCENn bit = 0)

Condition for clearing (IICBSYn bit = 0)	Condition for setting (IICBSYn bit = 1)
• When stop condition is detected • When the IICEn bit = 0 • After reset	• When start condition is detected • By setting the IICEn bit when the STCENn bit = 0

STCENn	Initial start enable trigger
0	Start conditions cannot be generated until a stop condition is detected following operation enable (IICEn bit = 1).
1	Start conditions can be generated even if a stop condition is not detected following operation enable (IICEn bit = 1).

Condition for clearing (STCENn bit = 0)	Condition for setting (STCENn bit = 1)
• When start condition is detected • After reset	• Setting by instruction

IICRSVn	Communication reservation function disable bit
0	Communication reservation enabled
1	Communication reservation disabled

Condition for clearing (IICRSVn bit = 0)	Condition for setting (IICRSVn bit = 1)
• Clearing by instruction • After reset	• Setting by instruction

Note Bits 6 and 7 are read-only bits.

Cautions 1. Write the STCENn bit only when operation is stopped (IICEn bit = 0).

2. When the STCENn bit = 1, the bus released status (IICBSYn bit = 0) is recognized regardless of the actual bus status immediately after the I²Cn bus operation is enabled. Therefore, to issue the first start condition (STTn bit = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

3. Write the IICRSVn bit only when operation is stopped (IICEn bit = 0).

Table 19-2. Clock Settings (2/2)

IICXm	IICCLm			Selection Clock	Transfer Clock	Settable Main Clock Frequency (fxx) Range	Operating Mode
Bit 0	Bit 3	Bit 1	Bit 0				
CLXm	SMCm	CLm1	CLm0				
0	0	0	0	fxx (when OCKS1 = 18H set)	fxx/44	2.50 MHz ≤ fxx ≤ 4.19 MHz	Standard mode (SMCm bit = 0)
				fxx/2 (when OCKS1 = 10H set)	fxx/88	4.00 MHz ≤ fxx ≤ 8.38 MHz	
				fxx/3 (when OCKS1 = 11H set)	fxx/132	6.00 MHz ≤ fxx ≤ 12.57 MHz	
				fxx/4 (when OCKS1 = 12H set)	fxx/176	8.00 MHz ≤ fxx ≤ 16.76 MHz	
				fxx/5 (when OCKS1 = 13H set)	fxx/220	10.00 MHz ≤ fxx ≤ 20.00 MHz	
0	0	0	1	fxx (when OCKS1 = 18H set)	fxx/86	4.19 MHz ≤ fxx ≤ 8.38 MHz	
				fxx/2 (when OCKS1 = 10H set)	fxx/172	8.38 MHz ≤ fxx ≤ 16.76 MHz	
				fxx/3 (when OCKS1 = 11H set)	fxx/258	12.57 MHz ≤ fxx ≤ 20.00 MHz	
				fxx/4 (when OCKS1 = 12H set)	fxx/344	16.76 MHz ≤ fxx ≤ 20.00 MHz	
0	0	1	0	fxx[Note]	fxx/86	4.19 MHz ≤ fxx ≤ 8.38 MHz	
0	0	1	1	fxx (when OCKS1 = 18H set)	fxx/66	fxx = 6.40 MHz	
				fxx/2 (when OCKS1 = 10H set)	fxx/132	fxx = 12.80 MHz	
				fxx/3 (when OCKS1 = 11H set)	fxx/198	fxx = 19.20 MHz	
0	1	0	×	fxx (when OCKS1 = 18H set)	fxx/24	4.19 MHz ≤ fxx ≤ 8.38 MHz	High-speed mode (SMCm bit = 1)
				fxx/2 (when OCKS1 = 10H set)	fxx/48	8.00 MHz ≤ fxx ≤ 16.76 MHz	
				fxx/3 (when OCKS1 = 11H set)	fxx/72	12.00 MHz ≤ fxx ≤ 20.00 MHz	
				fxx/4 (when OCKS1 = 12H set)	fxx/96	16.00 MHz ≤ fxx ≤ 20.00 MHz	
0	1	1	0	fxx[Note]	fxx/24	4.00 MHz ≤ fxx ≤ 8.38 MHz	
0	1	1	1	fxx (when OCKS1 = 18H set)	fxx/18	fxx = 6.40 MHz	
				fxx/2 (when OCKS1 = 10H set)	fxx/36	fxx = 12.80 MHz	
				fxx/3 (when OCKS1 = 11H set)	fxx/54	fxx = 19.20 MHz	
1	1	0	×	fxx (when OCKS1 = 18H set)	fxx/12	4.00 MHz ≤ fxx ≤ 4.19 MHz	
				fxx/2 (when OCKS1 = 10H set)	fxx/24	8.00 MHz ≤ fxx ≤ 8.38 MHz	
				fxx/3 (when OCKS1 = 11H set)	fxx/36	12.00 MHz ≤ fxx ≤ 12.57 MHz	
				fxx/4 (when OCKS1 = 12H set)	fxx/48	16.00 MHz ≤ fxx ≤ 16.67 MHz	
				fxx/5 (when OCKS1 = 13H set)	fxx/60	fxx = 20.00 MHz	
1	1	1	0	fxx[Note]	fxx/12	4.00 MHz ≤ fxx ≤ 4.19 MHz	
Other than above				Setting prohibited	–	–	–

Note Since the selection clock is fxx regardless of the value set to the OCKS1 register, clear the OCKS1 register to 00H (I²C division clock stopped status).

Remarks 1. m = 1, 2

2. ×: don't care

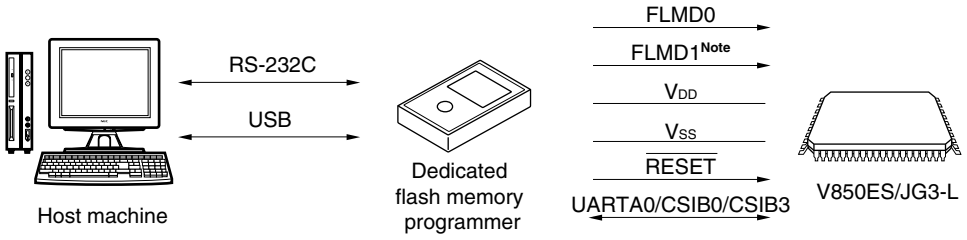
30.4 Rewriting by Dedicated Flash Memory Programmer

The flash memory can be rewritten by using a dedicated flash memory programmer after the V850ES/JG3-L is mounted on the target system (on-board programming). By combining the dedicated flash memory programmer with a dedicated program adapter (FA series), the flash memory can also be rewritten before the device is mounted on the target system (off-board programming).

30.4.1 Programming environment

The following shows the environment required for writing programs to the flash memory of the V850ES/JG3-L.

Figure 30-2. Environment Required for Writing Programs to Flash Memory



Note Connect the FLMD1 pin to the flash memory programmer or connect to GND via a pull-down resistor on the board.

A host machine is required for controlling the dedicated flash memory programmer. In some cases, however, it can be used stand-alone. For details, see the user's manual of the dedicated flash memory programmer.

UARTA0, CSIB0, or CSIB3 is used for the interface between the dedicated flash memory programmer and the V850ES/JG3-L to perform writing, erasing, etc. A dedicated program adapter (FA series) is required for off-board writing.

The following products are recommended:

- FA-70F3738GC-UEU-RX (GC-UEU type) (already wired)
- FA-70F3738GF-GAS-RX (GF-GAS type) (already wired)
- FA-70F3738F1-CAH-RX (F1-CAH type) (already wired)

<R> • FA-70F3793GC-UEU-RX (GC-UEU type) (already wired) (Tentative name : Under development)

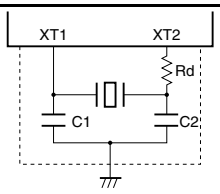
<R> • FA-70F3793F1-CAH-RX (F1-CAH type) (already wired) (Tentative name : Under development)

- FA-100GC-UEU-B (GC-UEU type) (not wired: wiring required)
- FA-100GF-GAS-B (GF-GAS type) (not wired: wiring required)

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

(a) Seiko Instruments Inc.: Crystal resonator (T_A = –40 to +85°C)

Oscillation frequency: f_{XT} = 32.768 kHz

Type	Circuit Example	Part Number	Load Capacitance of Crystal Resonator (pF)	Recommended Circuit Constant			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)
Surface mounting		SP-T2A	6	5	5	0	2.2	3.6
			12.5	18	18	0	2.2	3.6
		SSP-T7	7	8	8	0	2.2	3.6
Lead		VT-200	6	6	6	0	2.2	3.6
			12.5	18	18	0	2.2	3.6

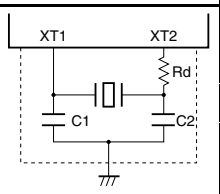
Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer.

If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the V850ES/JG3-L so that the internal operating conditions are within the specifications of the AC characteristics, DC characteristics, and operating conditions.

(b) Citizen Miyota Co., Ltd.: Crystal resonator (T_A = –40 to +85°C)

Oscillation frequency: f_{XT} = 32.768 kHz

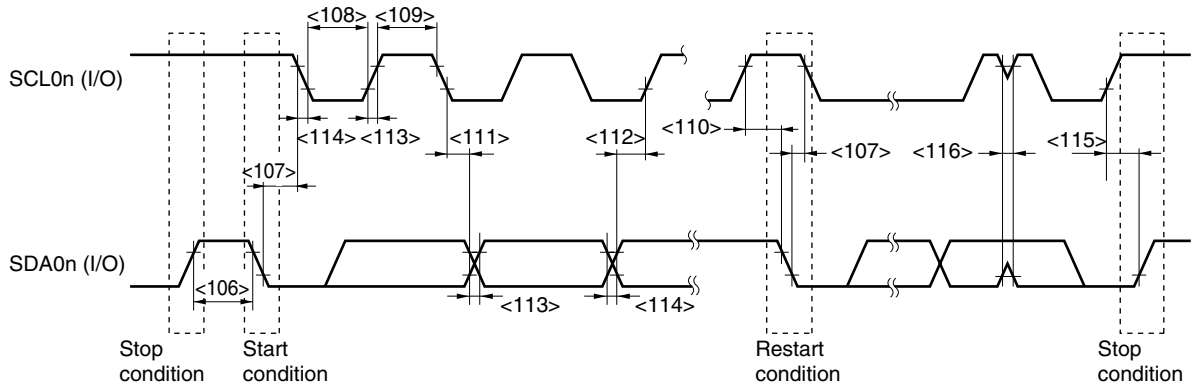
Type	Circuit Example	Part Number	Load Capacitance of Crystal Resonator (pF)	Recommended Circuit Constant			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (Ω)	MIN. (V)	MAX. (V)
Surface mounting		CM200S	9	12	12	100	2.2	3.6
		CMR200T	9	12	12	100	2.2	3.6
		CM519	9	12	12	100	2.2	3.6
Lead		CM315	9	12	12	100	2.2	3.6
		CFS-206	9	12	12	100	2.2	3.6

Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer.

If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the V850ES/JG3-L so that the internal operating conditions are within the specifications of the AC characteristics, DC characteristics, and operating conditions.

I²C Bus Timing



Remark n = 0 to 2

32.8.7 A/D converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1}, 2.7 V ≤ AV_{REF0} = AV_{REF1} ≤ 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Overall error[Note]		2.7 V ≤ AV_{REF0} ≤ 3.6 V			±0.6	%FSR
A/D conversion time	t_{CONV}	3.0 V ≤ AV_{REF0} ≤ 3.6 V	2.6		24	μs
		2.7 V ≤ AV_{REF0} ≤ 3.0 V	3.9		24	μs
Zero scale error					±0.5	%FSR
Full scale error					±0.5	%FSR
Non-linearity error					±4.0	LSB
Differential linearity error					±4.0	LSB
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		3.6	V
AV_{REF0} current	AI_{REF0}	Normal conversion mode		3	6.5	mA
		High-speed conversion mode		4	10	mA
		When A/D converter unused			5	μA

Note Excluding quantization error (±0.05 %FSR).

Caution Do not set (read/write) alternate-function ports during A/D conversion; otherwise the conversion resolution may be degraded.

Remark LSB: Least Significant Bit
FSR: Full Scale Range

33.8.10 RTC back-up mode characteristics

(1) V_{DD} Power-down timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.0 V to 3.6 V, RV_{DD} = 1.8 V to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
<R> V_{DD} negative slew rate	V_{DDNSR1}	When using RTC backup mode, and setting the LVI detection level to 2.80 ± 0.10 V			0.2	V/ms
<R>	V_{DDNSR2}	When using RTC backup mode, and setting the LVI detection level to 2.30 ± 0.10 V			0.07	V/ms

(2) V_{DD} Power-up timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.0 V to 3.6 V, RV_{DD} = 1.8 V to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
<R> V_{DD} positive slew rate	RV_{DDPSR}		3.0			V/s

(3) Regulator output voltage for RTC backup area (VCH)

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.0 V to 3.6 V, RV_{DD} = 1.8 V to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Regulator output voltage for RTC backup area (VCH)	VCH		0.8		1.8	V

(4) VCH setup time

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} = 2.0 V to 3.6 V, RV_{DD} = 2.0 V to 3.6 V, V_{SS} = EV_{SS} = AV_{SS} = 0V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VCH setup time	t_{SPOR}	The time from when RV_{DD} reaches the maximum amplitude (V_{DD} = 2.0 to 3.6 V) until VCH is stable			4.5	ms

(4/6)

Mnemonic	Operand	Opcode	Operation	Execution Clock			Flags				
				i	r	l	CY	OV	S	Z	SAT
OR	reg1,reg2	rrrrr001000RRRRR	GR[reg2]←GR[reg2]OR GR[reg1]	1	1	1		0	×	×	
ORI	imm16,reg1,reg2	rrrrr110100RRRRR iiiiiiiiiiiiiiii	GR[reg2]←GR[reg1]OR zero-extend(imm16)	1	1	1		0	×	×	
PREPARE	list12,imm5	0000011110iiiiiL LLLLLLLLLLL00001	Store-memory(sp–4,GR[reg in list12],Word) sp←sp–4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend(imm5)	n+1 Note 4	n+1 Note 4	n+1 Note 4					
	list12,imm5, sp/imm[Note 15]	0000011110iiiiiL LLLLLLLLLLLff011 imm16/imm32 **Note 16**	Store-memory(sp–4,GR[reg in list12],Word) sp←sp+4 repeat 1 step above until all regs in list12 is stored sp←sp-zero-extend (imm5) ep←sp/imm	n+2 Note 4 Note 17	n+2 Note 4 Note 17	n+2 Note 4 Note 17					
RETI		0000011111100000 0000000101000000	if PSW.EP=1 then PC ←EIPC PSW ←EIPSW else if PSW.NP=1 then PC ←FEPC PSW ←FEPSW else PC ←EIPC PSW ←EIPSW	3	3	3	R	R	R	R	R
SAR	reg1,reg2	rrrrr111111RRRRR 0000000010100000	GR[reg2]←GR[reg2]arithmetically shift right by GR[reg1]	1	1	1	×	0	×	×	
	imm5,reg2	rrrrr010101iiiii	GR[reg2]←GR[reg2]arithmetically shift right by zero-extend (imm5)	1	1	1	×	0	×	×	
SASF	cccc,reg2	rrrrr1111110cccc 0000001000000000	if conditions are satisfied then GR[reg2]←(GR[reg2]Logically shift left by 1) OR 00000001H else GR[reg2]←(GR[reg2]Logically shift left by 1) OR 00000000H	1	1	1					
SATADD	reg1,reg2	rrrrr000110RRRRR	GR[reg2]←saturated(GR[reg2]+GR[reg1])	1	1	1	×	×	×	×	×
	imm5,reg2	rrrrr010001iiiii	GR[reg2]←saturated(GR[reg2]+sign-extend(imm5)	1	1	1	×	×	×	×	×
SATSUB	reg1,reg2	rrrrr000101RRRRR	GR[reg2]←saturated(GR[reg2]–GR[reg1])	1	1	1	×	×	×	×	×
SATSUBI	imm16,reg1,reg2	rrrrr110011RRRRR iiiiiiiiiiiiiiii	GR[reg2]←saturated(GR[reg1]–sign-extend(imm16)	1	1	1	×	×	×	×	×
SATSUBR	reg1,reg2	rrrrr000100RRRRR	GR[reg2]←saturated(GR[reg1]–GR[reg2])	1	1	1	×	×	×	×	×
SETF	cccc,reg2	rrrrr1111110cccc 0000000000000000	If conditions are satisfied then GR[reg2]←00000001H else GR[reg2]←00000000H	1	1	1					