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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IDE, Memory Card, SPI, UART/USART
Peripherals	DMA, I²S, POR, Serial Audio, WDT
Number of I/O	34
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/scf5249lag120

- 1.8V core, 3.3V I/O
- 160 pin MAPBGA package (qualified at 140 MHz) and 144 pin QFP package (qualified at 120 MHz)
- -20^0 C to 70^0 C ambient operating temperature range

2 SCF5249 Block Diagram

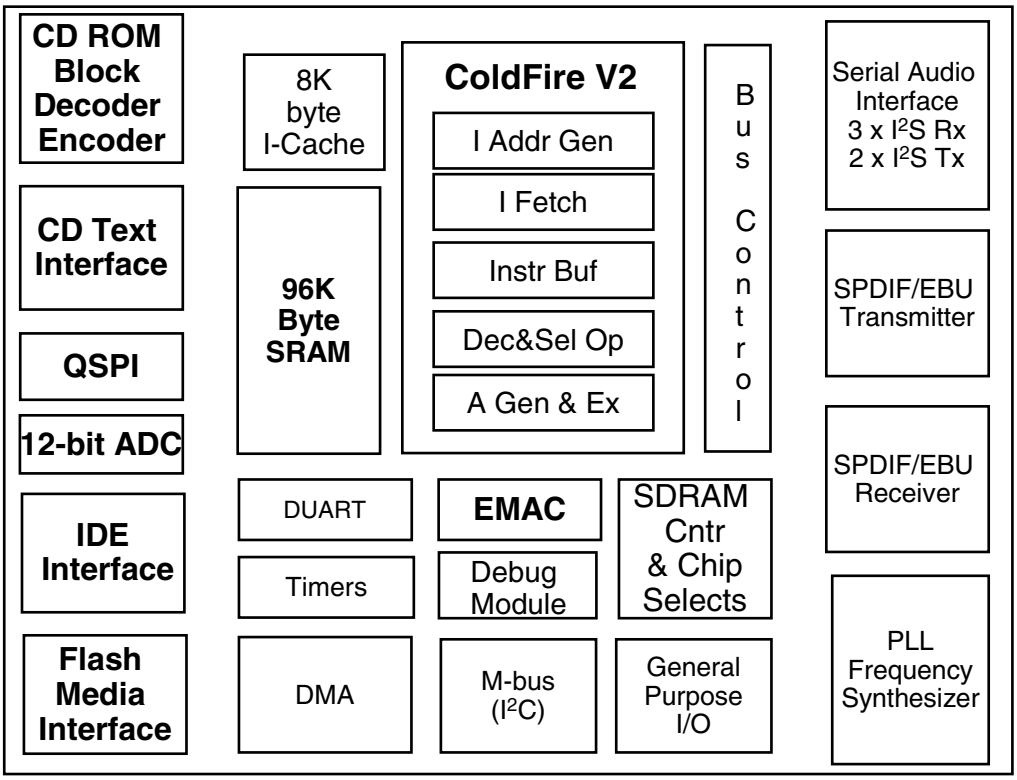

Figure 1. SCF5249 Block Diagram

3 SCF5249 Feature Details

The primary features of the SCF5249 integrated processor include the following:

- ColdFire V2 Processor Core operating at 140MHz
  - — Clock-doubled Version 2 microprocessor core
  - — 32-bit internal data bus, 16 bit external data bus
  - — 16 user-visible, 32-bit general-purpose registers
  - — Supervisor/user modes for system protection
  - — Vector base register to relocate exception-vector table
  - — Optimized for high-level language constructs

- DMA controller
  - Four fully programmable channels: Two dedicated to the audio interface module and two dedicated to the UART module (External requests are not supported.)
  - Supports dual- and single-address transfers with 32-bit data capability
  - Two address pointers that can increment or remain constant
  - 16-/24-bit transfer counter
  - Operand packing and unpacking support
  - Auto-alignment transfers supported for efficient block movement
  - Supports bursting and cycle stealing
  - All channels support memory to memory transfers
  - Interrupt capability
  - Provides two clock cycle internal access
- Enhanced Multiply-accumulator Unit
  - Single-cycle multiply-accumulate operations for 32 x 32 bit and 16 x 16 bit operands
  - Support for signed, unsigned, integer, and fixed-point fractional input operands
  - Four 48-bit accumulators to allow the use of a 40-bit product
  - The addition of 8 extension bits to increase the dynamic number range
  - Fast signed and unsigned integer multiplies
- 8-KByte Direct Mapped instruction cache
  - Clock-doubled to match microprocessor core speed
  - Flush capability
  - Non-blocking cache provides fast access to critical code and data
- 96-KByte SRAM
  - Provides one-cycle access to critical code and data
  - Split into two banks, SRAM0 (32K), and SRAM1 (64K)
  - DMA requests to/from internal SRAM1 supported
- Crystal Trim
  - The XTRIM output can be used to trim an external crystal oscillator circuit which would allow lock with an incoming IEC958 or serial audio signal
- Audio Interfaces
  - IEC958 input and output
  - Four serial Philips IIS/Sony EIAJ interfaces
    - One with input and output, one with output only, two with input only (Three inputs, two outputs)
    - Master and Slave operation

Table 3. SCF5249 Documentation

Document Name	Description	Order Number
CFPRM/D	ColdFire Family Programmer's Reference Manual	CFPRM/D
ColdFire2UM	Version 2/2M ColdFire Core Processor User's Manual	ColdFire2UM/D
ColdFire2UMAD	Version 2/2M ColdFire Core Processor User's Manual Addendum	ColdFire2UMAD/D
SCF5249UM	SCF5249 User's Manual	SCF5249UM/D

8 Signal Descriptions

8.1 Introduction

This section describes the SCF5249 input and output signals. The signal descriptions as shown in Table 4 are grouped according to relevant functionality.

Table 4. SCF5249 Signal Index

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Address	A[23:1] A[25]/GPO8	23 address lines, address line 25 multiplexed with gpo8.	Out	X
Read-write control	RW_b	Bus write enable - indicates if read or write cycle in progress	Out	H
Output enable	OE	Output enable for asynchronous memories connected to chip selects	Out	negated
Data	D[31:16]	Data bus used to transfer word data	In/Out	Hi-Z
Synchronous row address strobe	SDRAS	Row address strobe for external SDRAM.	Out	negated
Synchronous column address strobe	SDCAS	Column address strobe for external SDRAM	Out	negated
SDRAM write enable	SDWE	Write enable for external SDRAM	Out	negated
SDRAM upper byte enable	SDUDQM	Indicates during write cycle if high byte is written	Out	
SDRAM lower byte enable	SDLDQM	Indicates during write cycle if low byte is written	Out	
SDRAM chip selects	SDRAMCS1	SDRAM chip select	Outt	negated
SDRAM chip selects	SDRAMCS2/GPIO7	SDRAM chip select	In/Out	negated
SDRAM clock enable	BCLKE	SDRAM clock enable	Out	
System clock	SCLK/GPIO10	SDRAM clock output	In/Out	

Table 4. SCF5249 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
ADC	EBUIN3/ADIN0/GPI38 EBUIN4/ADIN1/GPI39 RXD2/ADIN2/GPI28 CTS2/ADIN3/GPI31	Analog to Digital converter input signals	In/Out	
ADC	TOUT1/ADOUT/GPO35	Analog to digital convertor output signal.	In/Out	
QSPI clock	SCL/QSPI_CLK	QSPI clock signal	In/Out	
QSPI data in	SDA/QSPI_DIN	QSPI data input	In/Out	
QSPI data out	QSPIDOUT/GPIO26	QSPI data out	In/Out	
QSPI chip selects	QSPICS0/GPIO29 QSPICS1/GPIO24 QSPICS2/GPIO21 QSPICS3/GPIO22	QSPI chip selects	In/Out	
Crystal in	CRIN	Crystal input	In	
Reset In	RSTI	Processor Reset Input	In	
Freescale Test Mode	TEST[3:0]	Should always be low.	In	
High Impedance	HIZ	Assertion three-states all output signal pins.	In	
Debug Data	DDATA3/GPIO4 DDATA2/GPIO2 DDATA1/GPIO1 DDATA0/GPIO0	Displays captured processor data and break-point status.	In/Out	Hi-Z
Processor Status	PST3/GPIO62 PST2/GPIO61 PST1/GPIO60 PST0/GPIO59	Indicates internal processor status.	In/Out	Hi-Z
Processor clock	PSTCLK/GPO63	Processor clock output	Out	
Test Clock	TCK	Clock signal for IEEE 1149.1A JTAG.	In	
Test Reset/Development Serial Clock	$\overline{\text{TRST}}$/DSCLK	Multiplexed signal that is asynchronous reset for JTAG controller. Clock input for debug module.	In	
Test Mode Select/ Break Point	TMS/$\overline{\text{BKPT}}$	Multiplexed signal that is test mode select in JTAG mode and a hardware break-point in debug mode.	In	
Test Data Input / Development Serial Input	TDI/DSI	Multiplexed serial input for the JTAG or background debug module.	In	
Test Data Output/Development Serial Output	TDO/DSO	Multiplexed serial output for the JTAG or background debug module.	Out	
Note: The CMD_SDIO2, SDATA0_SDIO1, RSTO/SDATA2_BS2, A25, QSPI_CS1, QSPI_CS3, SDRAM_CS2, EBUOUT2, BUFENB2, SUBR, SFSY, RCK, SRE, LRCK3, SWE, and the SCLK3 signals are only used in the 160 MAPBGA package.				

8.4 SDRAM Controller Signals

The following SDRAM signals provide a seamless interface to external SDRAM. An SDRAM width of 16 bits is supported and can access as much as 64 Mybtes of memory. ADRAMs are not supported.

Table 5. SDRAM Controller Signals

SDRAM Signal	Description
Synchronous DRAM row address strobe	The $\overline{\text{SDRAS}}$ active low pin provides a seamless interface to the RAS input on synchronous DRAM
Synchronous DRAM Column Address Strobe	The $\overline{\text{SDCAS}}$ active low pin provides a seamless interface to CAS input on synchronous DRAM.
Synchronous DRAM Write	The $\overline{\text{SDWE}}$ active-low pin is asserted to signify that a SDRAM write cycle is underway. This pin outputs logic ‘1’ during read bus cycles.
Synchronous DRAM Chip Enable	The $\overline{\text{SD\_CS1}}$ and The $\overline{\text{SDRAM\_CS2}}$/GPIO7 active-low output signal is used during synchronous mode to route directly to the chip select of up to two SDRAM devices. The $\overline{\text{SDRAM\_CS2}}$/gpio7 can be programmed to be gpio using the GPIO-FUNCTION register.
Synchronous DRAM UDQM and LQDM signals	The DRAM byte enables UDMQ and LDQM are driven by the SDUDQM and SDLDQM byte enable outputs.
Synchronous DRAM clock	The DRAM clock is driven by the SCLK signal
Synchronous DRAM Clock Enable	The BCLKE active high output signal is used during synchronous mode to route directly to the SCKE signal of external SDRAMs. This signal provides the clock enable to the SDRAM.

NOTE

The SDRAM_CS2 signal is only used on the 160 MAPBGA package.

8.5 Chip Selects

There are two chip select outputs on the SCF5249 device. $\overline{\text{CS0}}$ and $\overline{\text{CS1}}$/GPIO58. The second signal is multiplexed with a GPIO signal. The active low chip selects can be used to access asynchronous memories. The interface is glueless.

8.6 ISA Bus

The SCF5249 supports an ISA bus. (No ISA DMA channel). Using the ISA bus protocol, reads and writes to up to two ISA bus peripherals are possible. For the first peripheral, CS2/IDE-$\overline{\text{DIOR}}$/GPIO13 and IDE-$\overline{\text{DIOW}}$/GPIO14 are the read and write strobe. For the second peripheral, CS3/$\overline{\text{SRE}}$/GPIO11 and $\overline{\text{SWE}}$/GPIO12 are the read and write strobe. Either peripheral can insert wait states by pulling IDE-IORDY/GPIO16

8.12 Digital Audio Interface Signals

Table 10. Digital Audio Interface Signals

Serial Module Signal	Description
Digital Audio In	The EBUIN1/GPI36, EBUIN2/GPI37, EBUIN3/ADIN0/GPI38, and EBUIN4/ADIN1/GPI39 multiplexed signals can serve as general purpose input or can be driven by various digital audio (IEC958) input sources. Both functionalities are always active. Input chosen for IEC958 receiver is programmed within the audio module. Input value on the 4 pins can always be read from the appropriate gpio register..
Digital Audio Out	The EBUOUT1_GPO36 and EBUOUT2_GPO37 multiplexed pins can serve as general purpose I/O or as digital audio (IEC958) output. EBUOUT1 is digital audio out for consumer mode, EBUOUT2 is digital audio out for professional mode. The functionality of the pins is programmed with the GPIO-FUNCTION and GPIO1-FUNCTION register. During reset, the pin is configured as a digital audio output.

NOTE

The EBUOUT2 signal is only used on the 160 MAPBGA package.

8.13 Subcode Interface

There is a 3-line subcode interface on the SCF5249. This 3-line subcode interface allows the device to format and transmit subcode in EIAJ format to a CD channel encoder device. The three signals are described in Table 11.

Table 11. Subcode Interface Signal

Signal name	Description
RCK/GPIO51	Subcode clock input. When pin is used as subcode clock, this pin is driven by the CD channel encoder.
SFSY/GPIO52	Subcode sync output This signal is driven high if a subcode sync needs to be inserted in the EFM stream.
SUBR/GPIO53	Subcode data output This signal is a subcode data out pin.

NOTE

The SUBR, SFSY, and the RCK signals are only used in the 160 MAPBGA package.

8.19.5 Processor Status

The processor status pins, PST0_GPIO59, PST1_GPIO60, PST2_GPIO61, and PST3_GPIO62, indicate the SCF5249 processor status. During debug mode, the timing is synchronous with the processor clock (PSTCLK) and the status is not related to the current bus transfer. .

Table 14. Processor Status Signal Encodings

PST[3:0]		Definition
(HEX)	(BINARY)	
$0	0000	Continue execution
$1	0001	Begin execution of an instruction
$2	0010	Reserved
$3	0011	Entry into user-mode
$4	0100	Begin execution of PULSE and WDDATA instructions
$5	0101	Begin execution of taken branch or Synch_PC[1]
$6	0110	Reserved
$7	0111	Begin execution of RTE instruction
$8	1000	Begin 1-byte data transfer on DDATA
$9	1001	Begin 2-byte data transfer on DDATA
$A	1010	Begin 3-byte data transfer on DDATA
$B	1011	Begin 4-byte data transfer on DDATA
$C	1100	Exception processing[2]
$D	1101	Emulator mode entry exception processing[2]
$E	1110	Processor is stopped, waiting for interrupt[2]
$F	1111	Processor is halted[2]

Notes:
4. Rev. B enhancement.
5. These encodings are asserted for multiple cycles.

8.20 BDM/JTAG Signals

The SCF5249 complies with the IEEE 1149.1A JTAG testing standard. The JTAG test pins are multiplexed with background debug pins.

8.20.1 Test Clock

TCK is the dedicated JTAG test logic clock that is independent of the SCF5249 processor clock. Various JTAG operations occur on the rising or falling edge of TCK. The internal JTAG controller logic is designed such that holding TCK high or low for an indefinite period of time will not cause the JTAG test logic to lose state information. If TCK will not be used, it should be tied to ground.

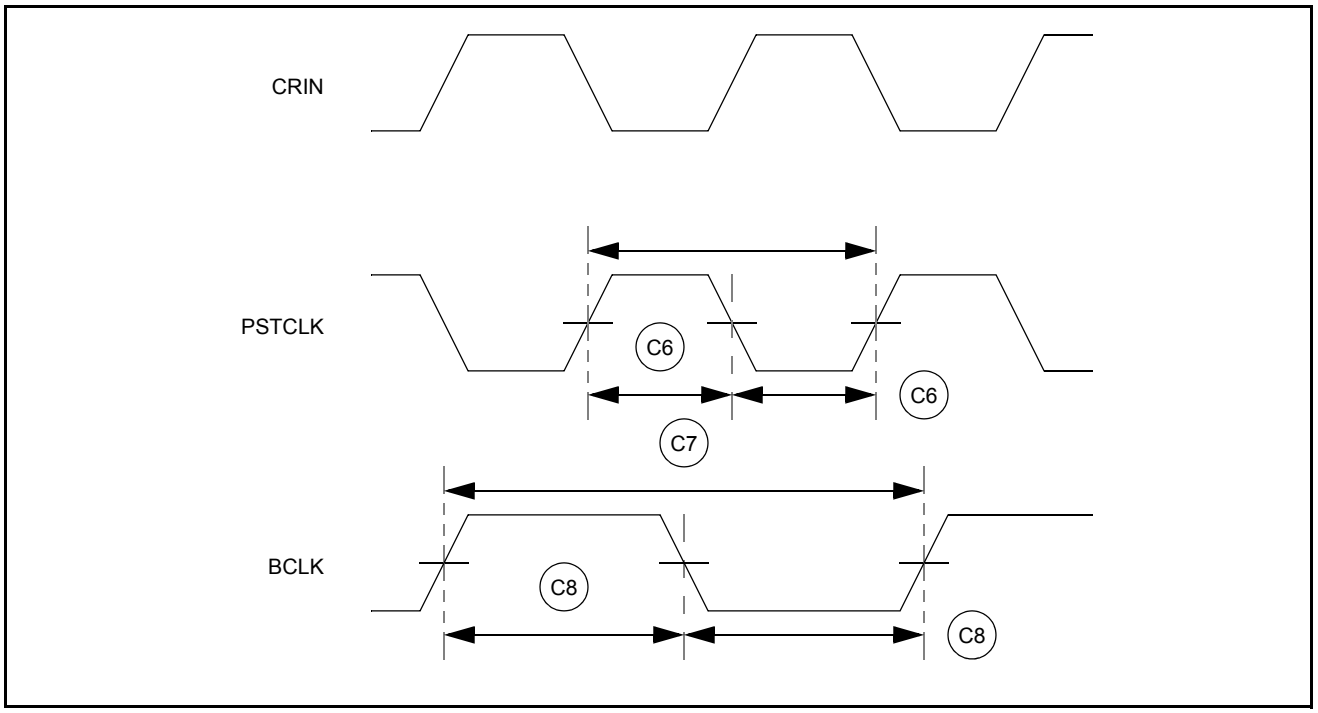

Figure 5. Clock Timing Definition

NOTE

Signals above are shown in relation to the clock. No relationship between signals is implied or intended.

9.1.1 Processor Bus Input Timing Specification

Table 20 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the SCLK output. All other timing relationships can be derived from these values.

Table 20. External Bus Input Timing Specifications

Num	Characteristic[a]				Units
		Symbol	Min	Max	
B0	SCLK	tCYC	14.26	—	ns
B1	Control input valid to SCLK high[b]	tCVCH	10	—	ns
B2	SCLK high to control inputs valid[b]	tCHCII	2	—	ns
B4	Data input (D[31:0]) valid to SCLK high	tDIVCH	6	—	ns

Table 20. External Bus Input Timing Specifications (continued)

Num	Characteristic[a]	Symbol	Min	Max	Units
B5	SCLK high to data input (D[31:0]) invalid	tCHDII	2	—	ns

a. Timing specifications have been indicated taking into account the full drive strength for the pads.
b. TA pin is being referred to as control input.

9.1.2 Processor Bus Output Timing Specifications

Table 21 lists processor bus output timings.

Table 21. External Bus Output Timing Specifications

NAME	CHARACTERISTIC	SYMBOL	MIN	MAX	UNIT
Control Outputs					
B6a	SCLK high to chip selects valid [a]	t_{CHCV}	—	$0.5t_{CYC}$ +10	ns
B6b	SCLK high to output enable ($\overline{OE}$) valid[b]	t_{CHOV}	—	$0.5t_{CYC}$ +10	ns
B7a	SCLK high to control output ($\overline{OE}$) invalid	t_{CHCOI}	$0.5t_{CYC}$ + 2	—	ns
B7b	SCLK high to chip selects invalid	t_{CHCI}	$0.5t_{CYC}$ + 2	—	ns
Address and Attribute Outputs					
B8	SCLK high to address (A[23:1]) and control (R/$\overline{W}$) valid	t_{CHAV}	—	10	ns
B9	SCLK high to address (A[23:1]) and control (R/$\overline{W}$) invalid	t_{CHAI}	2	—	ns
Data Outputs					
B11	SCLK high to data output (D[31:16]) valid	t_{CHDOV}	—	10	ns
B12	SCLK high to data output (D[31:16]) invalid	t_{CHDOI}	2	—	ns
B13	SCLK high to data output (D[31:16]) high impedance	t_{CHDOZ}	—	14	ns

a. $\overline{CS}n$ transitions after the falling edge of SCLK.
b. $\overline{OE}$ transitions after the falling edge of SCLK.

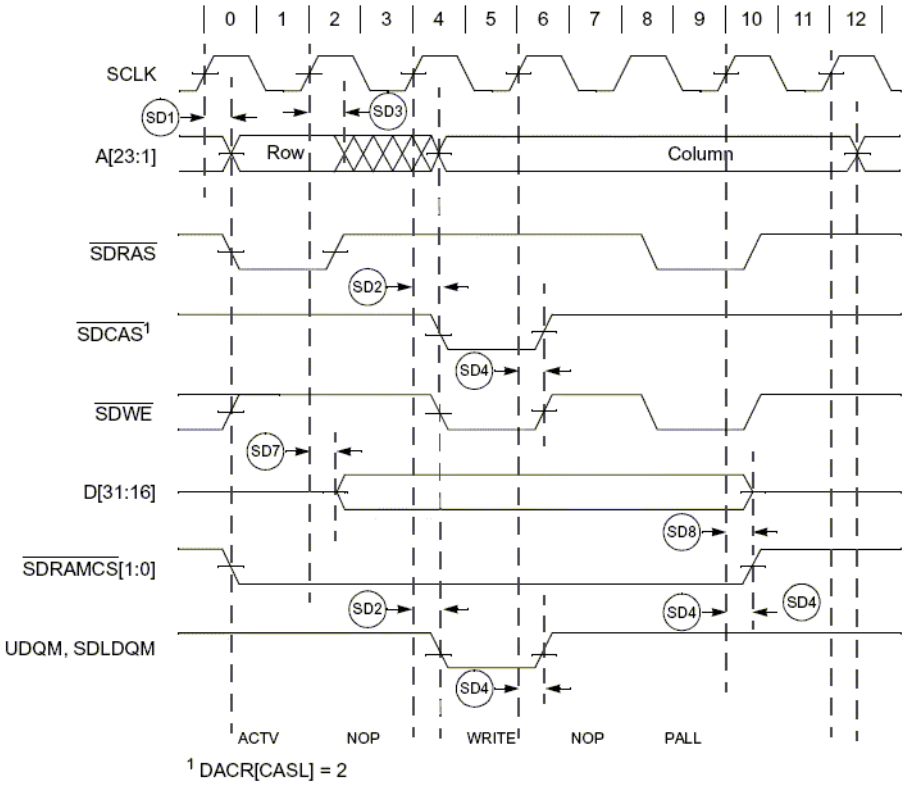

Figure 9. SDRAM Write Cycle

Table 23. Debug AC Timing Specification

Num	Characteristic	Min	Max	Units
D1	PSTCLK to signal Valid (Output valid)	---	6	nSec
D2	PSTCLK to signal Invalid (Output hold)	1.8	—	nSec
D3[1]	Signal Valid to PSTCLK (Input setup)	3	—	nSec
D4	PSTCLK to signal Invalid (Input hold)	5	—	nSec

1. DSCLK and DSI are internally synchronized. This setup time must be met only if recognition on a particular clock is required.
2. AC timing specs assume 50pF load capacitance on PSTCLK and output pins. If this value is different, the input and output timing specifications would need to be adjusted to match the clock load.

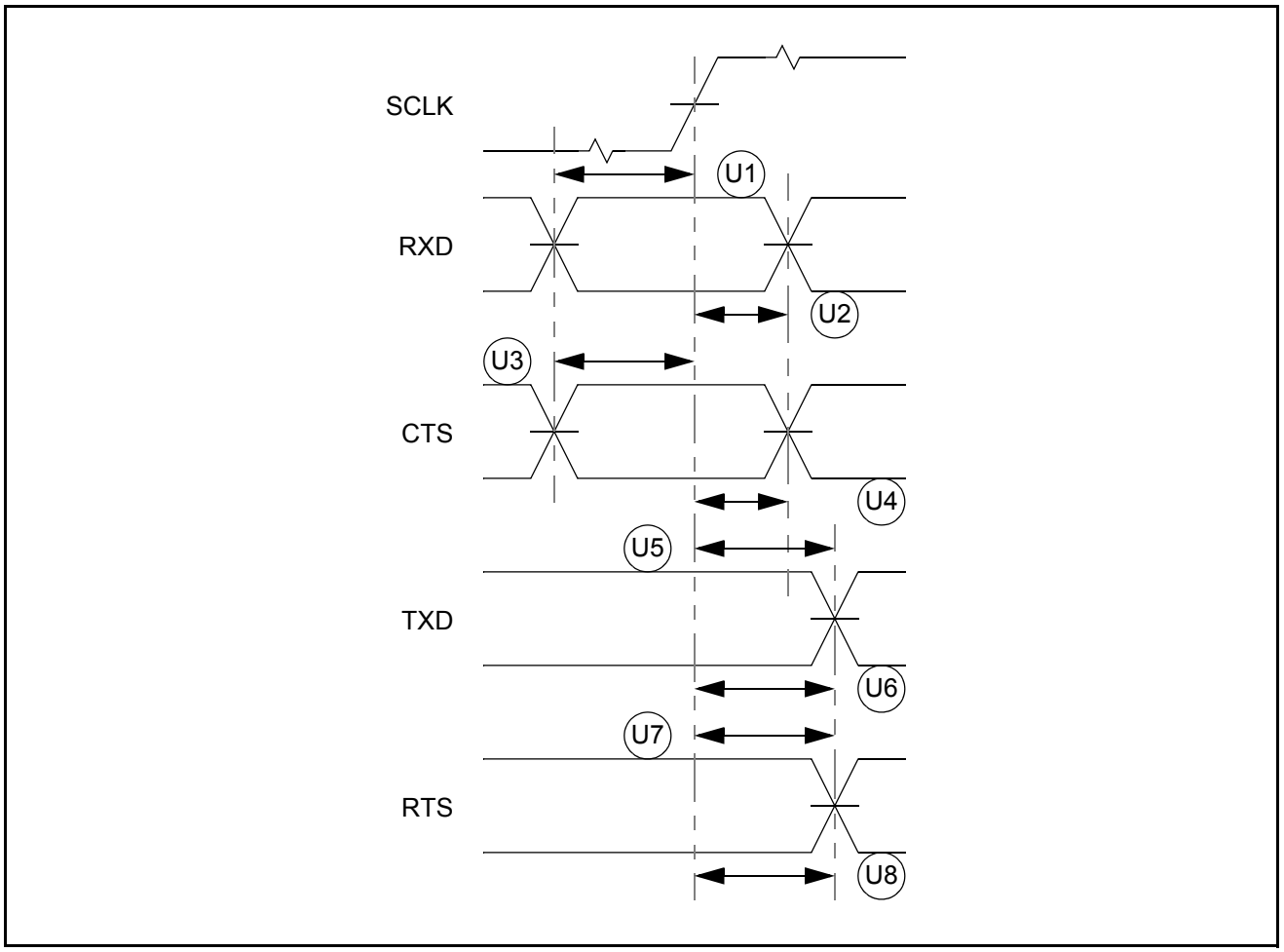

Figure 12. UART Timing Definition

Table 26. I2C-Bus Input Timing Specifications Between SCL and SDA

Num	Characteristic	Min	Max	Units
M1	Start Condition Hold Time	tbd	—	bus clocks
M2	Clock Low Period	tbd	—	bus clocks
M3	SCL/SDA Rise Time (VIL= 0.5 V to VIH = 2.4 V)	—	tbd	mSec
M4	Data Hold Time	tbd	—	nSec
M5	SCL/SDA Fall Time (VIH= 2.4 V to VIL = 0.5 V)	—	tbd	mSec
M6	Clock High time	tbd	—	bus clocks
M7	Data Setup Time	tbd	—	nSec
M8	Start Condition Setup Time (for repeated start condition only)	tbd	—	bus clocks

Table 26. I2C-Bus Input Timing Specifications Between SCL and SDA

Num	Characteristic	Min	Max	Units
M9	Stop Condition Setup Time	tbd	—	bus clocks

Table 27. I2C-Bus Output Timing Specifications Between SCL and SDA

Num	Characteristic	Min	Max	Units
M1[1]	Start Condition Hold Time	tbd	—	bus clocks
M2[1]	Clock Low Period	tbd	—	bus clocks
M3[2]	SCL/SDA Rise Time (V_{IL}= 0.5 V to V_{IH} = 2.4 V)	—	tbd	mSec
M4[1]	Data Hold Time	tbd	—	bus clocks
M5[3]	SCL/SDA Fall Time (V_{IH}= 2.4 V to V_{IL} = 0.5 V)	—	tbd	nSec
M6[1]	Clock High time	tbd	—	bus clocks
M7[1]	Data Setup Time	tbd	—	bus clocks
M8[1]	Start Condition Setup Time (for repeated start condition only)	tbd	—	bus clocks
M9[1]	Stop Condition Setup Time	tbd	—	bus clocks

1. Note: Output numbers are dependent on the value programmed into the MFDR; an MFDR programmed with the maximum frequency (MFDR = 0x20) will result in minimum output timings as shown in the above table. The MBUS interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the MFDR; however, numbers given in the above table are the minimum values.
2. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
3. Specified at a nominal 20 pF load.

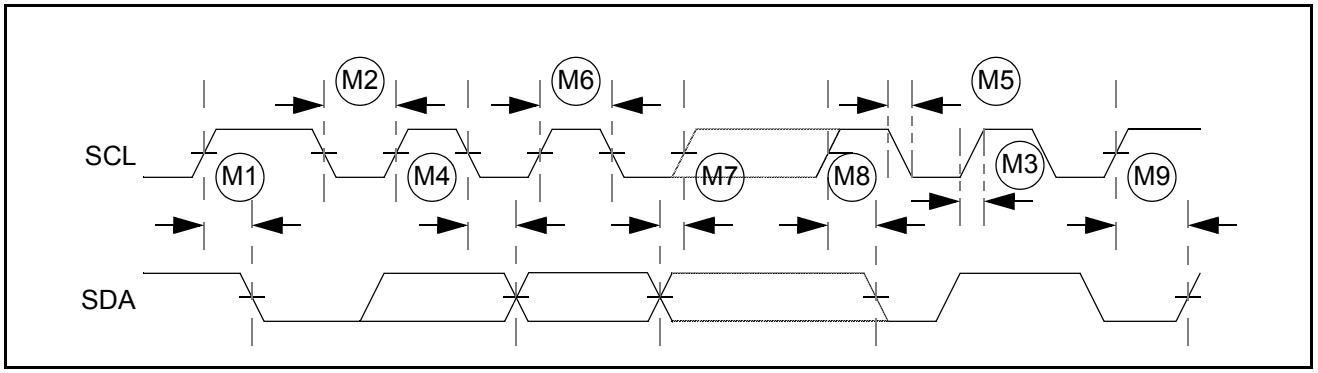

Figure 13. I2C Timing Definition

Table 28. I2C Output Bus Timings

Num	Characteristic	Min	Max	Units
M10[3]	SCL, SDA Valid to SCLK (input setup)	tbd	—	nSec
M11	SCLK to SCL, SDA Invalid (input hold)	tbd	—	nSec
M12[1]	SCLK to SCL, SDA Low (output valid)	—	tbd	nSec
M13[2]	SCLK to SCL, SDA Invalid (output hold)	tbd	—	nSec

1. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are driven low by the processor. The time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
2. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are actively being driven or held low by the processor.
3. SCL and SDA are internally synchronized.This setup time must be met only if recognition on a particular clock is required.

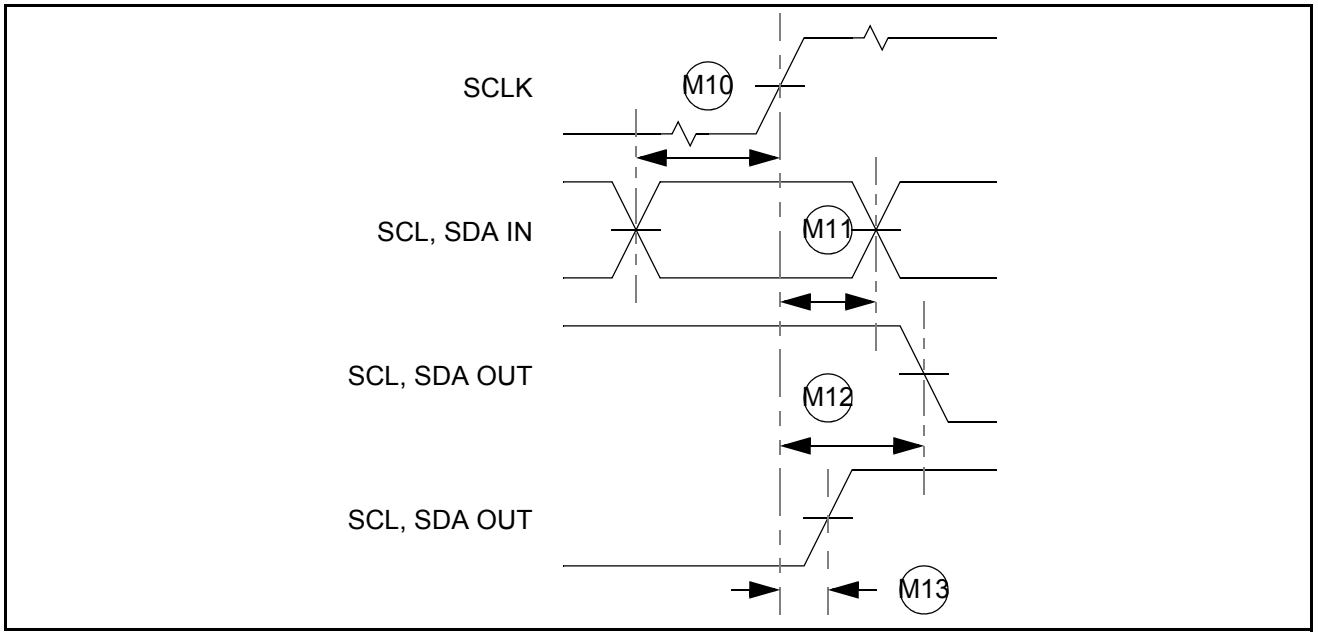

Figure 14. I²C and System Clock Timing Relationship

Table 29. General-Purpose I/O Port AC Timing Specifications

Num	Characteristic	Min	Max	Units
P1	GPIO Valid to SCLK (input setup)	tbd	—	nSec
P2	SCLK to GPIO Invalid (input hold)	tbd	—	nSec

Table 29. General-Purpose I/O Port AC Timing Specifications

Num	Characteristic	Min	Max	Units
P3	SCLK to GPIO Valid (output valid)	—	tbd	nSec
P4	SCLK to GPIO Invalid (output hold)	tbd	—	nSec

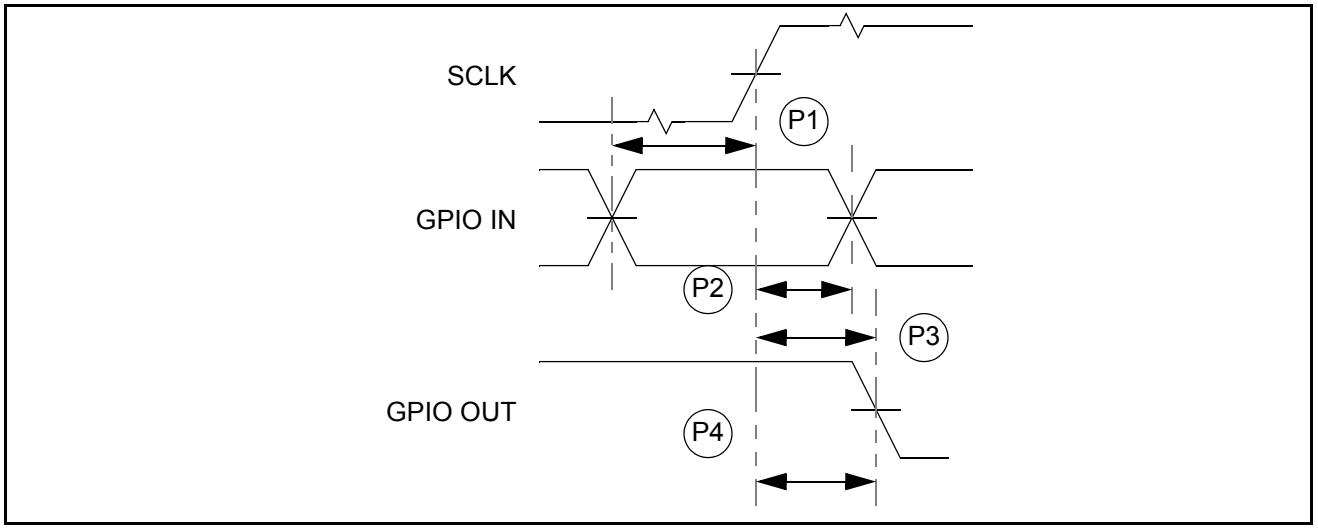

Figure 15. General-Purpose Parallel Port Timing Definition

Table 30. IEEE 1149.1 (JTAG) AC Timing Specifications

Num	Characteristic	Min	Max	Units
-	TCK Frequency of Operation	0	10	MHz
J1	TCK Cycle Time	100	-	nSec
J2a	TCK Clock Pulse High Width	25	-	nSec
J2b	TCK Clock Pulse Low Width	25	-	nSec
J3a	TCK Fall Time (V_{IH}=2.4 V to V_{IL}=0.5 V)	—	5	nSec
J3b	TCK Rise Time (V_{IL}=0.5 v to V_{IH}=2.4 V)	—	5	nSec
J4	TDI, TMS to TCK rising (Input Setup)	8	—	nSec
J5	TCK rising to TDI, TMS Invalid (Hold)	10	—	nSec
J6	Boundary Scan Data Valid to TCK (Setup)	tbd	—	nSec
J7	TCK to Boundary Scan Data Invalid to rising edge (Hold)	tbd	—	nSec

Table 34. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description
10	SCLK_OUT/GPIO15	I/O	MemoryStick/SD
11	BCLKE	O	sdram clock enable output
12	SDA/QSPI_DIN	I/O	IIC data/QSPI data in function select is PLLCR(11)
13	DATA24	I/O	data
14	A22	O	SDRAM address / static adr
15	SDUDQM	O	SDRAM UDQM
16	EF/GPIO19	I/O	error flag input
17	DATA25	I/O	data
18	DATA26	I/O	data
19	DATA27	I/O	data
20	PAD-GND		PAD-GND
21	DATA28	I/O	data
22	DATA29	I/O	data
23	SDATA3/GPIO56	I/O	SD interface data line
24	DATA30	I/O	data
25	BUFENB1/GPIO57	I/O	external buffer 1 enable
26	DATA31	I/O	data
27	CORE-VDD		CORE-VDD
28	A13	O	SDRAM address / static adr
29	CORE-GND		CORE-GND
30	A23	O	SDRAM address / static adr
31	A14	O	SDRAM address / static adr
32	A15	O	SDRAM address / static adr
33	A16	O	SDRAM address / static adr
34	PAD-VDD		PAD-VDD
35	A19	O	SDRAM address / static adr

Table 34. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description
36	A20	O	SDRAM address / static adr
37	TEST2	I	test
38	SDRAM-CS1	O	SDRAM chip select out 1
39	SDATA1_BS1/GPIO9	I/O	Memory Stick / SD
40	SDRAS	O	SDRAM RAS
41	SDCAS	O	SDRAM CAS
42	SDWE	O	SDRAM write enable
43	SDLDQM	O	SDRAM LDQM
44	GPIO5	I/O	GPIO5
45	QSPI_CS0/GPIO29	I/O	QSPI chip select 0
46	QSPI_DOUT/GPIO26	I/O	QSPI data out
47	GPIO6	I/O	GPIO6
48	DATA21	I/O	data
49	DATA19	I/O	data
50	QSPI_CS2/GPIO21	I/O	QSPI chip select 2
51	DATA20	I/O	data
52	DATA22	I/O	data
53	DATA18	I/O	data
54	DATA23	I/O	data
55	DATA17	I/O	data
56	PADD-VDD		PAD-VDD
57	DATA16	I/O	data
58	CFLG/GPIO18	I/O	CFLG input
59	EBUOUT1/GPO36	O	audio interfaces EBU out 1
60	CORE-GND		CORE-GND
61	EBUIN3/ADIN0/GPI38	I	audio interfaces EBU in 3 / AD convertor input0

Table 34. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description
62	EBUIN2/GPI37	I	audio interfaces EBU in 2
63	CORE-VDD		CORE-VDD
64	SCL2/GPIO3	I/O	IIS2 clock line
65	RSTI	I	Reset
66	TOUT1/ADOUT/GPO35	O	timer output 1 / AD output
67	LRCK2/GPIO44	O	audio interfaces EBU out 1
68	OE	O	Output Enable
69	SDA2/GPIO55	I/O	IIS2 data
70	SDATAO2/GPO41	O	audio interfaces serial data output 2
71	SCLK2/GPIO48	I/O	audio interfaces serial clock 2
72	PAD-GND		PAD-GND
73	TEST3	I	test
74	SDATAO1/GPIO25	I/O	audio interfaces serial data output 1
75	LRCK1	I/O	audio interfaces word clock 1
76	LRCK4/GPIO46	I/O	audio interfaces word clock 4
77	SDATAI4/GPI42	I	audio interfaces serial data in 4
78	SCLK1	I/O	audio interfaces serial clock 1
79	SCLK4/GPIO50	I/O	audio interfaces serial clock 4
80	TA/GPIO20	I/O	Transfer acknowledge
81	SDATAI1	I	audio interfaces serial data in 1
82	EBUIN1/GPI36	I	audio interfaces EBU in 1
83	PLLGRDVDD		PLLGRDVDD
84	PLLGRDGND		PLLGRDGND
85	PLLPADGND		PLLPADGND
86	PLLPADVDD		PLLPADVDD
87	PLLCOREGND		PLLCOREGND
88	PLLCOREVDD		PLLCOREVDD

Table 34. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description
141	CORE-VDD		CORE-VDD
142	A12	O	address
143	TEST1	I	test
144	PAD-VDD		PAD-VDD

10.2 Package

The SCF5249 is assembled in 144-pin QFP package. Thermal characteristics are not available at this time.

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