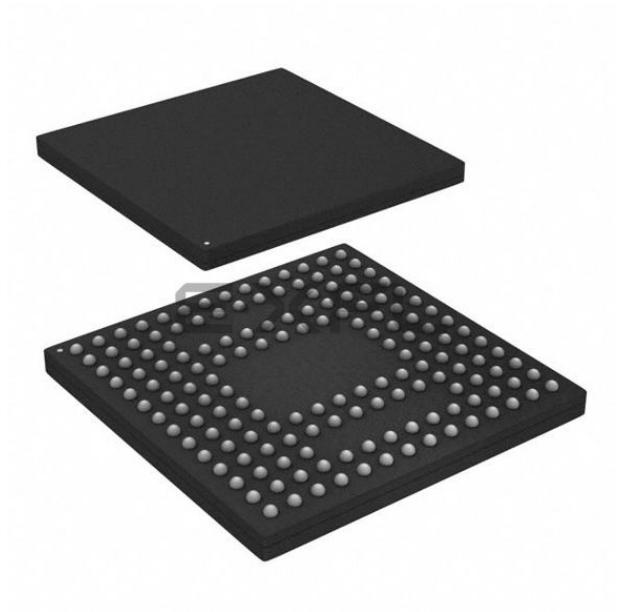

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	140MHz
Connectivity	I²C, IDE, Memory Card, SPI, UART/USART
Peripherals	DMA, I²S, POR, Serial Audio, WDT
Number of I/O	47
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	160-BGA
Supplier Device Package	160-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/scf5249vm140

integrated peripherals and EMAC allow the SCF5249 to replace both the microcontroller and the DSP in certain applications. Most peripheral pins can also be remapped as General Purpose I/O pins.

1.1 Orderable Parts Numbers

1.1.1 Orderable Part Table

Table 1. Orderable Part Numbers

Orderable Part Number	Maximum Clock Frequency	Package Type	Operating Temperature Range	Part Status
SCF5249LPV120	120 MHz	144 pin QFP	-20°C to 70°C	Leaded
SCF5249LAG120	120 MHz	144 pin QFP	-20°C to 70°C	Lead Free
SCF5249VF140	140 MHz	160 ball MAPBGA	-20°C to 70°C	Leaded
SCF5249VM140	140 MHz	160 ball MAPBGA	-20°C to 70°C	Lead Free

1.2 SCF5249 Features

The SCF5249 integrated microprocessor combines a Version 2 ColdFire® processor core operating at 140MHz with the following modules.

- DMA controller with 4 DMA channels
- Integrated Enhanced Multiply-accumulate Unit (EMAC)
- 8-KByte Direct Mapped Instruction Cache
- 96-KByte SRAM (A 64K and a 32K bank)
- Operates from external crystal oscillator
- Supports 16-bit wide SDRAM memories
- Serial Audio Interface which supports IIS and EIAJ audio protocols
- Digital audio transmitter and two receivers compliant with IEC958 audio protocol
- CD-ROM and CD-ROM XA block decoding and encoding function
- Two UARTS
- Queued Serial Peripheral Interface (QSPI) (Master Only)
- Two timers
- IDE and SmartMedia interfaces
- Analog/Digital Converter
- Flash Memory Card Interface
- Two I^2C modules
- System debug support
- General Purpose I/O pins shared with other functions

- 1.8V core, 3.3V I/O
- 160 pin MAPBGA package (qualified at 140 MHz) and 144 pin QFP package (qualified at 120 MHz)
- -20^0 C to 70^0 C ambient operating temperature range

2 SCF5249 Block Diagram

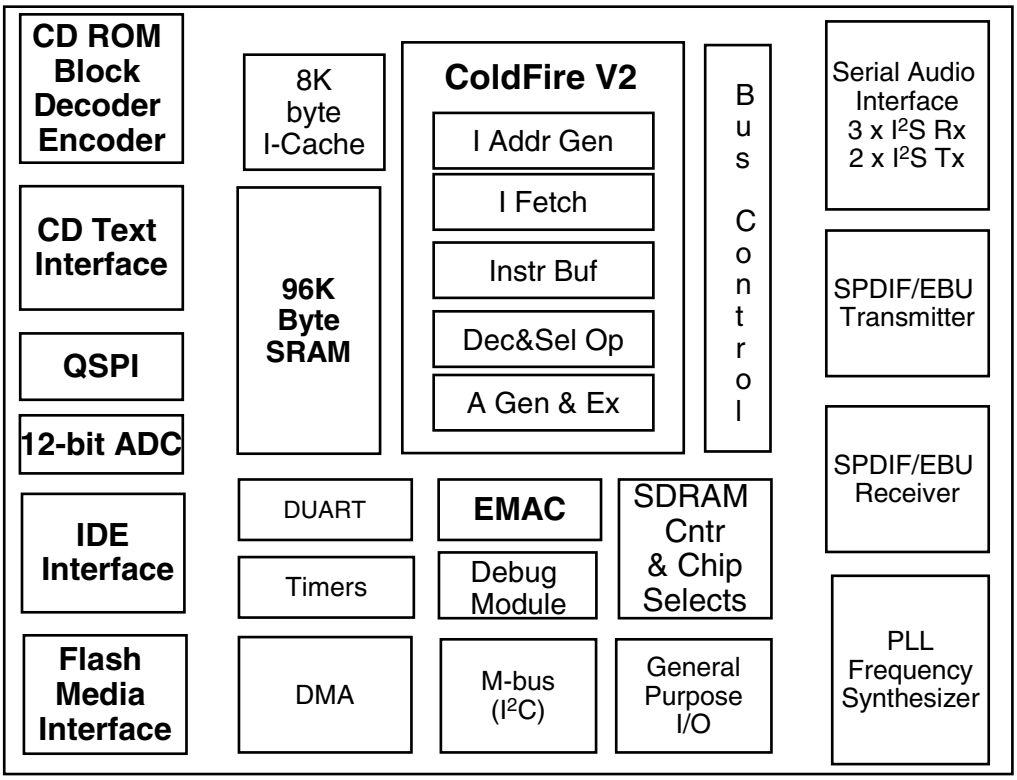

Figure 1. SCF5249 Block Diagram

3 SCF5249 Feature Details

The primary features of the SCF5249 integrated processor include the following:

- ColdFire V2 Processor Core operating at 140MHz
  - — Clock-doubled Version 2 microprocessor core
  - — 32-bit internal data bus, 16 bit external data bus
  - — 16 user-visible, 32-bit general-purpose registers
  - — Supervisor/user modes for system protection
  - — Vector base register to relocate exception-vector table
  - — Optimized for high-level language constructs

- DMA controller
  - Four fully programmable channels: Two dedicated to the audio interface module and two dedicated to the UART module (External requests are not supported.)
  - Supports dual- and single-address transfers with 32-bit data capability
  - Two address pointers that can increment or remain constant
  - 16-/24-bit transfer counter
  - Operand packing and unpacking support
  - Auto-alignment transfers supported for efficient block movement
  - Supports bursting and cycle stealing
  - All channels support memory to memory transfers
  - Interrupt capability
  - Provides two clock cycle internal access
- Enhanced Multiply-accumulator Unit
  - Single-cycle multiply-accumulate operations for 32 x 32 bit and 16 x 16 bit operands
  - Support for signed, unsigned, integer, and fixed-point fractional input operands
  - Four 48-bit accumulators to allow the use of a 40-bit product
  - The addition of 8 extension bits to increase the dynamic number range
  - Fast signed and unsigned integer multiplies
- 8-KByte Direct Mapped instruction cache
  - Clock-doubled to match microprocessor core speed
  - Flush capability
  - Non-blocking cache provides fast access to critical code and data
- 96-KByte SRAM
  - Provides one-cycle access to critical code and data
  - Split into two banks, SRAM0 (32K), and SRAM1 (64K)
  - DMA requests to/from internal SRAM1 supported
- Crystal Trim
  - The XTRIM output can be used to trim an external crystal oscillator circuit which would allow lock with an incoming IEC958 or serial audio signal
- Audio Interfaces
  - IEC958 input and output
  - Four serial Philips IIS/Sony EIAJ interfaces
    - One with input and output, one with output only, two with input only (Three inputs, two outputs)
    - Master and Slave operation

- System debug support
  - Real-time instruction trace for determining dynamic execution path
  - Background debug mode (BDM) for debug features while halted
  - Debug exception processing capability
  - Real-time debug support
- System Interface
  - Glueless bus interface with four chip selects and DRAMC support for interface to 16-bit for DRAM, SRAM, ROM, FLASH, and I/O devices
    - Two programmable chip-select signals for static memories or peripherals, with programmable wait states and port sizes.
    - Two dedicated chip selects for 16-bit wide DRAM /SDRAM.
    - CS0 is active after reset to provide boot-up from external FLASH/ROM.
  - Programmable interrupt controller
    - Low interrupt latency
    - Eight external interrupt requests
    - Programmable autovector generator
  - 44 programmable general-purpose inputs*
  - 46 programmable general-purpose outputs*
    - * For the 160 MAPBGA package
  - IEEE 1149.1 Test (JTAG) Module
- Clocking
  - Clock-multiplied PLL, programmable frequency
- 1.8V Core, 3.3V I/O
- 160 pin MAPBGA package (qualified at 140 MHz) and 144 pin QFP package (qualified at 120 MHz)

4 160 MAPBGA Ball Assignments

The following signals are not available on the 144 QFP package.

NOTE

The 144 QFP part is qualified for 120 MHz operation. The 160MAPBGA part is qualified for 140 MHz.

Table 2. 160 MAPBGA Ball Assignments

160 MAPBGA Ball Number	Function	GPIO
E3	cmd_sdio2	gpio34
G4	sdata0_sdio1	gpio54
H3	RSTO/sdata2_bs2	
K3	A25	gpo8
L4	QSPI_CS1	gpio24
L8	QSPI_CS3	gpio22
N8	SDRAM_CS2	gpio7
P9	EbuOut2	gpo 37
K11	BUFENb2	gpio17
G12	subr	gpio 53
F13	sfsy	gpio 52
F12	rck	gpio 51
E8	SRE	gpio11
B8	lrck3	gpio 45
E7	SWE	gpio12
A7	sclk3	gpio 49

5 SCF5249 Functional Overview

5.1 ColdFire V2 Core

The ColdFire processor Version 2 core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, which minimizes time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC data path with a dual-read-ported register file feeding an arithmetic/logic unit (ALU).

5.2 DMA Controller

The SCF5249 provides four fully programmable DMA channels for quick data transfer. Single and dual address mode is supported with the ability to program bursting and cycle stealing. Data transfer is selectable as 8, 16, 32, or 128-bits. Packing and unpacking is supported.

Two internal audio channels and the dual UART can be used with the DMA channels. All channels can perform memory to memory transfers. The DMA controller has a user-selectable, 24- or 16-bit counter and a programmable DMA exception handler.

External requests are not supported.

5.3 Enhanced Multiply and Accumulate Module (EMAC)

The integrated EMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture. The EMAC provides functionality in three related areas:

1. Faster signed and unsigned integer multiplies
2. New multiply-accumulate operations supporting signed and unsigned operands
3. New miscellaneous register operations

Multiplies of 16x16 and 32x32 with 48-bit accumulates are supported in addition to a full set of extensions for signed and unsigned integers plus signed, fixed-point fractional input operands. The EMAC has a single-clock issue for 32x32-bit multiplication instructions and implements a four-stage execution pipeline.

5.4 Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The SCF5249 processor uses a 8K-byte, direct-mapped instruction cache to achieve 125 MIPS at 140 Mhz. The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit. The instruction cache also includes a bursting interface for 16-bit and 8-bit port sizes to quickly fill cache lines.

5.5 Internal 96-KByte SRAM

The 96-KByte on-chip SRAM is split over two banks, SRAM0 (32k) and SRAM1 (64K). It provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance. Memory in the second bank can be accessed under DMA.

5.6 DRAM Controller

The SCF5249 DRAM controller provides a glueless interface for up to two banks of DRAM, each of which can be up to 32 MBytes. The controller supports a 16-bit data bus. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMS.

5.7 System Interface

The SCF5249 provides a glueless interface to 16-bit port size SRAM, ROM, and peripheral devices with independent programmable control of the assertion and negation of chip-select and write-enable signals.

The SCF5249 also supports bursting ROMs.

5.8 External Bus Interface

The bus interface controller transfers information between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus. The external bus interface provides 23 bits of address bus space, a 16-bit data bus, Output Enable, and Read/Write signals. This interface implements an extended synchronous protocol that supports bursting operations.

5.9 Serial Audio Interfaces

The SCF5249 digital audio interface provides four serial Philips IIS/Sony EIAJ interfaces. One interface is a 4-pin (1 bit clock, 1 word clock, 1 data in, 1 data out), the other three interfaces are 3-pin (1 bit clock, 1 word clock, 1 data in or out). The serial interfaces have no limit on minimum sampling frequency. Maximum sampling frequency is determined by maximum frequency on bit clock input. This is 1/3 the frequency of the internal system clock.

5.10 IEC958 Digital Audio Interfaces

The SCF5249 has two digital audio input interfaces, and one digital audio output interface. There are four digital audio input pins, two digital audio output pins. An internal multiplexer selects one of the four inputs to the digital audio input interface. There is one digital audio output interface but it has two IEC958 outputs. One output carries the professional “c” channel, and the other carries the consumer “c” channel. The rest carry identical data.

The IEC958 output can take the output from the internal IEC958 generator, or multiplex out one of the four IEC958 inputs.

5.11 Audio Bus

The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission. Each transmitter has a source select register.

In addition to the audio interfaces, there are six CPU accessible registers connected to the audio bus. Three of these registers allow data reads from the audio bus and allow selection of the audio source. The other three register provide a write path to the audio bus and can be selected by transmitters as the audio source. Through these registers, the CPU has access to the audio samples for processing.

Audio can be routed from a receiver to a transmitter without the data being processed by the core so the audio bus can be used as a digital audio data switch. The audio bus can also be used for audio format conversion.

5.12 CD-ROM Encoder/Decoder

The SCF5249 is capable of processing CD-ROM sectors in hardware. Processing is compliant with CD-ROM and CD-ROM XA standards.

5.16 IDE and SmartMedia Interfaces

The SCF5249 system bus allows connection of an IDE hard disk drive and SmartMedia flash card with a minimum of external hardware. The external hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses to propagate to the IDE bus. The control signals for the buffers are generated in the SCF5249.

5.17 Analog/Digital Converter (ADC)

The four channel ADC is a based on the Sigma-Delta concept with 12-bit resolution. The digital portion of the ADC is provided internally. The analog voltage comparator must be provided externally as well as an external integrator circuit (resistor/capacitor) which is driven by the ADC output. A software interrupt is provided when the ADC measurement cycle is complete.

5.18 Flash Memory Card Interface

The interface is Sony MemoryStick and SecureDigital compatible. However, there is no hardware support for MagicGate.

5.19 I^2C Module

The two-wire I^2C bus interface, which is compliant with the Philips I^2C bus standard, is a bidirectional serial bus that exchanges data between devices. The I^2C bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

5.20 Chip-Selects

Two programmable chip-select outputs provide signals that enable glueless connection to external memory and peripheral circuits. The base address, access permissions and automatic wait-state insertion are programmable with configuration registers. These signals also interface to 16-bit ports.

CS0 is active after reset to provide boot-up from external FLASH/ROM.

5.21 GPIO Interface

A total of 44 General Purpose inputs and 46 General Purpose outputs are available. These are multiplexed with various other signals. Eight of the GPIO inputs have edge sensitive interrupt capability.

5.22 Interrupt Controller

The interrupt controller provides user-programmable control of a total of 57 interrupts. There are 49 internal interrupt sources. In addition, there are 8 GPIOs where interrupts can be generated on the rising or falling edge of the pin. All interrupts are autovectored and interrupt levels are programmable.

Table 3. SCF5249 Documentation

Document Name	Description	Order Number
CFPRM/D	ColdFire Family Programmer's Reference Manual	CFPRM/D
ColdFire2UM	Version 2/2M ColdFire Core Processor User's Manual	ColdFire2UM/D
ColdFire2UMAD	Version 2/2M ColdFire Core Processor User's Manual Addendum	ColdFire2UMAD/D
SCF5249UM	SCF5249 User's Manual	SCF5249UM/D

8 Signal Descriptions

8.1 Introduction

This section describes the SCF5249 input and output signals. The signal descriptions as shown in Table 4 are grouped according to relevant functionality.

Table 4. SCF5249 Signal Index

Signal Name	Mnemonic	Function	Input/ Output	Reset State
Address	A[23:1] A[25]/GPO8	23 address lines, address line 25 multiplexed with gpo8.	Out	X
Read-write control	RW_b	Bus write enable - indicates if read or write cycle in progress	Out	H
Output enable	OE	Output enable for asynchronous memories connected to chip selects	Out	negated
Data	D[31:16]	Data bus used to transfer word data	In/Out	Hi-Z
Synchronous row address strobe	SDRAS	Row address strobe for external SDRAM.	Out	negated
Synchronous column address strobe	SDCAS	Column address strobe for external SDRAM	Out	negated
SDRAM write enable	SDWE	Write enable for external SDRAM	Out	negated
SDRAM upper byte enable	SDUDQM	Indicates during write cycle if high byte is written	Out	
SDRAM lower byte enable	SDLDQM	Indicates during write cycle if low byte is written	Out	
SDRAM chip selects	SDRAMCS1	SDRAM chip select	Outt	negated
SDRAM chip selects	SDRAMCS2/GPIO7	SDRAM chip select	In/Out	negated
SDRAM clock enable	BCLKE	SDRAM clock enable	Out	
System clock	SCLK/GPIO10	SDRAM clock output	In/Out	

Table 4. SCF5249 Signal Index (continued)

Signal Name	Mnemonic	Function	Input/ Output	Reset State
IEC958 inputs	EBUIN1/GPI36 EBUIN2/GPI37 EBUIN3/ADIN0/GPI38 EBUIN4/ADIN1/GPI39	Audio interfaces IEC958 inputs multiplexed with some A/D inputs	In	
IEC958 outputs	EBUOUT1/GPO36 EBUOUT2/GPO37	Audio interfaces IEC958 outputs	Out	
Serial data in	SDATAI1 SDATAI3/GPI41 SDATA14/GPI42	Audio interfaces serial data inputs	In	
Serial data out	SDATAO1/GPIO25 SDATAO2/GPO41	Audio interfaces serial data outputs	In/Out Out	
Word clock	LRCK1 LRCK2/GPIO44 LRCK3/GPIO45 LRCK4/GPIO46	Audio interfaces serial word clocks	In/Out	
Bit clock	SCLK1 SCLK2/GPIO48 SCLK3/GPIO49 SCLK4/GPIO50	Audio interfaces serial bit clocks	In/Out	
Serial input	EF/GPIO19	Error flag serial in	In/Out	
Serial input	CFLG/GPIO18	C-flag serial in	In/Out	
Subcode clock	RCK/GPIO51	Audio interfaces subcode clock	In/Out	
Subcode sync	SFSY/GPIO52	Aaudio interfaces subcode sync	In/Out	
Subcode data	SUBR/GPIO53	Audio interfaces subcode data	In/Out	
Clock frequency trim	XTRIM/GPO38	Clock trim control	Out	
Audio clocks out	MCLK1/GPIO39 MCLK2/GPIO42	DAC output clocks	Out	
MemoryStick/SecureDigital interface	CMDSDIO2/GPIO34	Secure Digital command lane MemoryStick interface 2 data i/o	In/Out	
	SCLKOUT/GPIO15	Clock out for both MemoryStick interfaces and for Secure Digital	In/Out	
	SDATA0_SDIO1/GPIO54	SecureDigital serial data bit 0 MemoryStick interface 1 data i/o	In/Out	
	SDATA1_BS1/GPIO9	SecureDigital serial data bit 1 MemoryStick interface 1 strobe	In/Out	
	RSTO/SDATA2_BS2	SecureDigital serial data bit 2 MemoryStick interface 2 strobe Reset output signal	In/Out	
	SDATA3/GPIO56	SecureDigital serial data bit 3	In/Out	

Table 7. Serial Module Signals

Serial Module Signal	Description
Receive Data	The RXD1_GPI27 and RXD2/ADIN2/GPI28 are the inputs on which serial data is received by the DUART. Data is sampled on RxD[1:0] on the rising edge of the serial clock source, with the least significant bit received first.
Transmit Data	The DUART transmits serial data on the TXD1/GPO27 and TXD2/GPO28 output signals. Data is transmitted on the falling edge of the serial clock source, with the least significant bit transmitted (LSB) first. When no data is being transmitted or the transmitter is disabled, these two signals are held high. TxD[1:0] are also held high in local loopback mode.
Request To Send	The $\overline{\text{RTS1}}$/GPO30 and $\overline{\text{RTS2}}$/GPO31 request-to-send outputs indicate to the peripheral device that the DUART is ready to send data and requires a clear-to-send signal to initiate transfer.
Clear To Send	Peripherals drive the $\overline{\text{CTS1}}$/GPI30 and $\overline{\text{CTS2}}$/ADIN3/GPI31 inputs to indicate to the SCF5249 serial module that it can begin data transmission.

8.10 Timer Module Signals

The following signals are external interface to the two general-purpose SCF5249 timers. These 16-bit timers can capture timer values, trigger external events, or internal interrupts, or count external events. These pins can be reused as GPO or GPI. Registers GPIO-FUNCTION and GPIO1-FUNCTION must be programmed for this.

Table 8. Timer Module Signals

Serial Module Signal	Description
Timer Input	Users can program the TIN0/GPI33 and TIN1/GPIO23 inputs as clocks that cause events in the counter and prescalars. They can also cause capture on the rising edge, falling edge, or both edges.
Timer Output	The TOUT0/GPO33 and TOUT1/ADOUT/GPO35 programmable outputs pulse or toggle on various timer events.

8.11 Serial Audio Interface Signals

All serial audio interface signals can be programmed to serve as general purpose I/Os or as serial audio interface signals. The function is programmed using GPIO-FUNCTION and GPIO1-FUNCTION registers.

NOTE

The LRCK3 and SCLK3 signals are only used in the 160 MAPBGA package..

8.14 Analog to Digital Converter (ADC)

The single output on the TOUT1/ADOUT/GPO35 pin provides the reference voltage in PDM format therefore this output requires an external integrator circuit (resistor/capacitor) to convert it to a DC level to be used by the external comparator circuit. Four external comparators compare the DC level obtained after filtering TOUT1/ADOUT/GPO35 with the relevant input signals. The outputs of the comparators are fed to the 4 ADIN inputs on the SCF5249: EBUIN3/ADIN0/GPI38, EBUIN4/ADIN1/GPI39, RXD2/ADIN2/GPI38 and CTS2/ADIN3/GPI31. Selection of function for pin TOUT1/ADOUT/GPO35 is done by writing GPIO function select register (determines if function is GPIO or not), and differentiation between timer and adout functions is done in the ADCONFIG Register.

8.15 Secure Digital/ MemoryStick Card Interface

The device has a versatile flash card interface that supports both SecureDigital and MemoryStick cards. The interface can either support one SecureDigital or two MemoryStick cards. No mixing of card types is possible. Table 12 gives the pin descriptions.

Table 12. Flash Memory Card Signals

Flash Memory Signal	Description
SCLKOUT/GPIO15	Clock out for both MemoryStick interfaces and for SecureDigital
CMD_SDIO2/GPIO34	Secure Digital command line MemoryStick interface 2 data i/o
SDATA0_SDIO1/GPIO54	SecureDigital serial data bit 0 MemoryStick interface 1 data i/o
SDATA1_BS1/GPIO9	SecureDigital serial data bit 1 MemoryStick interface 1 strobe
RSTO/SDATA2_BS2	SecureDigital serial data bit 2 MemoryStick interface 2 strobe Reset output signal Selection between Reset function and SDATA2_BS2 is done by programming PLLCR register.
SDATA3/GPIO57	SecureDigital serial data bit 3

NOTE

The SDATA0_SDIO1 and RSTO/SDATA2_BS2 signals are only used in the 160 MAPBGA package.

8.16 Queued Serial Peripheral Interface (QSPI)

Table 13. Queued Serial Peripheral Interface (QSPI) Signals

Serial Module Signal	Description
SCL_QSPICLK	Multiplexed signal IIC interface clock or QSPI clock output Function select is done via PLLCR register.
SDA_QSPIDIN	Multiplexed signal IIC interface data or QSPI data input. Function select is done via PLLCR register.
QSPIDOUT_GPIO26	QSPI data output
QSPICS0_GPIO29	4 different QSPI chip selects
QSPICS1_GPIO24	
QSPICS2_GPIO21	
QSPICS3_GPIO22	

NOTE

The QSPI interface is a high-speed serial interface allowing transmit and receive of serial data.

8.17 Crystal Trim

The XTRIM_GPIO38 output produces a pulse-density modulated phase/frequency difference signal to be used after low-pass filtering to control varicap-voltage to control crystal oscillation frequency. This will lock the crystal to the incoming digital audio signal.

8.18 Clock Out

The MCLK1/GPO39 and /MCLK2/GPO42 can serve as general purpose I/Os or as DAC clock outputs. When programmed as DAC clock outputs, these signals are directly derived from the crystal.

8.19 Debug and Test Signals

These signals interface with external I/O to provide processor status signals.

8.19.1 Test Mode

The TEST[3:0] inputs are used for various manufacturing and debug tests. For normal mode these inputs should be always be tied low. Use TEST0 to switch between background debug mode and JTAG mode. Drive TEST0 high for debug mode.

8.19.2 High Impedance

The assertion of $\overline{\text{HI\_Z}}$ will force all output drivers to a high-impedance state. The timing on $\overline{\text{HI\_Z}}$ is independent of the clock.

8.20.2 Test Reset/Development Serial Clock

The TEST[3:0] signals determine the function of the $\overline{\text{TRST}}$/DSCLK dual-purpose pin. If TEST[3:0]=0001, the DSCLK function is selected. If TEST[3:0]= 0000, the TRST function is selected. TEST[3:0] should not be changed while $\overline{\text{RSTI}}$ = 1. When used as $\overline{\text{TRST}}$, this pin will asynchronously reset the internal JTAG controller to the test logic reset state, causing the JTAG instruction register to choose the ìbypassî command. When this occurs, all the JTAG logic is benign and will not interfere with the normal functionality of the SCF5249 processor. Although this signal is asynchronous, Freescale recommends that $\overline{\text{TRST}}$ make only a 0 to 1 (asserted to negated) transition while TMS is held at a logic 1 value. $\overline{\text{TRST}}$ has an internal pullup so that if it is not driven low its value will default to a logic level of 1. However, if $\overline{\text{TRST}}$ will not be used, it can either be tied to ground or, if TCK is clocked, it can be tied to VDD. If it is tied to ground, it will place the JTAG controller in the test logic reset state immediately. If it is tied to VDD, it will cause the JTAG controller (if TMS is a logic 1) to eventually end up in the test logic reset state after 5 clocks of TCK. This pin is also used as the development serial clock (DSCLK) for the serial interface to the Debug Module.The maximum frequency for the DSCLK signal is 1/5 the BCLKO frequency.

8.20.3 Test Mode Select/Break Point

The TEST[3:0] signals determine the TMS/$\overline{\text{BKPT}}$ pin function. If TEST[3:0] =0001, the $\overline{\text{BKPT}}$ function is selected. If TEST[3:0] = 0000, then the TMS function is selected. TEST[3:0] should not change while $_{\text{RSTI}}$ = 1. When used as TMS, this input signal provides the JTAG controller with information to determine which test operation mode should be performed. The value of TMS and current state of the internal 16-state JTAG controller state machine at the rising edge of TCK determine whether the JTAG controller holds its current state or advances to the next state. This directly controls whether JTAG data or instruction operations occur. TMS has an internal pullup so that if it is not driven low, its value will default to a logic level of 1. However, if TMS will not be used, it should be tied to VDD. This pin also signals a hardware breakpoint to the processor when in the debug mode.

8.20.4 Test Data Input/Development Serial Input

The TDI/DS is a dual-function pin. If TEST[3:0] = 0001, then DSI is selected. If TEST[3:0] = 0000, then TDI is selected. When used as TDI, this input signal provides the serial data port for loading the various JTAG shift registers composed of the boundary scan register, the bypass register, and the instruction register. Shifting in of data depends on the state of the JTAG controller state machine and the instruction currently in the instruction register. This data shift occurs on the rising edge of TCK. TDI also has an internal pullup so that if it is not driven low its value will default to a logic level of 1. However, if TDI will not be used, it should be tied to VDD. This pin also provides the single-bit communication for the debug module commands.

8.20.5 Test Data Output/Development Serial Output

The TDO/DSO is a dual-function pin. When TEST[3:0] = 0001, then DSO is selected. When TEST[3:0] = 0000, TDO is selected. When used as TDO, this output signal provides the serial data port for outputting

Table 17. DC Electrical Specifications (Vcc = 3.3 Vdc ± 0.3 Vdc)

Characteristic	Symbol	Min	Max	Units
Operation Voltage Range for I/O	V_{cc}	3.0	3.6	V
Input High Voltage	V_{IH}	2	5.5	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current @ 0.0 V /3.3 V During Normal Operation	I_{in}	-	±1	μμA
Hi-Impedance (Three-State) Leakage Current @ 0.0 V/3.3 V During Normal Operation	I_{TSI}	-	±1	μμA
Output High Voltage I_{OH} = 8mA[1], 4mA[2], 2mA[3]	V_{OH}	2.4	-	V
Output Low Voltage I_{OL} = 8mA[1], 4mA[2], 2mA[3]	V_{OL}	-	0.4	V
Schmitt Trigger Low to High Threshold Point[6]	V_{T+}	1.47	-	V
Schmitt Trigger High to Low Threshold Point[6]	V_{T-}	-	.95	V
Load Capacitance (DATA[31:16], DCL0, DCL1, SCLK[4:1], SCLKOUT, EBUOUT[2:1], LRCK[4:1], SDATAO[2:1], CFLG, EF, DBCDDATA[3:0], DBCPST[3:0], CNPSTCLK, IDEDIOR, IDEDIOW, IORDY, SRE, SWE)	C_L	-	50	pF
Load Capacitance (ADDR[25, 23:9], SCLK)	C_L	-	40	pF
Load Capacitance (BCLKE, SDCAS, SDRAS, SDLDQM, SDRAMCS[2:1],, SDUDQM, SDWE, BUFENB[2:1])	C_L	-	30	pF
Load Capacitance (SDA, SDA2, SCL, SCL2, CMDSDIO2, SDATA2BS2, SDATA1BS1, SDATA0SDIO1, CS[1:0], OE, R/$\overline{W}$, TA, TXD[2:0], XTRIM, TDO/DSO, RCK, SFSY, SUBR, SDATA3, TOUT[1:0], QSPIDOUT, QSPICS[3:0], GP[6:5])	C_L	-	20	pF
Capacitance[5], V_{in} = 0 V, f = 1 MHz	C_{IN}	-	6	pF

1. DATA[31:16], ADDR[25, 23:9], PSTCLK, SCLK
2. SCL, SDA, PST[3:0], DDATA[3:0], TDSO, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, $\overline{SDRAMCS}$[2:1], $\overline{SDLDQM}$, $\overline{SDUDQM}$, R/$\overline{W}$
3. TOUT[1:0], RTS[2:0], TXD[2:1], SCLK[4:1]
4. $\overline{BKPT}$/TMS, DSI/TDI, DSCLK/$\overline{TRST}$
5. Capacitance C_{IN} is periodically sampled rather than 100% tested.
6. SCLK[4:1], SCL, SCL2, SDA, SDA2, CRIN, RSTI

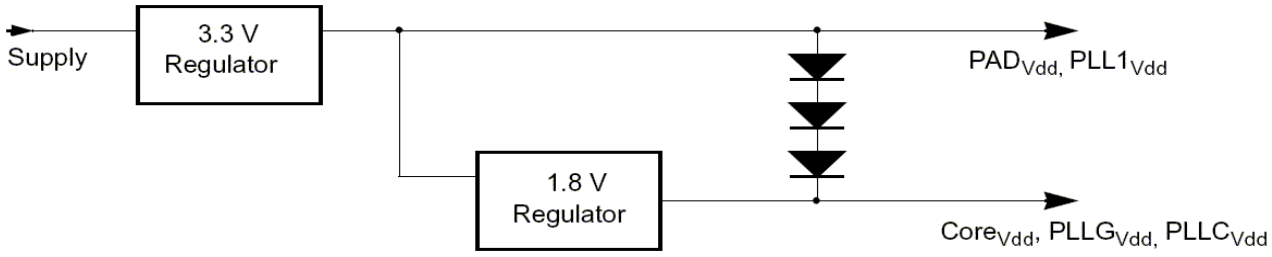

Figure 3. Example Circuit to Control Supply Sequencing

When a DC-DC convertor is used in the system to generate the 1.8V supply, additional care is required. If possible, the 1.8V DC-DC convertor should be supplied by the 3.3V supply. If this is impossible or considered inefficient, the designer needs to ensure that the rise time of the 1.8V supply still complies with the recommendations stated above. Adding the 3 diodes will help resolve issues associated with a slow rise time of the 1.8V supply. Further, a Schotty diode could be added between the supplies, which would have the effect of holding the 1.8V supply to match the 3.3V supply should the 1.8V supply come-up first. This diode also has the function of ensuring that there is not a large voltage differential between the Core supply and the PAD supply during power-down.

Refer to the *M5249C3 Reference Board Useris Manual* for the recommended diode types.

A further note is the recommendation for hard resetting of the device. Freescale recommends using a dynamic reset circuit. This allows for control of the voltage at which the reset will be released and ensure that the correct voltage level at the RESET pin is achieved in all cases. Passive (RC) reset networks do not always achieve the desired results.

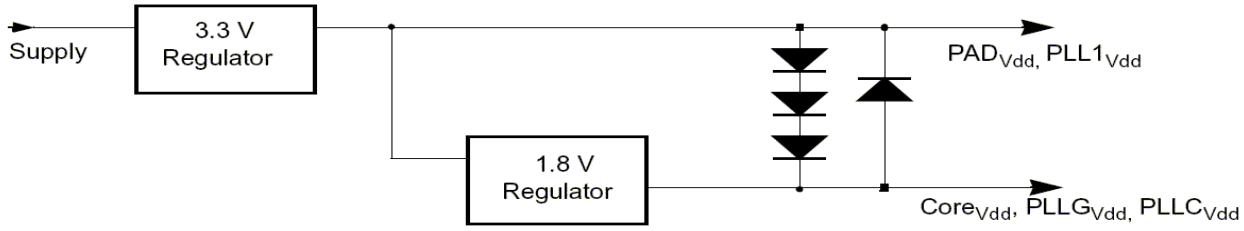

Figure 4. SCF5249 Power Supply

NOTE

The following signals are not available on the 144 QFP package.

Table 18. 160 MAPBGA Ball Assignments

160MAPBGA Ball Number	Function	GPIO
E3	CMD_SDIO2	GPIO34
G4	SDATA0-SDIO1	GPIO54
H3	RSTO/SDATA2_BS2	
K3	A25	GPO8

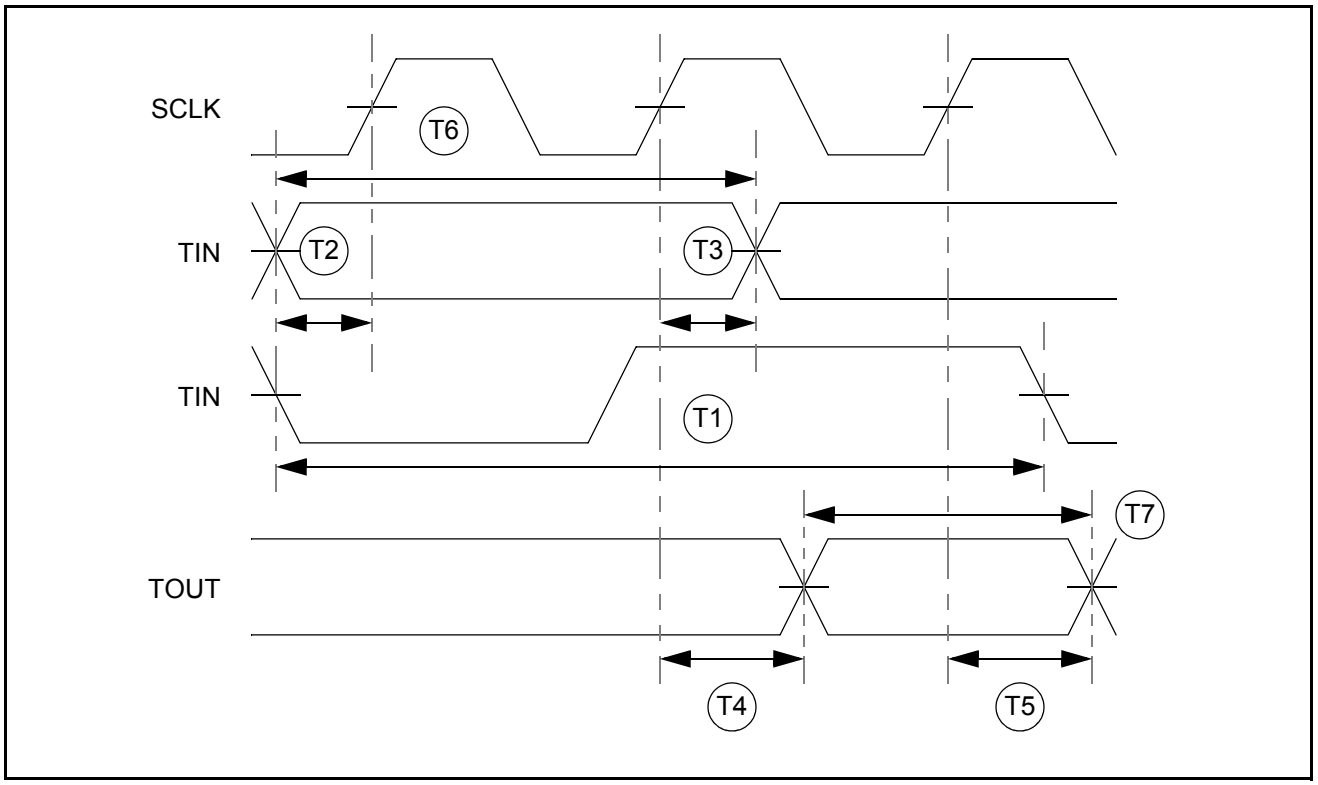

Figure 11. Timer Module Timing Definition

Table 25. UART Module AC Timing Specifications

Num	Characteristic	Min	Max	Units
U1	RXD Valid to BCLK (input setup)	tbd	—	nSec
U2	SCLK to RXD Invalid (input hold)	tbd	—	nSec
U3	$\overline{\text{CTS}}$ Valid to SCLK (input setup)	tbd	—	nSec
U4	SCLK to $\overline{\text{CTS}}$ Invalid (input hold)	tbd	—	nSec
U5	SCLK to TXD Valid (output valid)	---	tbd	nSec
U6	SCLK to TXD Invalid (output hold)	tbd	—	nSec
U7	SCLK to $\overline{\text{RTS}}$ Valid (output valid)	---	tbd	nSec
U8	SCLK to $\overline{\text{RTS}}$ Invalid (output hold)	tbd	—	nSec

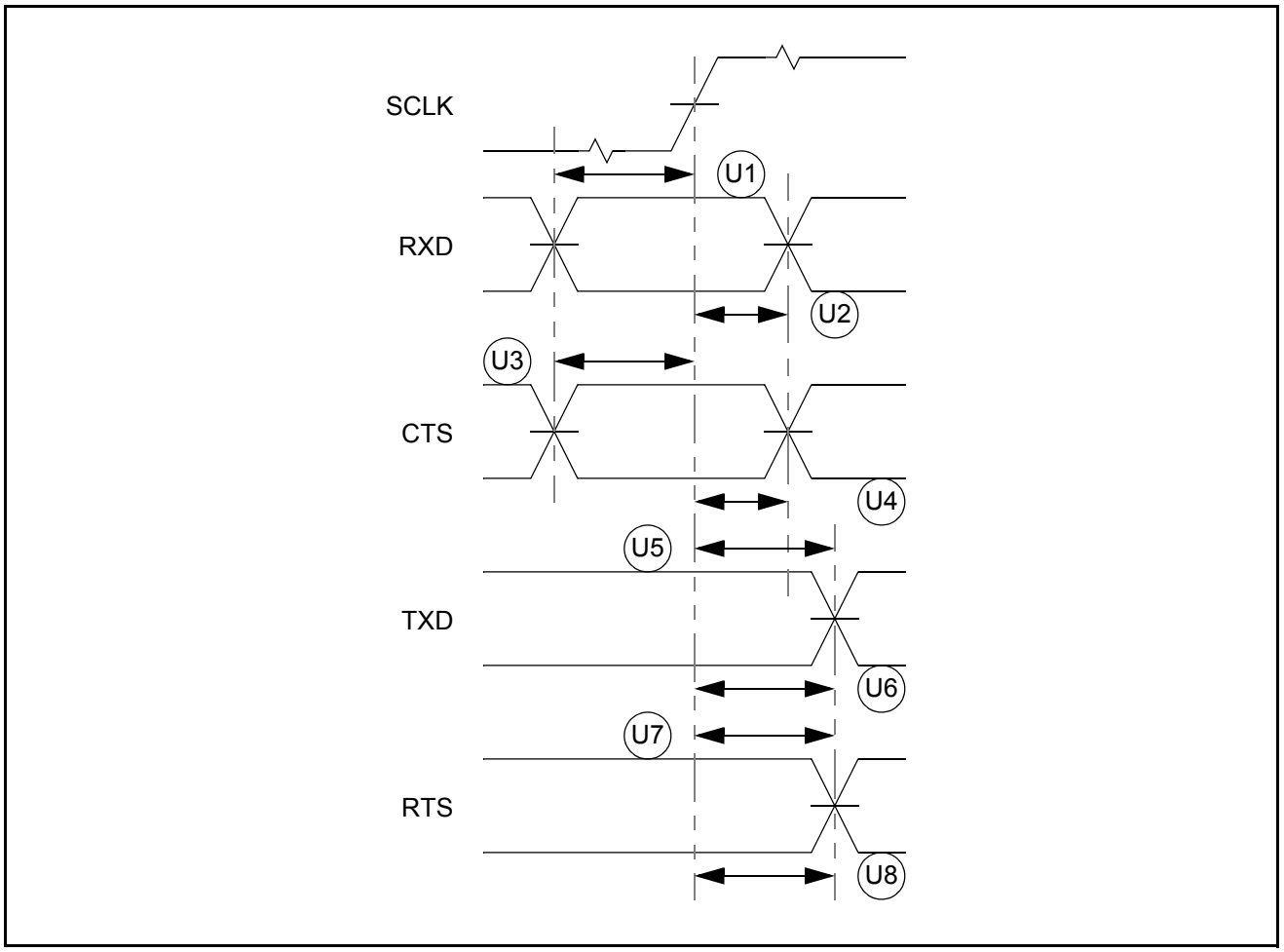

Figure 12. UART Timing Definition

Table 26. I2C-Bus Input Timing Specifications Between SCL and SDA

Num	Characteristic	Min	Max	Units
M1	Start Condition Hold Time	tbd	—	bus clocks
M2	Clock Low Period	tbd	—	bus clocks
M3	SCL/SDA Rise Time (VIL= 0.5 V to VIH = 2.4 V)	—	tbd	mSec
M4	Data Hold Time	tbd	—	nSec
M5	SCL/SDA Fall Time (VIH= 2.4 V to VIL = 0.5 V)	—	tbd	mSec
M6	Clock High time	tbd	—	bus clocks
M7	Data Setup Time	tbd	—	nSec
M8	Start Condition Setup Time (for repeated start condition only)	tbd	—	bus clocks

Table 28. I2C Output Bus Timings

Num	Characteristic	Min	Max	Units
M10[3]	SCL, SDA Valid to SCLK (input setup)	tbd	—	nSec
M11	SCLK to SCL, SDA Invalid (input hold)	tbd	—	nSec
M12[1]	SCLK to SCL, SDA Low (output valid)	—	tbd	nSec
M13[2]	SCLK to SCL, SDA Invalid (output hold)	tbd	—	nSec

1. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are driven low by the processor. The time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
2. Since SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, this specification applies only when SCL or SDA are actively being driven or held low by the processor.
3. SCL and SDA are internally synchronized.This setup time must be met only if recognition on a particular clock is required.

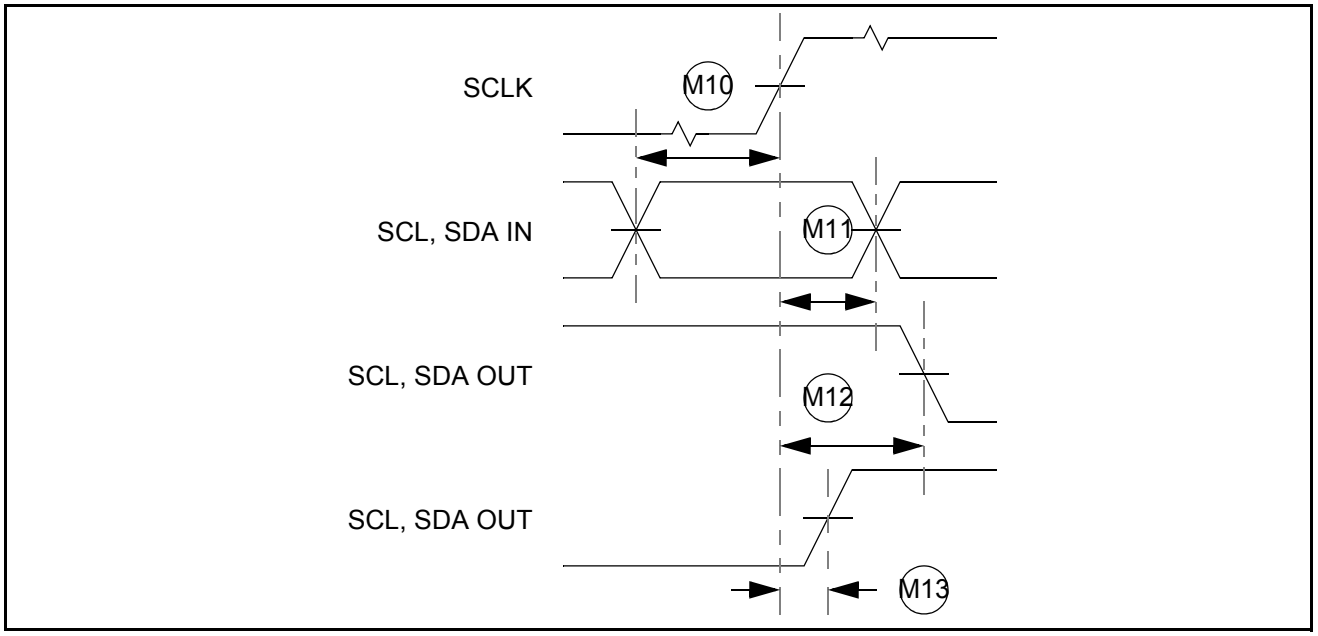

Figure 14. I²C and System Clock Timing Relationship

Table 29. General-Purpose I/O Port AC Timing Specifications

Num	Characteristic	Min	Max	Units
P1	GPIO Valid to SCLK (input setup)	tbd	—	nSec
P2	SCLK to GPIO Invalid (input hold)	tbd	—	nSec

Table 34. 144 QFP Pin Assignments (continued)

144 QFP Pin Number	Name	Type	Description
116	DDATA2/GPIO2	I/O	debug
117	CTS2_B/ADIN3/GPI31	I	second UART clear / AD input 3
118	DDATA0/GPIO0	I/O	debug
119	RXD2/GPI28/ADIN2	I	second UART receive data input / AD input 2
120	TDSO	O	JTAG/debug
121	RTS2_B/GPO31	O	second UART request to send
122	SDATAI3/GPI41	I	audio interfaces serial data input 3
123	CTS1_B/GPI30	I	first UART clear to send
124	TXD2/GPO28	O	second UART transmit data output
125	RTS1_B/GPO30	O	first UART request to send
126	EBUIN4/ADIN1/GPI39	I	audio interfaces EBU input 4 / AD input 1
127	TXD1/GPO27	O	first UART transmit data output
128	128 RXD1/GPI27	I	first UART receive data input
129	CS1/GPIO58	I/O	chip select 1
130	CORE-GND		CORE-GND
131	A1	O	SDRAM address / static adr
132	TIN1/GPIO23	I/O	Timer input 1
133	A2	O	address
134	A3	O	address
135	PAD-GND		PAD-GND
136	A4	O	address
137	A6	O	address
138	A5	O	address
139	A8	O	address
140	A7	O	address