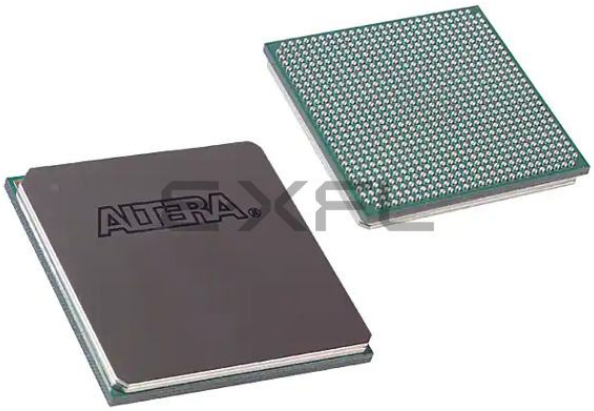
Intel - 10CX105YF780I6G Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	38000
Number of Logic Elements/Cells	104000
Total RAM Bits	8641536
Number of I/O	284
Number of Gates	-
Voltage - Supply	0.9V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10cx105yf780i6g

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Symbol	Description	Condition	Minimum	Maximum	Unit
I_{OUT}	DC output current per pin	—	–25 (2)(3)(4)(5)(6)	25	mA
T_J	Operating junction temperature	—	–55	125	°C
T_{STG}	Storage temperature (no bias)	—	–65	150	°C

Related Information

- AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.
- Power-Up and Power-Down Sequences, Power Management in Intel Cyclone 10 GX Devices chapter
  Provides the power sequencing requirements for Intel Cyclone 10 GX devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 2.70 V for LVDS I/O can only be at 2.70 V for ~4% over the lifetime of the device.

---

(2) The maximum current allowed through any LVDS I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA.

(3) Total current per LVDS I/O bank must not exceed 100 mA.

(4) Voltage level must not exceed 1.89 V.

(5) Applies to all I/O standards and settings supported by LVDS I/O banks, including single-ended and differential I/Os.

(6) Applies only to LVDS I/O banks. 3 V I/O banks are not covered under this specification and must be implemented as per the power sequencing requirement. For more details, refer to *AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria® 10, and Intel Stratix® 10 Devices* and *Power Management in Intel Cyclone 10 GX Devices chapter*.

Symbol	Description	Condition	Minimum [8]	Typical	Maximum [8]	Unit
		1.2 V	1.14	1.2	1.26	V
V_{CCERAM}	Embedded memory power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} [9]	Battery back-up power supply (For design security volatile key register)	1.8 V	1.71	1.8	1.89	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3.0	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.35 V	[10]	1.35	[10]	V
		1.25 V	1.19	1.25	1.31	V
		1.2 V	[10]	1.2	[10]	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V

continued...

(8) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) If you do not use the design security feature in Intel Cyclone 10 GX devices, connect V_{CCBAT} to a 1.5-V to 1.8-V power supply. Intel Cyclone 10 GX power-on reset (POR) circuitry monitors V_{CCBAT}. Intel Cyclone 10 GX devices do not exit POR if V_{CCBAT} is not powered up.

(10) For minimum and maximum voltage values, refer to the I/O Standard Specifications section.

Single-Ended I/O Standards Specifications

Table 12. Single-Ended I/O Standards Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} [20] (mA)	I_{OH} [20] (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.3	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 13. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Cyclone 10 GX Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135/ SSTL-135 Class I, II	1.283	1.35	1.418	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125/ SSTL-125 Class I, II	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-12/ SSTL-12 Class I, II	1.14	1.2	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}

continued...

(20) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.0-V LVTTL specification (2 mA), you should set the current strength settings to 2 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

Symbol/Description	Condition	Min	Typ	Max	Unit
t_{LTR} (40)	—	—	—	10	µs
t_{LTD} (41)	—	4	—	—	µs
t_{LTD_manual} (42)	—	4	—	—	µs
$t_{LTR_LTD_manual}$ (43)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR PPM tolerance	PCIe-only	-300	—	300	PPM
	All other protocols	-1000	—	1000	PPM
Programmable DC Gain	Setting = 0-4	0	—	10	dB
Programmable AC Gain at High Gain mode and Data Rate ≤ 6 Gbps	Setting = 0-28 V_{CCR_GXB} = 0.95 V	0	—	19	dB
	Setting = 0-28 V_{CCR_GXB} = 1.03 V	0	—	21	dB

Table 26. Transmitter Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	—	High Speed Differential I/O (44)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω

continued...

(40) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(41) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(42) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(43) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(44) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Cyclone 10 GX transceivers.

Symbol/Description	Condition	Min	Typ	Max	Unit
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 0.95 V	—	450	—	mV
	V_{CCT_GXB} = 1.03 V	—	500	—	mV
Rise time [45]	20% to 80%	20	—	130	ps
Fall time [45]	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate setting of SLEW_R5 [46]	—	—	15	ps

Table 27. Typical Transmitter V_{OD} Settings

Symbol	V_{OD} Setting	V_{OD}-to-V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}-to-V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70

continued...

(45) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the design configurations.

(46) SLEW_R1 is the slowest and SLEW_R5 is the fastest. SLEW_R6 and SLEW_R7 are not used.

Symbol	V_{OD} Setting	V_{OD}-to-V_{CCT_GXB} Ratio
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

Table 28. Transmitter Channel-to-channel Skew Specifications

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps
xN Clock	Within 2 banks	230	ps
PLL Feedback Compensation [47], [48]	Side-wide	1600	ps

Related Information

PLLs and Clock Networks

(47) `refclk` is set to 125 MHz during the test.

(48) You can reduce the lane-to-lane skew by increasing the reference clock frequency.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	50	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} (50)(51)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.13	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	650	ps (p-p)
t_{OUTPJ} (52)	Period jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} (52)	Cycle-to-cycle jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(50) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(51) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(52) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	—	10	—	—	ns
t_{INCCJ} (54)(55)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.15	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	750	ps (p-p)
t_{OUTPJ_DC}	Period jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} (56)	Period jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} (56)	Cycle-to-cycle jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
$t_{CASC_OUTPJ_DC}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)

Related Information

Memory Output Clock Jitter Specifications on page 43
Provides more information about the external memory interface clock output jitter specifications.

(54) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(55) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(56) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Intel Cyclone 10 GX Devices table.

External Temperature Sensing Diode Specifications

Table 35. External Temperature Sensing Diode Specifications for Intel Cyclone 10 GX Devices

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third party external diode ADC and integration specifics.

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	100	µA
V_{bias}, voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	—	1.03	—	—

Internal Voltage Sensor Specifications

Table 36. Internal Voltage Sensor Specifications for Intel Cyclone 10 GX Devices

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	—	6	Bit
Sampling rate		—	—	500	Ksps
Differential non-linearity (DNL)		—	—	±1	LSB
Integral non-linearity (INL)		—	—	±1	LSB
Gain error		—	—	±1	%
Offset error		—	—	±1	LSB
Input capacitance		—	20	—	pF
Clock frequency		0.1	—	11	MHz
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.5	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.25	V

Symbol		Condition	–E5, –I5			–E6, –I6			Unit
			Min	Typ	Max	Min	Typ	Max	
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate) (59)	SERDES factor J = 4 to 10 (60)(61)(62)	(62)	—	1434	(62)	—	1250	Mbps
		SERDES factor J = 3 (60)(61)(62)	(62)	—	1076	(62)	—	938	Mbps
		SERDES factor J = 2, uses DDR registers	(62)	—	275 (63)	(62)	—	250 (63)	Mbps
		SERDES factor J = 1, uses DDR registers	(62)	—	275 (63)	(62)	—	250 (63)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.12	—	—	0.15	UI
	t_{DUTY} (64)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	%
	$t_{RISE\ \&}$ & t_{FALL} (61) (65)	True Differential I/O Standards	—	—	180	—	—	200	ps

continued...

(59) Requires package skew compensation with PCB trace length.

(60) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(61) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(62) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(63) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

(64) Not applicable for `DIVCLK` = 1.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.4 Gbps

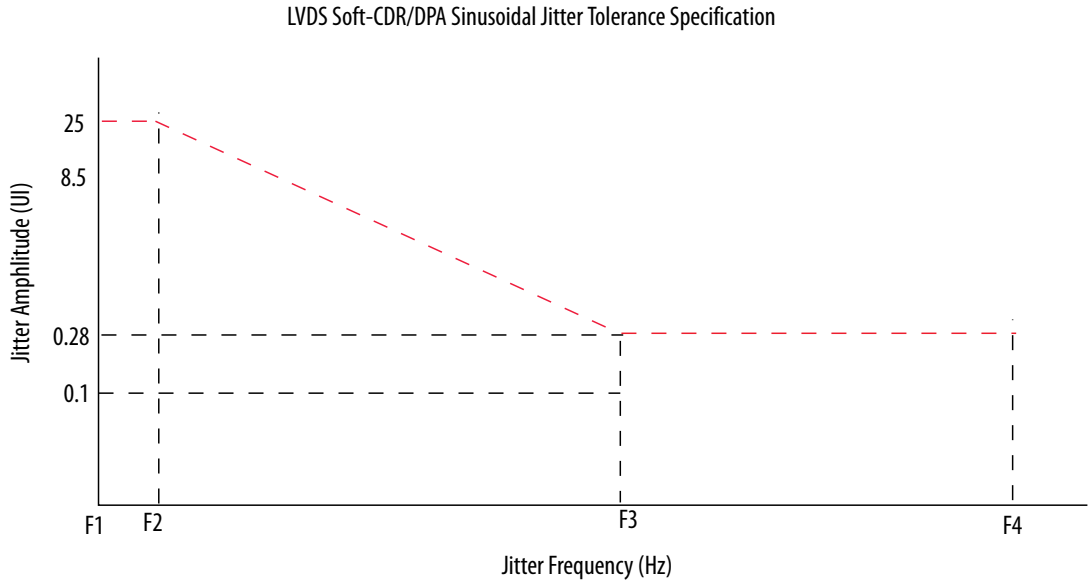
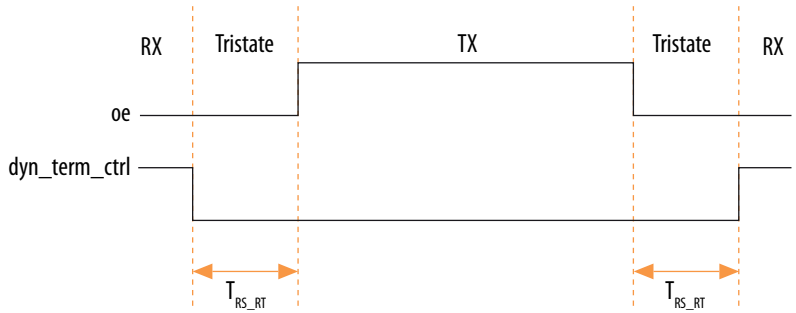


Table 39. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.4 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.28
F4	50,000,000	0.28

Figure 5. Timing Diagram for on oe and dyn_term_ctrl Signals



Configuration Specifications

This section provides configuration specifications and timing for Intel Cyclone 10 GX devices.

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

Table 45. Fast and Standard POR Delay Specification for Intel Cyclone 10 GX Devices

POR Delay	Minimum	Maximum	Unit
Fast	4	12 [68]	ms
Standard	100	300	ms

Related Information

MSEL Pin Settings
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

[68] The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

JTAG Configuration Timing

Table 46. JTAG Timing Parameters and Values for Intel Cyclone 10 GX Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30, 167 (69)	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

FPP Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

(69) The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

Table 47. DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices

You cannot turn on encryption and compression at the same time for Intel Cyclone 10 GX devices.

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] Ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
FPP (32-bit wide)	Off	Off	1
	On	Off	4
	Off	On	8

FPP Configuration Timing when DCLK-to-DATA[] = 1

Note: When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Intel Cyclone 10 GX Devices table.

Table 48. FPP Timing Parameters When the DCLK-to-DATA[] Ratio is 1 for Intel Cyclone 10 GX Devices

Use these timing parameters when the decompression and design security features are disabled.

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (70)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (71)	µs

continued...

(70) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

Related Information

- PS Configuration Timing on page 50
- AS Configuration Timing
  Provides the AS configuration timing waveform.

DCLK Frequency Specification in the AS Configuration Scheme

Table 51. DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme.

The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

You can only set 12.5, 25, 50, and 100 MHz in the Intel Quartus Prime software.

Parameter	Minimum	Typical	Maximum	Intel Quartus Prime Software Settings	Unit
DCLK frequency in AS configuration scheme	5.3	7.5	9.7	12.5	MHz
	10.5	15.0	19.3	25.0	MHz
	21.0	30.0	38.5	50.0	MHz
	42.0	60.0	77.0	100.0	MHz

PS Configuration Timing

Table 52. PS Timing Parameters for Intel Cyclone 10 GX Devices

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	480	1,440	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	320	960	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	3,000 (78)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	3,000 (79)	µs

continued...

Initialization

Table 53. Initialization Clock Source Option and the Maximum Frequency for Intel Cyclone 10 GX Devices

Initialization Clock Source	Configuration Scheme	Maximum Frequency (MHz)	Minimum Number of Clock Cycles
Internal Oscillator	AS, PS, and FPP	12.5	600
CLKUSR [82][83]	AS, PS, and FPP	100	

Configuration Files

There are two types of configuration bit stream formats for different configuration schemes:

- PS and FPP—Raw Binary File (`.rbf`)
- AS—Raw Programming Data File (`.rpd`)

The `.rpd` file size follows the Intel configuration devices capacity. However, the actual configuration bit stream size for `.rpd` file is the same as `.rbf` file.

(82) To enable CLKUSR as the initialization clock source, in the Intel Quartus Prime software, select **Device and Pin Options ➤ General ➤ Device initialization clock source ➤ CLKUSR pin**.

(83) If you use the CLKUSR pin for AS and transceiver calibration simultaneously, the only allowed frequency is 100 MHz.

Minimum Configuration Time Estimation

Table 55. Minimum Configuration Time Estimation for Intel Cyclone 10 GX Devices

The estimated values are based on the uncompressed configuration bit stream sizes in the Configuration Bit Stream Sizes for Intel Cyclone 10 GX Devices table.

Variant	Product Line	Active Serial [84]			Fast Passive Parallel [85]		
		Width	DCLK (MHz)	Minimum Configuration Time (ms)	Width	DCLK (MHz)	Minimum Configuration Time (ms)
Intel Cyclone 10 GX	GX 085	4	100	204.81	32	100	25.60
	GX 105	4	100	204.81	32	100	25.60
	GX 150	4	100	204.81	32	100	25.60
	GX 220	4	100	204.81	32	100	25.60

Related Information

- Configuration Files on page 52
- DCLK Frequency Specification in the AS Configuration Scheme on page 50
  Provides the DCLK frequency using internal oscillator.

(84) The minimum configuration time is calculated based on DCLK frequency of 100 MHz. Only external CLKUSR may guarantee the frequency accuracy of 100 MHz. If you use internal oscillator of 100 MHz, you may not get the actual frequency of 100 MHz. For the DCLK frequency using internal oscillator, refer to the DCLK Frequency Specification in the AS Configuration Scheme table.

(85) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

AN775: I/O Timing Information Generation Guidelines
Provides the techniques to generate I/O timing information using the Intel Quartus Prime software.

Programmable IOE Delay

Table 58. IOE Programmable Delay for Intel Cyclone 10 GX Devices

For the exact values for each setting, use the latest version of the Intel Quartus Prime software. The values in the table show the delay of programmable IOE delay chain with maximum offset settings after excluding the intrinsic delay (delay at minimum offset settings).

Programmable IOE delay settings are only applicable for I/O buffers and do not apply for any other delay elements in the PHYLite for Parallel Interfaces Intel Cyclone 10 FPGA IP core.

Parameter [89]	Maximum Offset	Minimum Offset [90]	Fast Model		Slow Model		Unit
			Extended	Industrial	–E5, –I5	–E6, –I6	
Input Delay Chain Setting (`IO_IN_DLY_CHN`)	63	0	2.012	2.003	5.241	6.035	ns
Output Delay Chain Setting (`IO_OUT_DLY_CHN`)	15	0	0.478	0.475	1.263	1.462	ns

Glossary

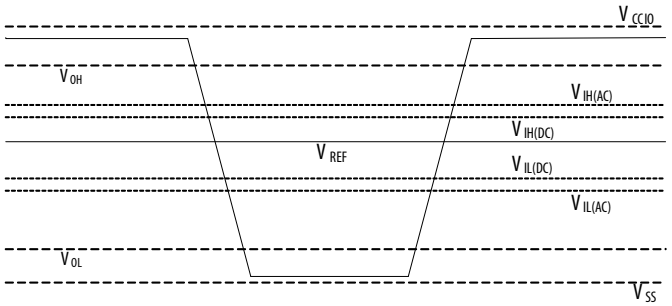
Table 59. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms

continued...

(89) You can set this value in the Intel Quartus Prime software by selecting **Input Delay Chain Setting** or **Output Delay Chain Setting** in the **Assignment Name** column.

(90) Minimum offset does not include the intrinsic delay.

Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%)
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
t_{RISE}	Signal low-to-high transition time (20–80%)
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.

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